PMC-Sierra, Inc.

USING EXTERNAL PULL-DOWN RESISTORS WITH 5V TOLERANT 3.3V INPUTS

RELEASED

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REVISION HISTORY

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1	December 2001	Jeff Brown	Document created.
2	November 2002	Bill Richardson	Customer Notification

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1 INTRODUCTION

This document relates to specific PMC-Sierra devices having a 3.3V core voltage and 5V tolerant input pins. 5V tolerance allows these 3.3V devices to connect to legacy 5V devices without requiring external voltage converters. A list of the relevant devices and pins is provided below. This document applies only if you are connecting these inputs to a tri-state bus and you are considering using external pull-down resistors to force one or more of the lines on this bus to zero when it is tri-stated.

These input pins/pads exhibit a temporary active pull-up behavior for a small portion of the signal transition. The only situation where this could have an impact on the circuit design is when an external pull-down resistor is used on a tri-stated line. This application note describes the behavior of these input pins/pads and provides simple design guidelines for you to use if you are considering attaching an external pull-down to these inputs.

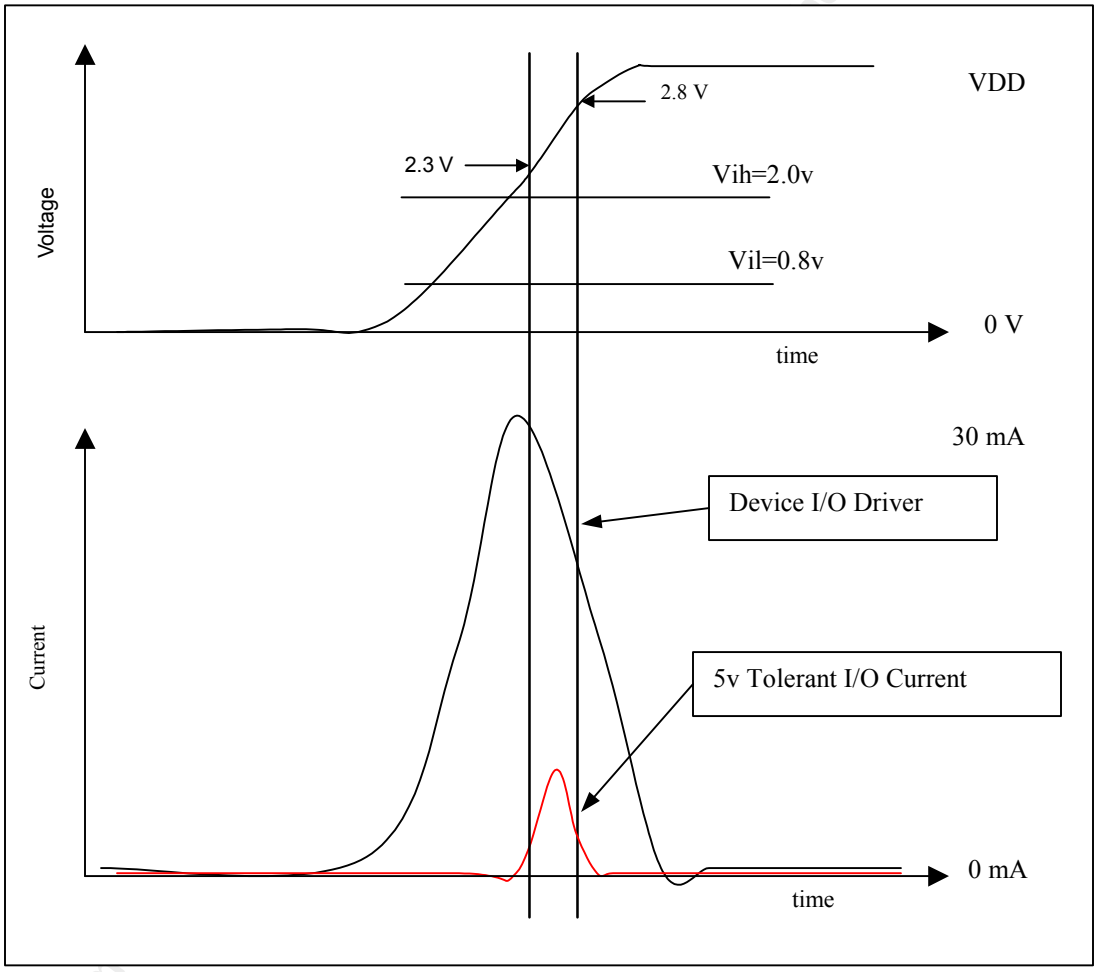
TABLE 1 Relevant Device I/Os

Device	5V Tolerant I/Os
PM4388 (TOCTL) PM6388 (EOCTL) PM5351 (S/UNI Tetra) PM5349 (S/UNI Quad) PM5313 (Spectra-622) PM7346 (QJET) PM7347 (JET) PM7349 (4xD3F) PM7339 (CDB) PM4351 (Comet) PM5356 (S/UNI-622 Max) PM5357 (S/UNI-622POS) PM7351 (S/UNI-VORTEX) PM7350 (S/UNI-DUPLEX)	Bi-directional data bus. D[7:0]
PM7324 (S/UNI Atlas)	Bi-directional data bus. D[15:0]

2 5V TOLERANT INPUT BEHAVIOR

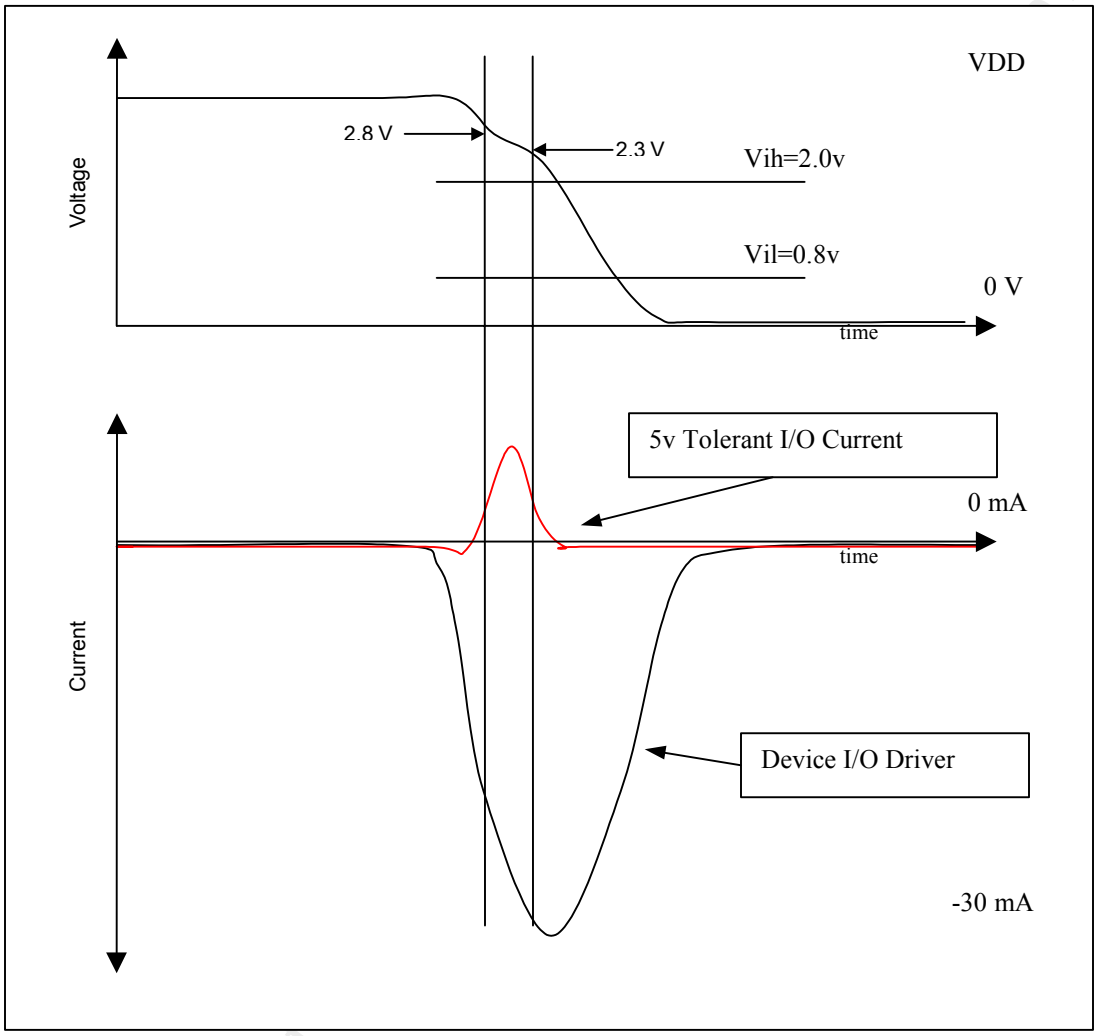
These devices have a 3.3v core, but contain I/O pads designed to tolerate 5v inputs for connection to legacy systems. With these 5v tolerant pads, as the input voltage transitions between 2.3v to 2.8v up to 2.0ma (Vdd = 3.65v, Vbias = 3.65v, and the temperature = 85C) of current can be sourced onto the I/O pad. The time during which this additional current is present is determined by the rise or fall time of the transition. **At other levels there is no current present.** Figures 1 and 2, illustrate the effects of the additional current, and are not actual measurements.

Figure 1 - Current and voltage transitions from 0v to Vdd



In the case where the voltage level is driven from a “0” to a “1” (see Figure 1), the current from the 5v tolerant pad will be added to the current that is driven by the external device driver. The added current will increase the slope of the voltage level. Therefore, this will have no significant effect other than slightly improving the rise time response.

Figure 2 - Current and voltage transitions from Vdd to 0v



During the transition of a “1” to a “0” (see Figure 2) the internal pad sources current onto the I/O pin during the transition from 2.8v to 2.3v levels. It can source up to 2.0mA of current during this brief period. To ensure rapid fall times, TTL output drivers are designed to sink large currents. An output driver on the external device will typically sink at least 20ma to 40ma of current during the “Vdd” to “zero” volt transition and hence will not be affected by this characteristic.

Note that if a 5v supply is available on the board, the VBIAS pin can be tied to 5v. This will reduce the maximum current during the transition to less than 350uA.

Table 2 below lists the specific condition where the extra current has any affect. For all other conditions the effects are negligible.

TABLE 2 I/O Pad States

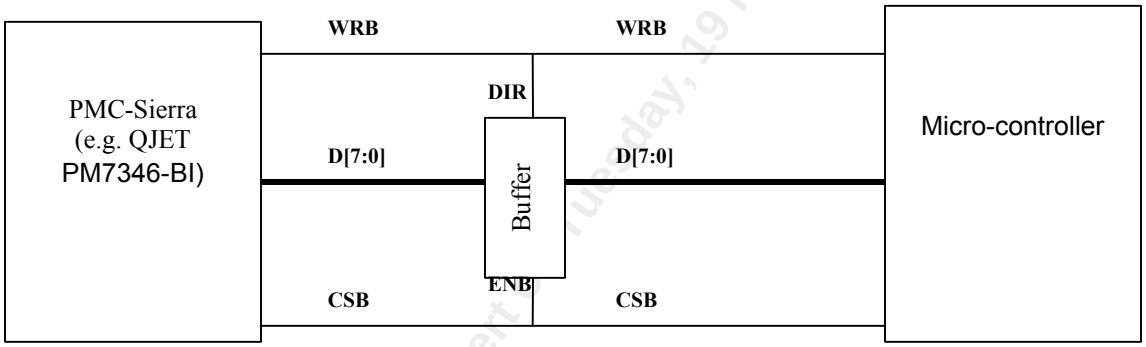
Situation	Condition	Effect
5V tolerant input pin driven by an external device's output pin	'0' → '1' transition	Small amount of extra current put onto the line by the input pad during the transition in the 2.8V to 2.3V region works with the output driver.
	'1' → '0' transition	Small amount of extra current put onto the line by the input pad during the transition in the 2.8V to 2.3V region works against the output driver, but these drivers are able to sink much higher levels of current.
All I/O Pads Tri-stated, with external pull-up resistor	I/O Pads tri-stated with last voltage value a '0'	Tri-stated line will be pulled to a '1'. The internal active pull-up works with the external pull-up while the voltage moves between 2.3V and 2.8V.
	I/O Pads tri-stated with last voltage value a '1'	Tri-stated line will stay at '1'. Since the voltage remains above 2.8V the internal active pull-up will have no impact.
All I/O Pads Tri-stated, with external pull-down resistor	I/O Pads tri-stated with last voltage value a '0'	Tri-stated line will stay at '0'. Since the voltage remains below 2.3V the internal active pull-up will have no impact.
	I/O Pads tri-stated with last voltage value a '1'	**Tri-stated line will be pulled down from a '1' to a '0'. The internal active pull-up works against the external pull-down between 2.8V and 2.3V. A weak pull-down resistor may not be able to pull the tri-stated line to a '0'.**

3 DESIGN GUIDELINE – READING A "ZERO" ON A TRI-STATE BUS

For signals that require a specific value during reset or idle cycles (when the bus is in tri-state), an external pull-down resistor is often used to pull the bus to zero. For example, if a processor needs to read all zeros on the data bus during the reset cycle to put itself in a certain state then an external pull-down may be used. Alternatively, the processor may have this internal pull-down incorporated into its data bus I/O pads.

Because of the I/O pad characteristics described above, a more robust design is to use a buffer between the PMC-Sierra device and any external device reading the tri-stated bus. This is particularly true if the device reading the bus (in this example the processor) has a weak internal pull-down (e.g. 10k ohm). Such a weak pull-down may not be able to pull the tri-stated bus to zero in all operating conditions.

Figure 3 - Buffer added between the PMC-Sierra device and the Micro-controller device



A pull-down resistor strong enough to overcome the 2.0 mA maximum current that the PMC-Sierra device may generate (at worst case conditions) can be used, but is not recommended if the VBIAS input is tied to 3.3v. This resistor would have to be 400 ohms or less, and may draw an undesirable level of current. If the VBIAS input were tied to 5V the external resistor would be 5000 ohms, which is tolerable.

4 REFERENCES

- PM7339 S/UNI-CDB Long Form Datasheet, PMC-2000367, Issue 4
- PM7346 S/UNI-QJET Long Form Datasheet, PMC-960835, Issue 6
- PM7347 S/UNI For J2/E3/T3 (S/UNI-JET) Datasheet, PMC-1990267, Issue 3
- PM7349 S/UNI-4xD3F Data Sheet, PMC-2000314, Issue 5
- PM4388 TOCTL Datasheet, PMC-1960840, Issue 5
- PM6388 EOCTL Datasheet, PMC-1971019, Issue 6
- PM5351 S/UNI-TETRA Long Form Datasheet, PMC-1971240, Issue 7
- PM5349 S/UNI-QUAD Long Form Datasheet, PMC-1971239, Issue 6
- PM5313 SPECTRA-622 Telecom Standard Product Datasheet, PMC-1981162, Issue 6
- PM4351 Combined E1/T1 Transceiver Standard Product Datasheet, PMC-1970624, Issue 10
- PM5356 S/UNI-622-MAX Long Form Datasheet, PMC-1980589, Issue 3
- PM5357 S/UNI-622-POS Long Form Datasheet, PMC-1980911, Issue 5
- PM7350 S/UNI-DUPLEX Dual Serial Link PHY Multiplexer Datasheet, PMC-1980581, Issue 5
- PM7351 Octal Serial Link Multiplexer (S/UNI-VORTEX) Datasheet, PMC-1980582, Issue 5
- PM7324 S/UNI-ATLAS Datasheet, PMC-1971154, Issue 7

NOTES

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