4K-bit TTL bipolar PROM (512 x 8)

82S115

FEATURES

- Address access time: 90ns max
- Input loading: -150μA max
- On-chip storage latches
- Schottky clamped
- Fully TTL compatible
- Outputs: 3-State

APPLICATIONS

- Microprogramming
- Hardware algorithms
- Character generation
- Control store
- Sequential controllers

DESCRIPTION

The 82S115 is field programmable and includes on-chip decoding and 2 chip enable inputs for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations. A D-type latch is used to enable the 3-State output drivers. In the Transparent Read mode, stored data is addressed by applying a binary code to the address inputs while holding Strobe High. In this mode the bit drivers will be controlled solely by $\overline{CE}_1$ and CE_2 lines.

In the Latched Read mode, outputs are held in their previous state (High, Low, or Hi-Z) as long as Strobe is Low, regardless of the state of address or chip enable. A positive Strobe transition causes data from the applied address to reach the output if the chip is enabled, and causes outputs to go to the Hi-Z State if the chip is disabled.

A negative Strobe transition causes outputs to be locked into their last Read Data condition if the chip was enabled, or causes outputs to be locked into the Hi-Z condition if the chip was disabled.

ORDERING INFORMATION

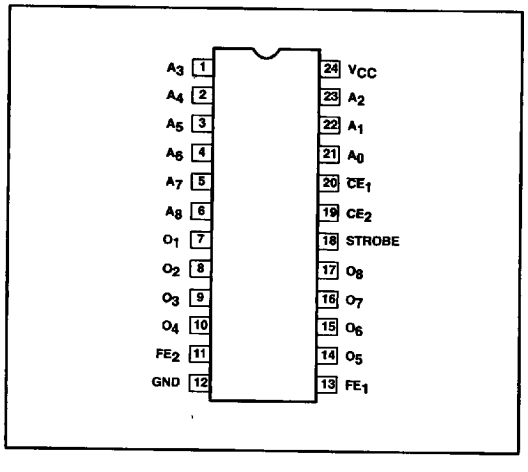
DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
24-Pin Ceramic DIP (600mil-wide)	82S115/BJA	GDIP1-T24
24-Pin Ceramic Flat Pack	82S115/BKA	GDFP2-F24

* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_I, V_O	Input voltage	+5.5	V_{DC}
T_A	Operating temperature range	−55 to +125	°C
T_{STG}	Storage temperature range	−65 to +150	°C

PIN CONFIGURATION



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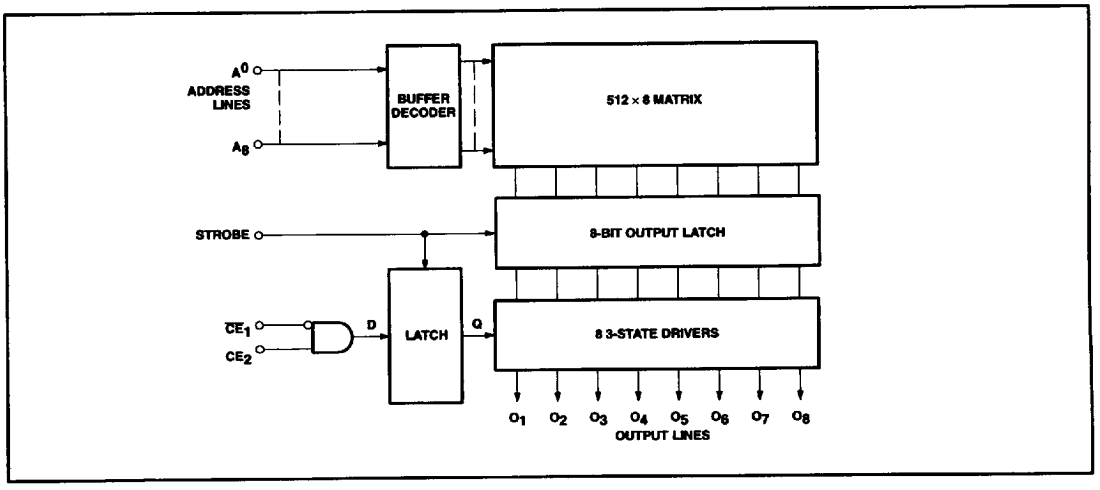
BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS[5]	LIMITS			UNIT
			Min	Typ[8]	Max	
Input voltage						
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IK}	Clamp	V_{CC} = 4.5V, I_I = -18mA		-0.8	-1.2	V
Output voltage						
		$\overline{CE}_1$ = Low, CE_2 = High				
V_{OL}	Low	I_O = 9.6mA		0.4	0.5	V
V_{OH}	High	V_{CC} = 4.5V, I_O = -2mA	2.4			V
Input current[5]						
		V_{CC} = 5.5V				
I_{IL}	Low	V_I = 0.45V			-150	µA
I_{IH}	High	V_I = 5.5V			50	µA
Output current[5]						
		V_{CC} = 5.5V				
I_{OZ}	Hi-Z State	$\overline{CE}_1$ = High or CE_2 = Low, V_O = 5.5V			100	µA
		$\overline{CE}_1$ = High or CE_2 = Low, V_O = 0.5V			-100	µA
I_{OS}	Short circuit[1]	$\overline{CE}_1$ = Low, CE_2 = High, V_O = 0V, High stored	-15		-85	mA
Supply current						
$\overline{CE}_1$ $\overline{CE}_2$ I_{CC}		$\overline{CE}_1$ = High, $\overline{CE}_2$ = Low, V_{CC} = 5.5V		130	185	mA
Capacitance[9]						
		$\overline{CE}_1$ = High or CE_2 = Low, V_{CC} = 5.0V				
C_{IN}	Input	V_I = 2.0V		5	10	pF
C_{OUT}	Output	V_O = 2.0V		8	13	pF

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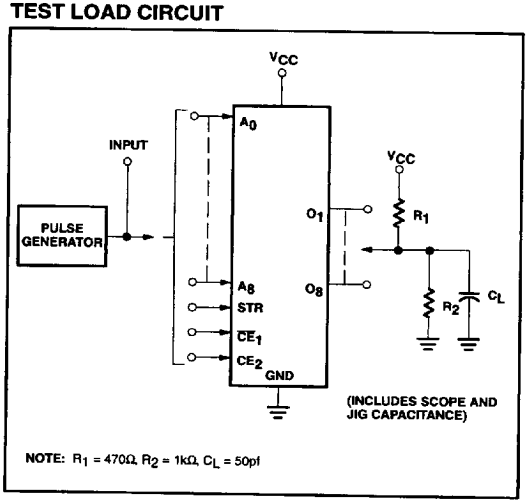
AC ELECTRICAL CHARACTERISTICS -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ[8]	Max	
t_{AA} t_{CE}	Access time[6]	Output Output	Address Chip enable	Latched or transparent Read[2, 4]		40 20	90 50	ns ns
t_{CD}	Disable time	Output	Chip disable	Latched or transparent Read[2, 4]		20	55	ns
t_{CDS} t_{CDH}	Setup time Hold time	Output	Chip enable	Latched Read only3, 4	50 15			
t_{ADH}	Hold time	Address	Strobe	Latched Read only3, 4	5	0		
t_{SW}	Strobe pulse width			Latched Read only3, 4	40	15		ns
t_{SL}	Strobe latch time			Latched Read only3, 4	90	35		ns
t_{DL}	Strobe delatch time			Latched Read only3, 4			45	ns

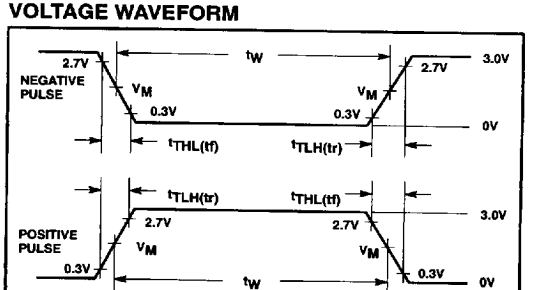
NOTES:
1. No more than one output should be grounded at the same time and strobe should be disabled Strobe is in the High state.
2. If the Strobe is High, the device functions in a manner identical to conventional bipolar ROMs. The timing diagram shows valid data will appear T_{AA} nanoseconds after the address has changed to T_{CE} nanoseconds after the output circuit is enabled. T_{CD} is the time required to disable the output and switch it to an off or High impedance state after it has been enabled.
3. In latched Read Mode data from any selected address will be held on the output when Strobe is lowered only when Strobe is raised will new location data be transferred and chip enable conditions be stored. the new data will appear on the outputs if the chip enable conditions enable the outputs.
4. During operation the fusing pins FE_1 and FE_2 may be grounded or left floating.
5. Positive current is defined as into the terminal referenced.
6. Tested at an address cycle time of 1µs.
7. Areas shown by crosshatch are latched data from previous address.
8. Typical values are at V_{CC} = 5V, T_A = 25°C.
9. Guaranteed, but not tested.

TEST LOAD CIRCUIT



NOTE: R_1 = 470Ω, R_2 = 1kΩ, C_L = 50pf

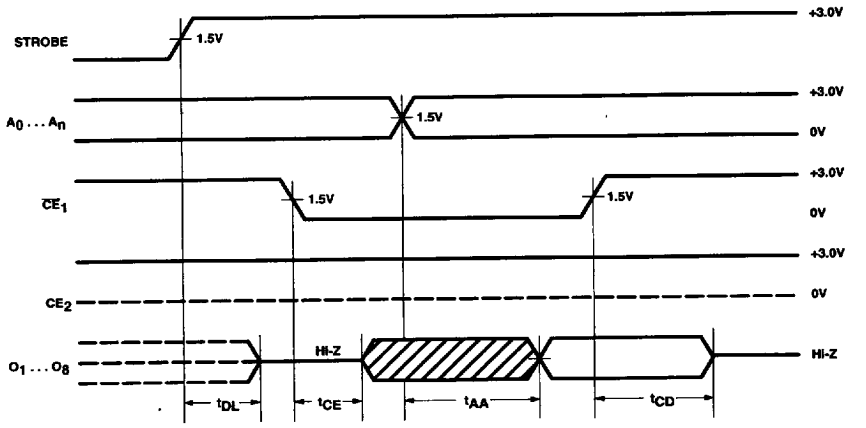
VOLTAGE WAVEFORM



Input Pulse Definition

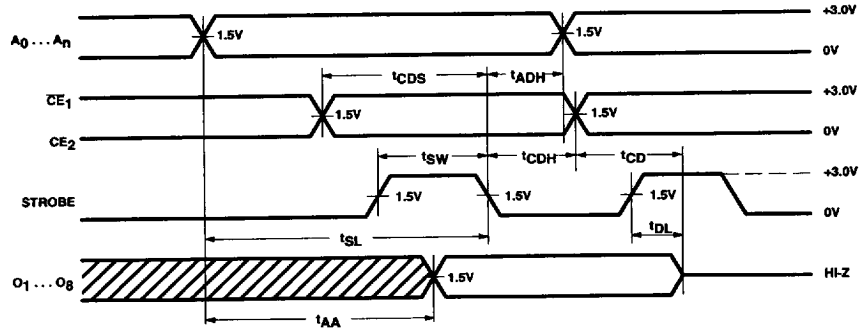
INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

TIMING DIAGRAMS



NOTE:
Output latches not used
All AC measurements at 1.5V unless otherwise specified

Transparent Read[2, 7]



NOTE:
Output latches used
All AC measurements at 1 5V unless otherwise specified

Latched Read[3, 7]