

DATA SHEET

FI1236MK2

Desktop video tuner
system RTMA M/N

Preliminary specification
File under BU Tuners, DC03

1996 Mar 19

Desktop video tuner system RTMA M/N

FI1236MK2

FEATURES

- System RTMA M and N
- True 5 V device (low power dissipation)
- Full frequency range from channel 2 (55.25 MHz) to channel 69 (801.25 MHz)
- PLL controlled tuning
- True-synchronous vision IF demodulator (PLL)
- Demodulated video output, AF sound output, second sound IF output
- I²C-bus control of tuning, address selection, AFC status information
- Complies with FCC and DOC regulations on radiation
- Small horizontally mounted metal housing.

DESCRIPTION

The FI1236MK2 is designed to meet a wide range of RF applications in the PC Multi-Media environment.

The FI1236MK2 types are available with a single 75 Ω input for TV reception. The input connector is available in either standard phono (female socket) or F (female socket).

The tuning and bandswitching are performed through the built-in digitally controlled I²C-bus. All front-ends meet the FCC and DOC radiation requirements.

The FI1236MK2 consists of a tuner section and an IF section, which are all designed on a single PCB. The front-end is assembled in a metal housing made of a rectangular tin plated steel frame with front and rear covers which have soldered contacts to the frame. A single phono or F aerial socket is mounted on one side of the frame. All other connections are made via pins at the bottom.

The tuner section is equipped with 3 tuned RF MOSFET input stages, with a 3-band mixer-oscillator IC, containing the oscillators, mixers and IF amplifier. Tuning and band switching in the tuner section are done with a digital programmable PLL tuning system. This enables tuning with step-size programmable between 31.25, 50.0 or 62.5 kHz. A DC-DC converter is built around the PLL synthesizer IC to provide the tuning voltage, thus making the FI1236MK2 front-end a true 5 V device.

The IF section uses a true-synchronous vision IF demodulator (PLL) with an intercarrier SAW filter in front of it. The analog AFC voltage is fed to the 5-level A/D converter in the PLL tuning IC, so that the AFC status can be read via the I²C-bus.



ORDERING INFORMATION

TYPE	CONNECTOR	CATALOGUE NUMBERS
FI1236MK2/HM/PH	standard phono	3139 147 13251
FI1236MK2/HM/F	F	3139 147 13261

MARKING

The following items of information are printed on a sticker that is on the top cover of the tuner:

- Type number
- Code number
- Origin letter of factory
- Change code
- Year and week code.

INTERMEDIATE FREQUENCIES

SYSTEM	FREQUENCY ⁽¹⁾ (MHz)
	NTSC M/N
Picture carrier	45.75
Colour	42.17
Sound	41.25

Note

1. The oscillator frequency is above the input signal frequency.

CHANNEL COVERAGE

BAND	CHANNELS
Low band	55.25 to 160.00 MHz
Mid band	160.00 to 454.00 MHz
High band	454.00 to 801.25 MHz

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BLOCK DIAGRAM

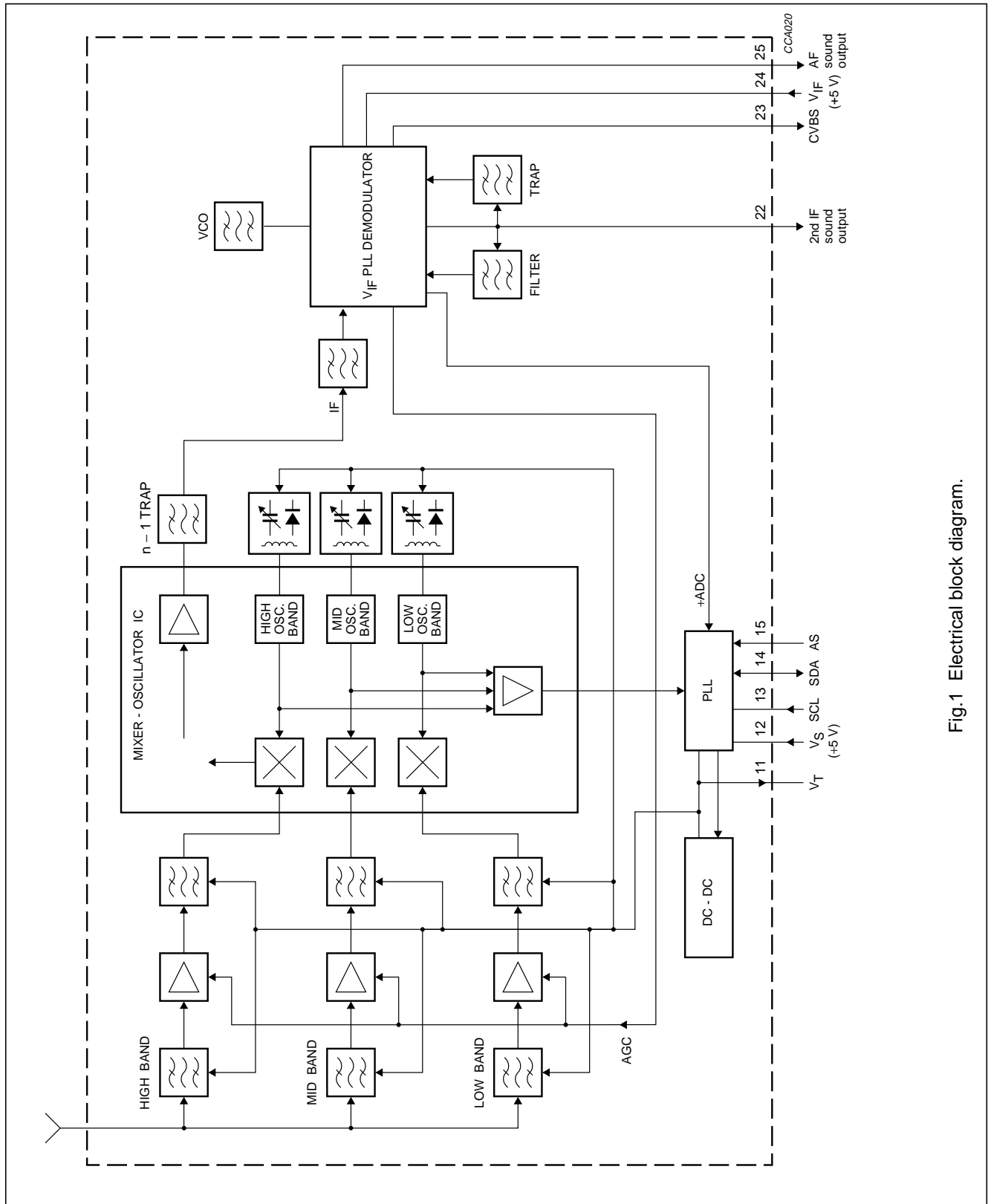


Fig.1 Electrical block diagram.

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F11236MK2**PINNING**

SYMBOL	PIN	DESCRIPTION
V _T	11	tuning voltage (monitor)
V _S	12	supply voltage tuner section +5 V
SCL	13	I ² C-bus serial clock
SDA	14	I ² C-bus serial data
AS	15	I ² C-bus address select
n.c.	21	not connected
2 nd IF sound output	22	second IF sound output
CVBS	23	Composite Video Baseband Signal output
V _{IF}	24	supply voltage IF section +5 V
AF sound output	25	AF sound output
–	TH1, TH2, TH3 and TH4	mounting tags (ground)

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LIMITING VALUES

Limiting values under operational conditions

The tuner can be guaranteed to function properly under the following conditions.

SYMBOL	PARAMETER	PIN	MIN.	TYP.	MAX.	UNIT
V_S	supply voltage	12	4.75	5.00	5.25	V
$V_{S(\text{ripple})}$	peak-to-peak ripple voltage susceptibility (at 5 V \pm 5%); note 1 20 Hz to 100 kHz >100 kHz to 500 kHz		–	–	20	mV
			–	–	10	mV
I_S	supply current		–	–	120	mA
V_{SCL}	SCL bus input voltage	13	–0.3	–	+5.25	V
V_{SDA}	SDA bus input voltage	14	–0.3	–	+5.25	V
I_{SDA}	SDA bus current (open collector)		–1	–	+5	mA
V_{AS}	address select voltage; note 2	15	–	–	+5.25	V
Z_{IF}	2 nd IF sound output load impedance: DC AC	22	0.5	–	–	k Ω
			0.5	–	–	k Ω
Z_{CVBS}	Composite Video Baseband Signal load impedance: DC AC	23	–	75	–	Ω
			–	75	–	Ω
t_L	load time constant		–	–	100	ns
V_{IF}	IF supply voltage	24	4.75	5.0	5.25	V
$V_{IF(\text{ripple})}$	peak-to-peak ripple voltage susceptibility (at 5 V \pm 5%); note 1 20 Hz to 100 kHz >100 kHz to 500 kHz		–	–	20	mV
			–	–	10	mV
I_{IF}	IF supply current		–	–	100	mA
Z_{AF}	AF sound output load impedance: DC AC	25	1.0	–	–	k Ω
			0.6	–	–	k Ω

Notes

1. Sinusoidal ripple voltage superimposed on the 5 V supply voltage in the frequency range of 20 Hz to 500 kHz. Criteria for TV interference >57 dB.
2. For detailed information about the address decoding, refer to Chapter "Application information".

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Environmental conditions

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Non-operational conditions						
T _{amb}	ambient temperature		-25	-	+85	°C
RH	relative humidity		-	-	100	%
g _B	bump acceleration	25 g	-	-	245	m/s ²
g _S	shock acceleration	50 g	-	-	490	m/s ²
	vibration amplitude	10 to 55 Hz	-	0.35	-	mm
Operational conditions						
T _{amb}	ambient temperature		-10	-	+60	°C
RH	relative humidity		-	-	95	%

OVERALL PERFORMANCE

Conditional data

Unless otherwise specified, all electrical values for Chapter "Overall performance" apply at the following conditions.

SYMBOL	PARAMETER	VALUE	UNIT
T _{amb}	ambient temperature	25 ±5	°C
RH	relative humidity	60 ±15	%
V _S	supply voltage (tuner and IF section)	5 ±0.125	V
Z _{CVBS}	video output load impedance (DC)	>75	Ω
Z _{IF}	IF sound output load impedance (DC)	>500	Ω
t _{pr}	pre-heating time (+5 V at pin 24)	10	minute
Z _{S(AE)}	aerial source impedance (unbalanced)	75	Ω

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TUNER SECTION

Tuner characteristics

For detailed information about the PLL programming, refer to Chapter "Application information".

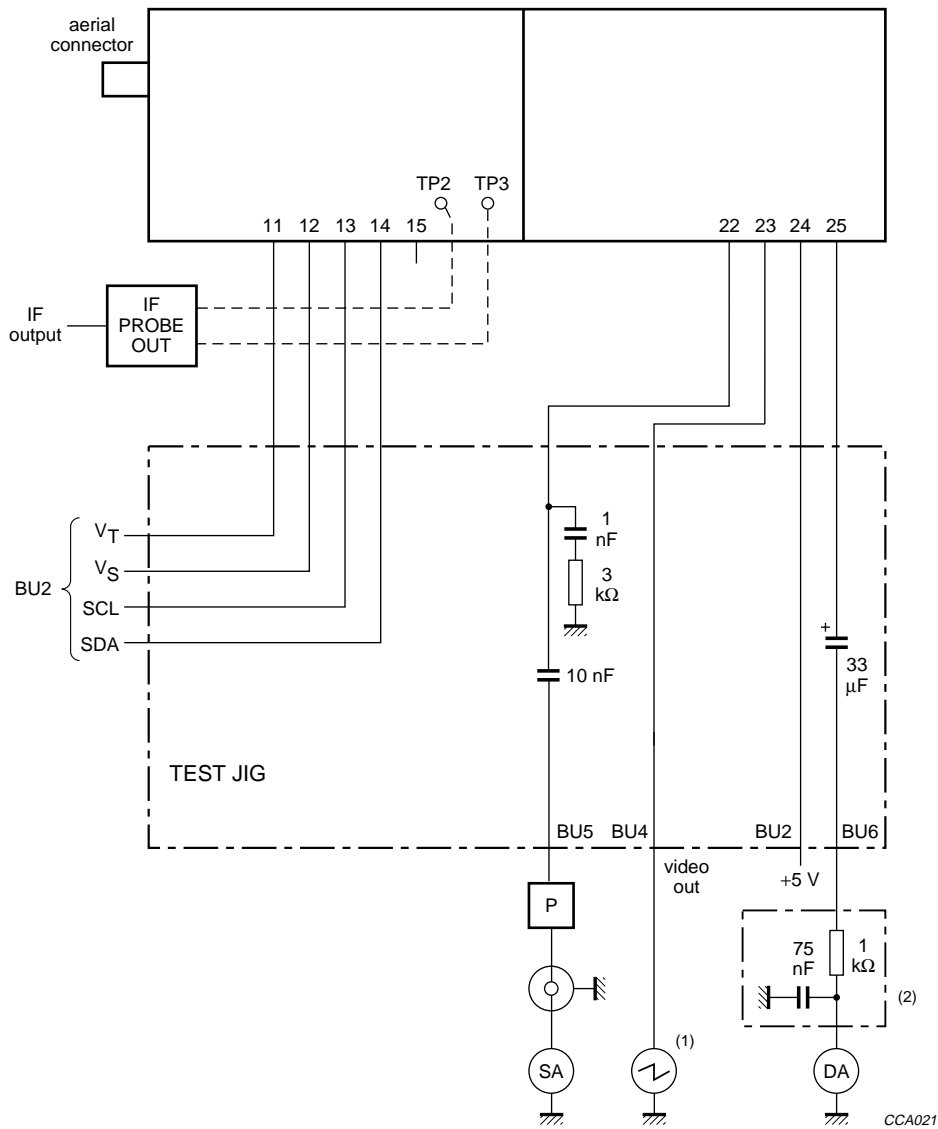
The desktop video tuner is guaranteed to function properly within the specified operational conditions, but a certain deterioration of performance parameters may occur at the limits of the operational conditions.

Test equipment

EQUIPMENT	PARAMETER	VALUE	UNIT
DC voltmeter	input impedance	>1	M Ω
Oscilloscope	input impedance: resistance capacitance	>1 <15	M Ω pF
Spectrum analyzer	input impedance	50	Ω
FET probe	input impedance: resistance capacitance	1 3.5	M Ω pF
	output impedance	50	Ω
	voltage gain	0	dB

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(1) BU4 loaded with 75 Ω.

(2) 75 μs de-emphasis.

SA = spectrum analyzer.

P = FET probe.

DA = distortion analyzer.

The minimum load impedance required at the CVBS output (pin 23) is 75 Ω (both AC and DC).

Fig.2 Typical test set up.

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Definitions of test signals (see Fig.2)

TEST SIGNAL	FREQ. (MHz)	AMPLITUDE	MODULATION	
			VIDEO	AUDIO
A0: unmodulated vision carrier	477.25	60 dB μ V		
A1: RTMA M/N standard signal with video modulation	477.25	60 dB μ V (top sync)	100% (rest carrier 12.5%) 2T pulse and bar	
B1: unmodulated sound carrier M system	481.25	-7 dB w.r.t. A0 to A1		
B2: FM modulated sound carrier M system	481.25	-7 dB w.r.t. A0 to A1		1 kHz; modulation frequency deviation \pm 25 kHz; 75 μ s pre-emphasis
B3: unmodulated sound carrier M system	483.25	-12 dB w.r.t. A0 to A1		

Aerial input characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
VSWR	reflection coefficient	referred to 75 Ω impedance (worst case on or between picture and sound carrier at maximum gain)	-	5	
V _{PSM}	surge protection voltage		5	-	kV
V _{ant}	antenna connection disturbance voltage	54 MHz to <300 MHz	-	34	dB μ V
		300 MHz to <1 000 MHz	-	50	dB μ V

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General characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_b	frequency range: low band mid band high band		55.25 163.25 457.25	– – –	157.25 451.25 801.25	MHz MHz MHz
Δf_b	margin: for low band for mid/high band		1.5 3	– –	– –	MHz MHz
α_i	image rejection (nominal gain to 10 dB gain reduction): low band (channel 2 to 6) mid band (channel 7 to 13) high band (channel 14 to 69)		60 60 50	– – –	– – –	dB dB dB
α_{IF}	IF rejection (picture)		60	–	–	dB
Z_{IF}	$\frac{1}{2}$ IF susceptibility: channel 2 to 13 channel 14 to 69		75 60	– –	– –	dB μ V dB μ V
m_x	cross modulation: in-channel in-band low band ($n \pm 2$) mid band ($n \pm 3$) high band ($n \pm 5$) out of band		65 78 78 84 –	– – – – 100	– – – – –	dB μ V dB μ V dB μ V dB μ V dB μ V
	breakthrough susceptibility: channel 2 to 69		60	–	–	dB μ V
V_{osc}	oscillator voltage at all pins		–	–	70	dB μ V
t_{li}	oscillators lock-in time	charge pump set logic HIGH	–	–	150	ms
α_{vs}	the video signal-to-sound interference ratio with the tuner exposed to sound signals in the audio frequency range 100 Hz to 10 kHz and sound pressure levels up to 105 dB (20 μ Pa)		40	–	–	dB
V_{ESD}	electrostatic discharge (ESD) on all pins	note 1	2	–	–	kV

Note

- All the pins of the desktop video tuner are protected against electrostatic discharge (ESD) up to 2 kV. The product is classified in category B ("MIL-STD-883C").

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Video and audio characteristics (see Fig.2)

PARAMETER	TEST SIGNAL	TEST POINT	MIN.	TYP.	MAX.	UNIT
CVBS characteristics:						
video amplitude signal at pin 23	A1 (peak-to-peak value)	BU4	0.7	–	1.1	V
DC level sync pulse at pin 23	A1	BU4	–	0.35	–	V
Video amplitude drop with respect to modulation 0.1 MHz at $T_{amb} = 45\text{ }^{\circ}\text{C}$:						
at 1 MHz	A1	BU4	–1.0	–	+1.0	dB
at 2 MHz	A1	BU4	–1.5	–	+1.5	dB
at 3 MHz	A1	BU4	–2.5	–	+1.5	dB
at 3.58 MHz	A1	BU4	–4.0	–	+2.0	dB
Sound carrier rejection	A1 (1 MHz) + B1	BU4	40	–	–	dB
Residual 47.25 MHz signal in video channel: level of 1.5 MHz	A1 + B3	BU4	–	–	68	dB μ V
Residual 91.5 MHz signal in video channel	A1	BU4	–	–	80	dB μ V
Second IF sound output level at level of 4.5 MHz	A1 + B1	BU5	84	–	–	dB μ V
Test on 2T pulse at $T_{amb} = 45\text{ }^{\circ}\text{C}$:						
2T pulse/bar response	A1	BU4	–2.5	–	+2.5	%
2T pulse response	A1	BU4	–	–	+3.0	%
CVBS S/N (unweighted)	A1 + B1	BU4	41	–	–	dB
Gain limited sensitivity at 1 dB reduction of video output	A1	BU4	–	–	30	dB μ V
Audio characteristics:						
AF output level measured via LP 20 kHz filter, RMS detector, 75 μ s de-emphasis	A1 + B2	BU6	0.25	0.35	0.50	V
THD (Total Harmonic Distortion) measured via LP 20 kHz filter, RMS detector, 75 μ s de-emphasis	A1 + B2	BU6	–	–	0.5	%
S/N measured via CCIR filter, peak CCIR detector, 75 μ s de-emphasis	A1 (full field colour bar) + B1	BU6	41	–	–	dB
AF 3 dB response measured via LP 20 kHz filter, RMS detector, de-emphasis off	A1 (black) + B1	BU6	90	–	–	kHz
AM suppression ratio	A1 + B2	BU6	40	–	–	dB

Digital AFC status

PARAMETER	CONDITIONS	FREQUENCY (kHz)	DIGITAL READ-OUT
ADC word at I ² C-bus during read operation	input voltage at pin 10:		
	0.0 to 0.15V _S	–125	00
	0.15 to 0.30V _S	–62.5	01
	0.30 to 0.45V _S	0	02
	0.45 to 0.60V _S	+62.5	03
	0.60 to 1.00V _S	+125	04

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APPLICATION INFORMATION

A detailed description of the I²C-bus specification, with applications, is given in brochure "The I²C-bus and how to use it". This brochure may be ordered using the code number 9398 393 40011.

WRITE mode

BYTE	BITS								
	7 MSB	6	5	4	3	2	1	0 LSB	A ⁽¹⁾
Address byte	1	1	0	0	0	MA1	MA0	0	A
Program divider byte 1	0	n14	n13	n12	n11	n10	n9	n8	A
Program divider byte 2	n7	n6	n5	n4	n3	n2	n1	n0	A
Control information byte 1	1	CP	T2	T1	T0	RSA	RSB	OS	A
Control information byte 2	P7	P6	P5	P4	P3	P2	P1	P0	A

Note

1. A = Acknowledge.

ADDRESS SELECTION

V_S = +5 V (PLL supply voltage)

MA1	MA0	ADDRESS	VOLTAGE AT PIN 15
0	0	C0	0 to 0.1V _S
0	1	C2	0.2 to 0.3V _S
1	0	C4	0.4 to 0.6V _S
1	1	C6	0.9V _S to V _S

PROGRAMMABLE DIVIDER SETTINGS (BYTES 1 AND 2)

Divider ratio:

$N = 16 \times \{f_{RF(pc)} + f_{IF(pc)}\}$, where (pc) is picture carrier and f_{RF} and f_{IF} are expressed in MHz.

$f_{osc} = N/16$ (MHz).

$N = (8192 \times n13) + (4096 \times n12) + (2048 \times n11) + (1024 \times n10) + (512 \times n9) + (256 \times n8) + (128 \times n7) + (64 \times n6) + (32 \times n5) + (16 \times n4) + (8 \times n3) + (4 \times n2) + (2 \times n1) + n0$

CONTROL BYTE

Charge pump settings:

CP = 1, for fast tuning

CP = 0, for moderate speed tuning with slightly better residual oscillator FM.

Test mode settings:

T2 = T1 = 0; T0 = 1, for normal operation.

PLL disabling:

OS = 0, for normal operation

OS = 1, for switching the charge pump to the high impedance state.

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Ratio select bits

RSA	RSB	STEP SIZE
X	0	50 kHz
0	1	31.25 kHz (for slow picture search)
1	1	62.5 kHz (for normal picture search)

PORTS BYTE

Band switching

BAND	BIT ⁽¹⁾							
	P0	P1	P2	P3 ⁽²⁾	P4	P5	P6	P7
Low band	0	0	0	X	0	1	0	1
Mid band	0	0	0	X	1	0	0	1
High band	0	0	0	X	1	1	0	0

Notes

1. X = don't care; P0 to P7 are output ports on the PLL device.
2. P3 is a system switch output for customer applications.

TELEGRAM EXAMPLES (WRITE MODE)

Start - Adb - Ack - Db1 - Ack - Db2 - Ack - Cb - Ack - Pb - Ack - Stop.

Start - Adb - Ack - Cb - Ack - Pb - Ack - Db1 - Ack - Db2 - Ack - Stop.

Start - Adb - Ack - Db1 - Ack - Db2 - Ack - Cb - Ack - Stop.

Start - Adb - Ack - Db1 - Ack - Db2 - Ack - Stop.

Where:

Start = start condition

Adb = address byte

Ack = acknowledge

Db1 = divider byte 1

Db2 = divider byte 2

Cb = control byte

Pb = ports byte

Stop = stop condition.

Remark: for channel selection involving band switching, and to ensure smooth tuning to the desired channel without causing unnecessary charge pump action, it is recommended to consider the difference between wanted channel frequency (f_w) and the current channel frequency (f_c):

- If $f_w > f_c$, use telegram as:
Start - Adb - Ack - Db1 - Ack - Db2 - Ack - Cb - Ack - Pb - Ack - Stop
- If $f_w < f_c$, use telegram as:
Start - Adb - Ack - Cb - Ack - Pb - Ack - Db1 - Ack - Db2 - Ack - Stop.

Unnecessary charge pump action will result in very low tuning voltage ($V_T \approx 0$ V) which may drive the oscillator to extreme conditions.

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READ mode

The in-lock can be read by setting the R/W bit to 1.

BYTE	BITS								
	7 MSB	6	5	4	3	2	1	0 LSB	A ⁽⁵⁾
Address byte	1	1	0	0	0	MA1	MA0	1	A
Status byte	POR ⁽¹⁾	FL ⁽²⁾	I2 ⁽³⁾	I1 ⁽³⁾	I0 ⁽³⁾	A2 ⁽⁴⁾	A1 ⁽⁴⁾	A0 ⁽⁴⁾	A

Notes

1. POR = Power On Reset. POR is internally set to 1 in case V_S drops below 3 V. The POR bit is reset when an end of data is detected by the PLL IC.
2. FL = In-lock flag; FL = 1: loop is phase-locked. The loop must be phase-locked during at least 8 periods of the internal 7.8125 kHz reference frequency before the FL flag is internally set to 1.
3. I2, I1 and I0 = digital information for I/O ports P2, P1 and P0 respectively.
4. A2, A1 and A0 = built-in 5-level A/D converter on I/O port P6. AFC information to the controller of the IF section is available on pin 10 (see Table "Digital AFC status").
5. A = Acknowledge.

TELEGRAM EXAMPLES (READ MODE)

Start - Adb - Ack - STB - Ack - STB - - Stop (no Ack from processor = End-of-data).

Start - Adb - Ack - STB - - Stop (no Ack from processor = End-of-data).

Where:

STB = Status byte.

Video buffer

A video buffer is built into the video module to enable the unit to drive a 75 Ω load directly. In case it is required to use the F11236MK2 as a replacement for the F11236 in the same videocard, it is necessary to replace the 75 Ω series resistor in the video card by a 0 Ω series resistor. At the same time the 22 kΩ series resistor in the tuning supply must be removed.

I²C-bus load

The F11236MK2 contains a series resistor (R = 100 Ω) in the SCL and SDA lines. Both lines also have a capacitive load of typical 56 pF (see Fig.3).

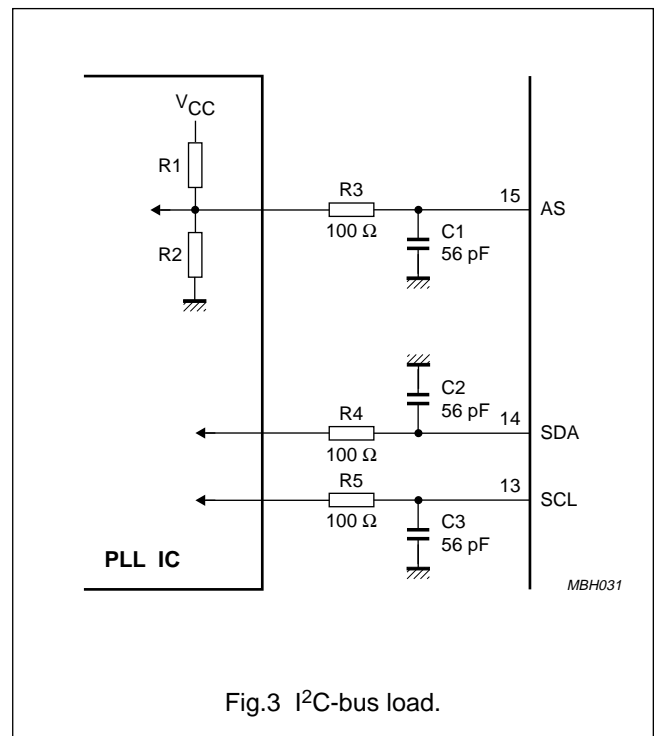
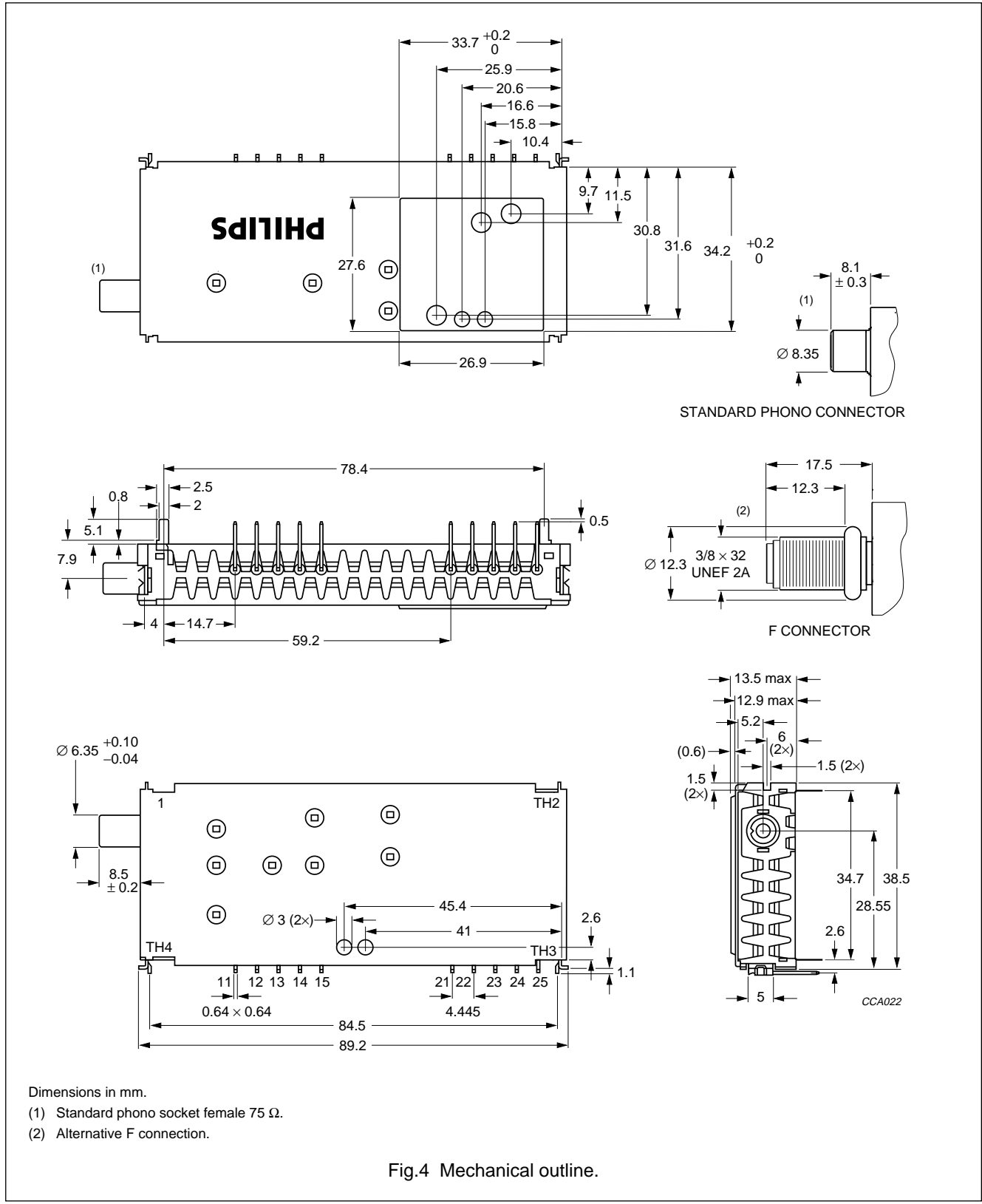


Fig.3 I²C-bus load.

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MECHANICAL DATA



Dimensions in mm.

- (1) Standard phono socket female 75 Ω .
- (2) Alternative F connection.

Fig.4 Mechanical outline.

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Aerial connections

Standard-phono socket female 75 Ω or F (female).

Solderability

The solderability of pins and mounting tags when tested initially and after 16 hours steam ageing in accordance with "IEC 68-2-20", test Ta, method 1 (solder bath 235 °C for 2 s), results in a wetted area of 95%. No de-wetting will occur when soldered at 260 °C for 5 s.

Resistance to soldering heat

The product will not be damaged when tested in accordance with "IEC 68-2-20", test Tb, method 1A (solder bath 260 °C for 10 ± 1 s).

Mass

Approximately 50 g.

Robustness of pins

The pins will not be damaged when tested in accordance with "IEC 68-2-21":

- Test Ua1, tensile of 10 N in axial direction
- Test Ua2, thrust of 4 N in axial direction.

Punching pattern of chassis PCB

Field rejects are often related to broken tag joints. Therefore, the following punching pattern is recommended (see Fig.5).

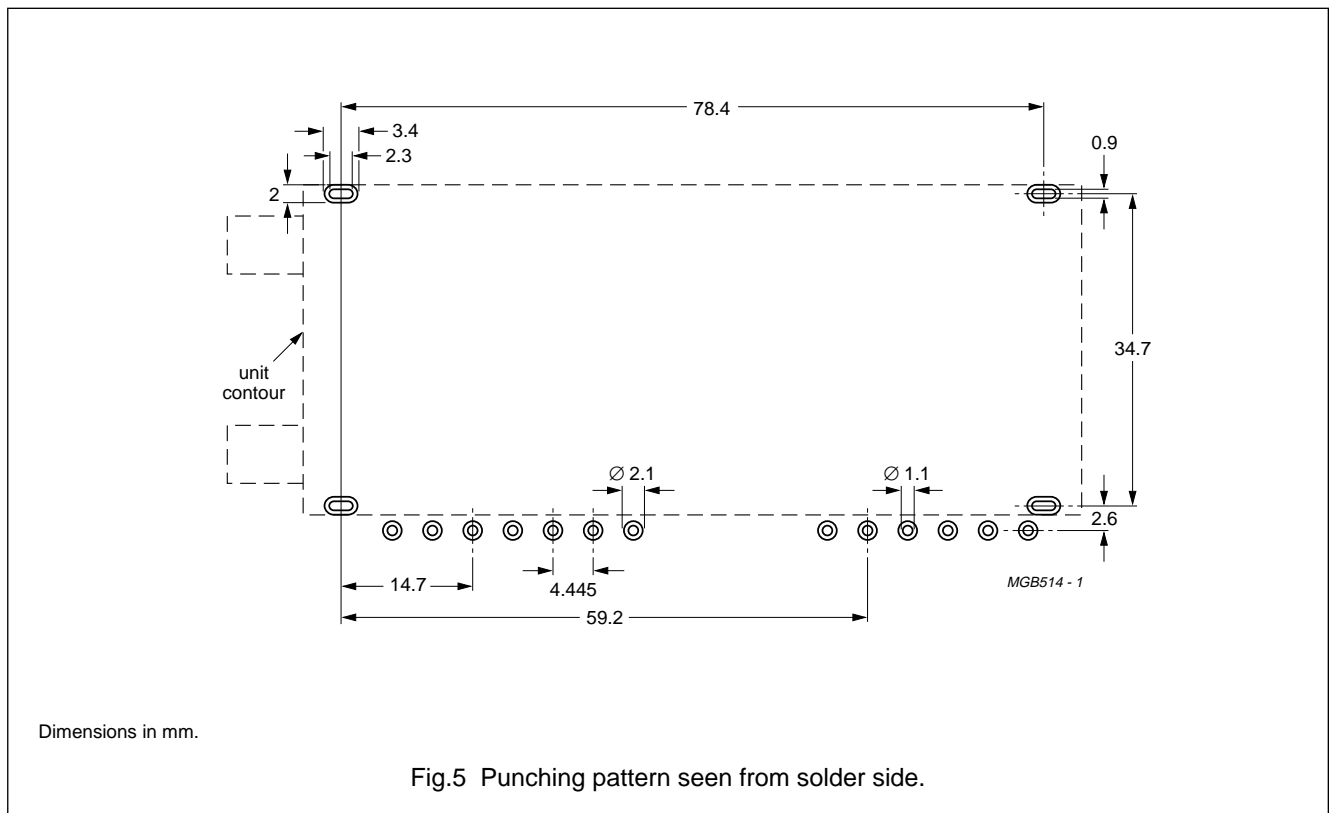


Fig.5 Punching pattern seen from solder side.

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

PURCHASE OF PHILIPS I²C COMPONENTS



Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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NOTES

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NOTES

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