DATA SHEET

74F841/842
Bus interface latches

Product data

2004 Jan 23

Replaces datasheet 74F841/842/843/845/846 of 1999 Jun 23

Philips
Semiconductors

PHILIPS

10-bit bus interface latches, non-inverting/inverting (3-State) 74F841/74F842

FEATURES

- High speed parallel latches
- Extra data width for wide address/data paths or buses carrying parity
- High impedance NPN base input structure minimizes bus loading
- I_{IL} is 20 μA for minimum bus loading
- Buffered control inputs to reduce AC effects
- Ideal where high speed, light loading, or increased fan-in are required as with MOS microprocessors
- Positive and negative over-shoots are clamped to ground
- 3-State outputs glitch free during power-up and power-down
- 48 mA sink current
- Slim dual in-line 300 mil package
- Broadside pinout

DESCRIPTION

The 74F841 and 74F842 bus interface latches are designed to provide extra data width for wider address/data paths of buses carrying parity.

The 74F841 consists of ten D-type latches with 3-State outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition. On the LE HIGH-to-LOW transition, the data that meets the set-up and hold time is latched.

Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the output is in the high-impedance state.

The 74F842 is the inverted output version of the 74F841.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F841, 74F842	5.5 ns	60 mA

ORDERING INFORMATION

COMMERCIAL RANGE: V_{CC} = 5 V ± 10%; T_{amb} = 0 °C to +70 °C

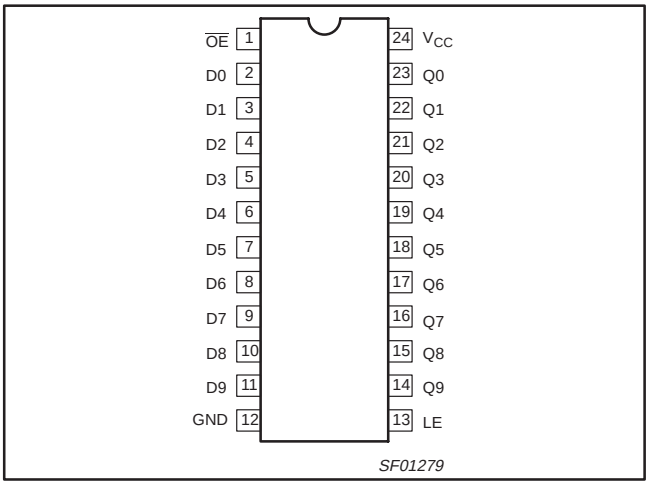
Type number	Package		
	Name	Description	Version
N74F841N, N74F842N	DIP24	plastic dual in-line package; 24 leads (300 mil)	SOT222-1
N74F841D, N74F842D	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

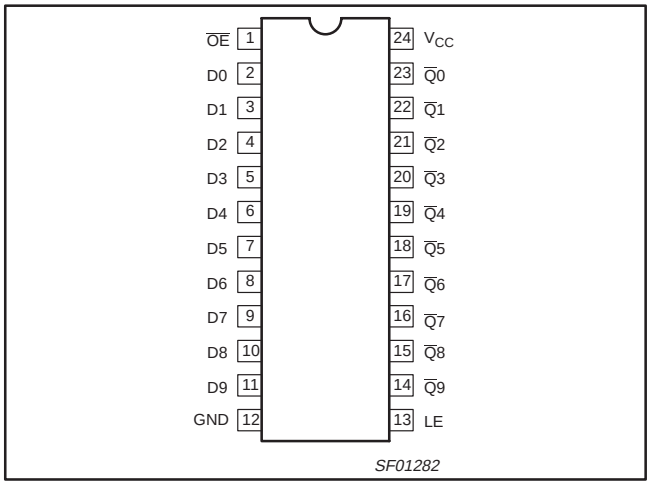
PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Dn	Data inputs	1.0/0.033	20 μA / 20 μA
LE	Latch Enable input	1.0/0.033	20 μA / 20 μA
$\overline{OE}$	Output Enable input (active-LOW)	1.0/0.033	20 μA / 20 μA
Qn	Data outputs	1200/80	24 mA / 48 mA
$\overline{Q}$n	Data outputs	1200/80	24 mA / 48 mA

NOTE: One (1.0) FAST Unit Load is defined as: 20 μA in the HIGH state and 0.6 mA in the LOW state.

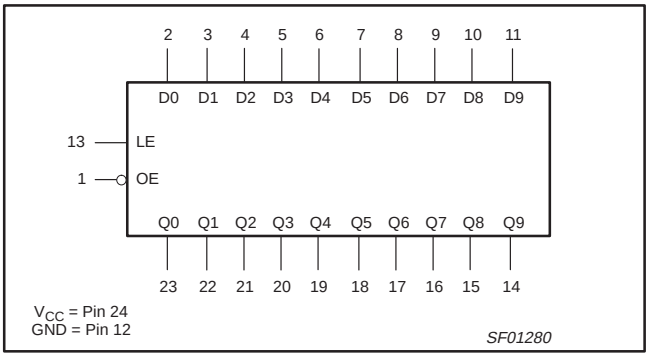
PIN CONFIGURATION for 74F841



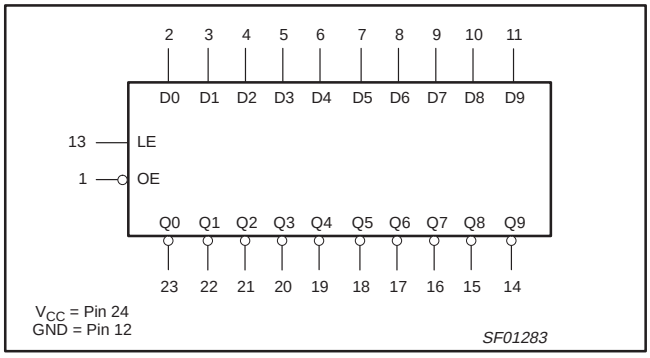
PIN CONFIGURATION for 74F842



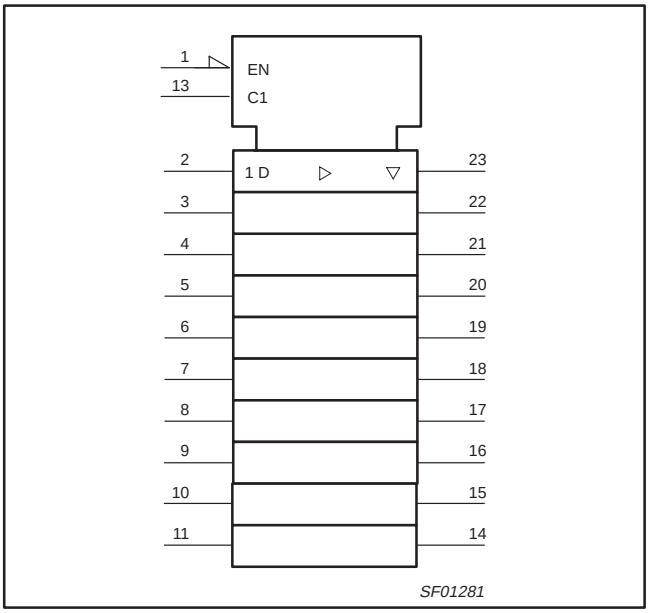
LOGIC SYMBOL for 74F841



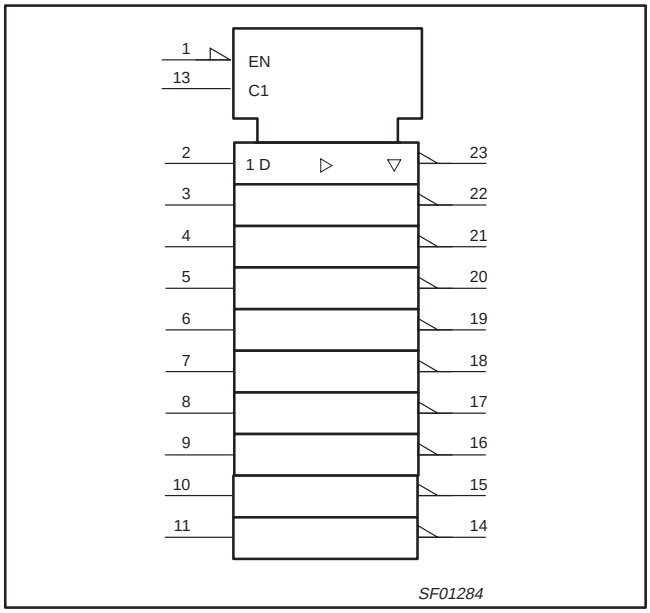
LOGIC SYMBOL for 74F842



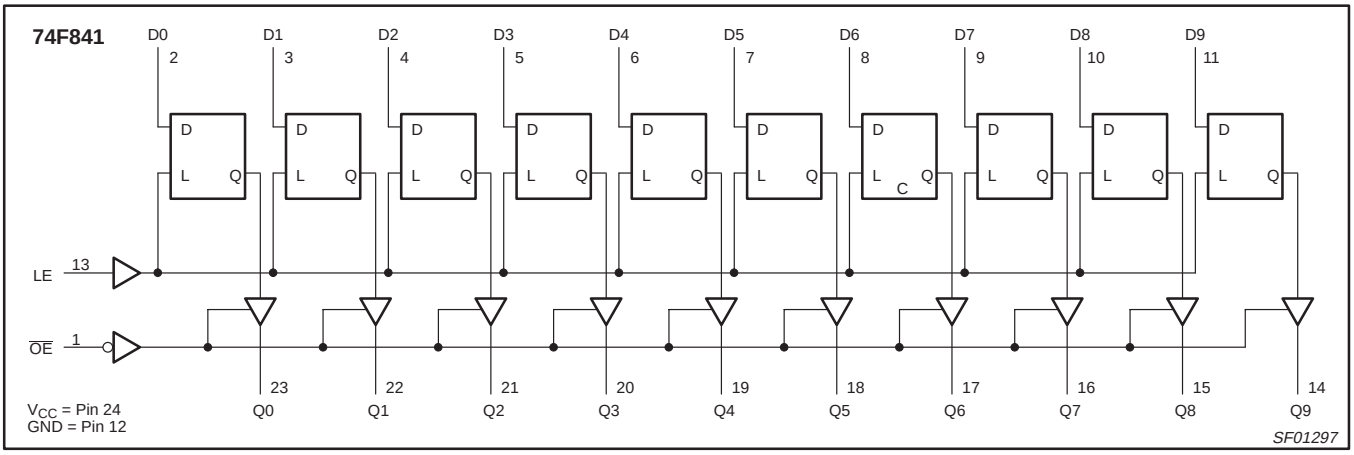
LOGIC SYMBOL (IEEE/IEC) for 74F841



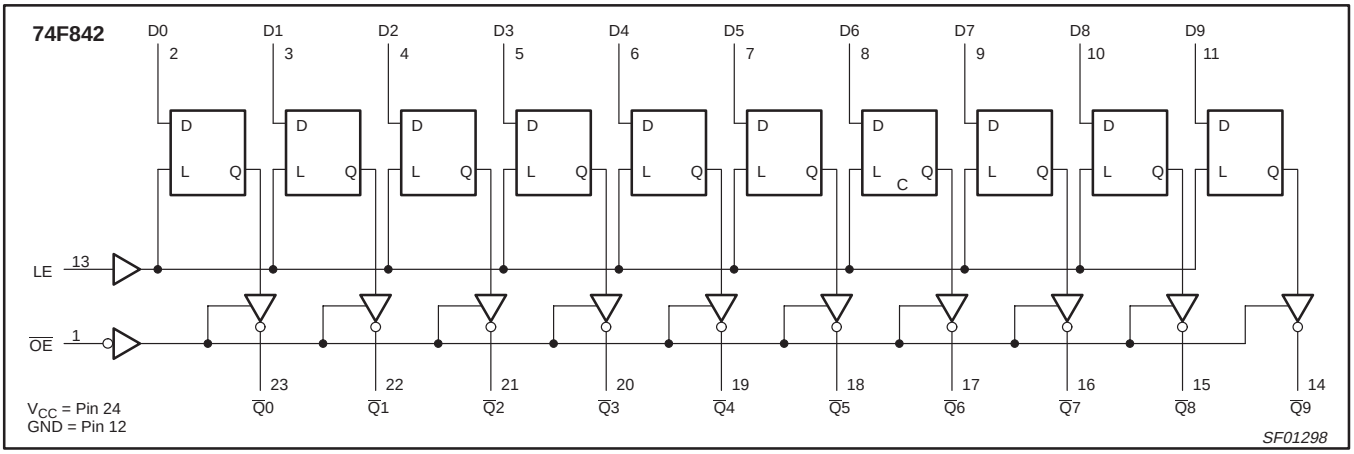
LOGIC SYMBOL (IEEE/IEC) for 74F842



LOGIC DIAGRAM for 74F841



LOGIC DIAGRAM for 74F842



FUNCTION TABLE for 74F841 and 74F842

INPUTS			OUTPUTS		OPERATING MODE
			74F841	74F842	
$\overline{OE}$	LE	Dn	Qn	$\overline{Q}$n	
L	H	L	L	H	Transparent
L	H	H	H	L	
L	↓	l	L	H	Latched
L	↓	h	H	L	
H	X	X	Z	Z	High Impedance
L	L	X	NC	NC	Hold

H = HIGH voltage level
L = LOW voltage level
h = HIGH state one set-up time before the HIGH-to-LOW LE transition
l = LOW state one set-up time before the HIGH-to-LOW LE transition
↓ = HIGH-to-LOW transition
X = Don't care
NC= No change
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS

Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	supply voltage	–0.5 to +7.0	V
V_{IN}	input voltage	–0.5 to +7.0	V
I_{IN}	input current	–30 to +5	mA
V_{OUT}	voltage applied to output in HIGH output state	–0.5 to V_{CC}	V
I_{OUT}	current applied to output in LOW output state	84	mA
T_{amb}	operating free-air temperature range	0 to +70	°C
T_{stg}	storage temperature range	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	supply voltage	4.5	5.0	5.5	V
V_{IH}	HIGH-level input voltage	2.0	–	–	V
V_{IL}	LOW-level input voltage	–	–	0.8	V
I_{IK}	input clamp current	–	–	–18	mA
I_{OH}	HIGH-level output current	–	–	–24	mA
I_{OL}	LOW-level output current	–	–	48	mA
T_{amb}	operating free-air temperature range	0	–	+70	°C

DC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS[1]			LIMITS			UNIT
					MIN	TYP[2]	MAX	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN; V_{IL} = MAX; V_{IH} = MIN	I_{OH} = –15 mA	± 10%V_{CC}	2.2	–	–	V
				± 5%V_{CC}	2.2	3.3	–	V
			I_{OH} = –24 mA	± 10%V_{CC}	2.0	–	–	V
				± 5%V_{CC}	2.0	–	–	V
V_{OL}	LOW-level output voltage	V_{CC} = MIN; V_{IL} = MAX; V_{IH} = MIN	I_{OL} = 32 mA	± 10%V_{CC}	–	0.38	0.55	V
			I_{OL} = 48 mA	± 5%V_{CC}	–	0.38	0.55	V
V_{IK}	Input clamp voltage	V_{CC} = MIN; I_I = I_{IK}			–	–0.73	–1.2	V
I_I	Input current at maximum input voltage	V_{CC} = 0 V; V_I = 7.0 V			–	–	100	µA
I_{IH}	HIGH-level input current	V_{CC} = MAX; V_I = 2.7 V			–	–	20	µA
I_{IL}	LOW-level input current	V_{CC} = MAX; V_I = 0.5 V			–	–	–20	µA
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX; V_O = 2.7 V			–	–	50	µA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX; V_O = 0.5 V			–	–	–50	µA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			–100	–	–225	mA
I_{CC}	Supply current (total)	74F841	I_{CCH}	V_{CC} = MAX	–	50	65	mA
			I_{CCL}		–	60	80	mA
			I_{CCZ}		–	70	92	mA
		74F842	I_{CCH}	V_{CC} = MAX	–	40	60	mA
			I_{CCL}		–	65	90	mA
			I_{CCZ}		–	60	90	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5 V, T_{amb} = 25 °C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I_{OS} tests should be performed last.

AC ELECTRICAL CHARACTERISTICS for 74F841/74F842

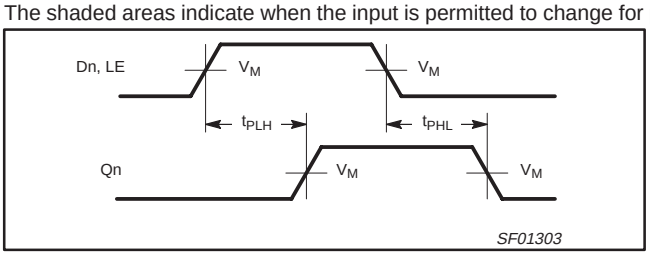
SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_{amb} = +25 °C V_{CC} = +5.0 V C_L = 50 pF; R_L = 500 Ω			T_{amb} = 0 °C to +70 °C V_{CC} = +5.0 V ± 10% C_L = 50 pF; R_L = 500 Ω		
				MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	74F841	Waveform 1, 2	2.0 2.5	4.0 4.5	7.5 7.5	2.0 2.5	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay LE to Qn		Waveform 1, 2	4.5 4.0	6.5 6.0	9.5 9.0	4.0 3.5	10.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay Dn to $\overline{Q}$n	74F842	Waveform 1, 2	3.5 3.0	5.5 5.0	8.5 8.0	4.5 4.0	9.0 8.5	ns
t_{PLH} t_{PHL}	Propagation delay LE to $\overline{Q}$n		Waveform 1, 2	5.0 4.5	7.0 6.5	10.0 9.0	3.0 3.0	10.5 9.5	ns
t_{PZH} t_{PZL}	Output enable time HIGH or LOW-level $\overline{OE}$ to Qn or $\overline{Q}$n		Waveform 4 Waveform 5	2.5 4.0	4.5 6.0	8.0 9.5	2.0 3.0	8.5 10.5	ns
t_{PHZ} t_{PLZ}	Output disable time HIGH or LOW-level $\overline{OE}$ to Qn or $\overline{Q}$n		Waveform 4 Waveform 5	1.0 1.0	4.5 5.0	8.0 8.0	1.0 1.0	8.5 8.5	ns

AC SET-UP REQUIREMENTS for 74F841/74F842

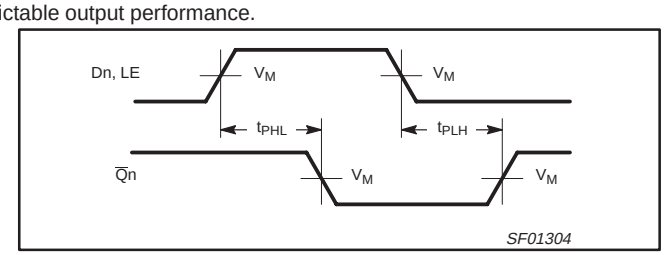
SYMBOL	PARAMETER		TEST CONDITION	LIMITS				UNIT
				T_{amb} = +25 °C V_{CC} = +5.0 V C_L = 50 pF; R_L = 500 Ω		T_{amb} = 0 °C to +70 °C V_{CC} = +5.0 V ± 10% C_L = 50 pF; R_L = 500 Ω		
				MIN	TYP	MIN	MAX	
t_s(H) t_s(L)	Set-up time, HIGH or LOW Dn to LE		Waveform 3	0.0 0.0	– –	1.0 1.0	– –	ns
t_h(H) t_h(L)	Hold time, HIGH or LOW Dn to LE	74F841	Waveform 3	2.5 3.0	– –	3.0 4.0	– –	ns
t_w(H)	LE pulse width, HIGH		Waveform 3	3.5	–	4.0	–	ns
t_h(H) t_h(L)	Hold time, HIGH or LOW Dn to LE	74F842	Waveform 3	3.0 3.5	– –	3.5 4.5	– –	ns
t_w(H)	LE pulse width, HIGH		Waveform 3	3.0	–	3.0	–	ns

AC WAVEFORMS

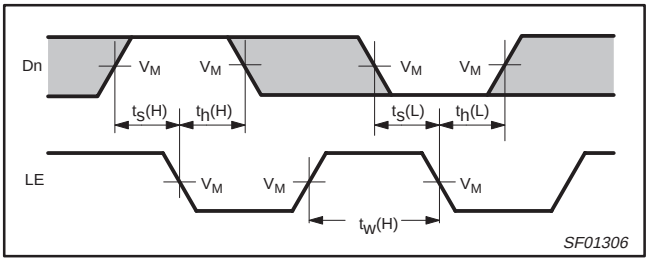
For all waveforms, V_M = 1.5 V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



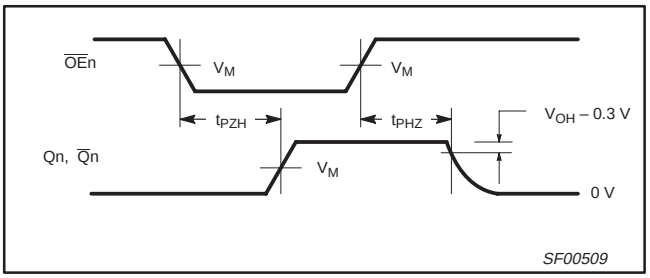
Waveform 1. Propagation delay, non-inverting path



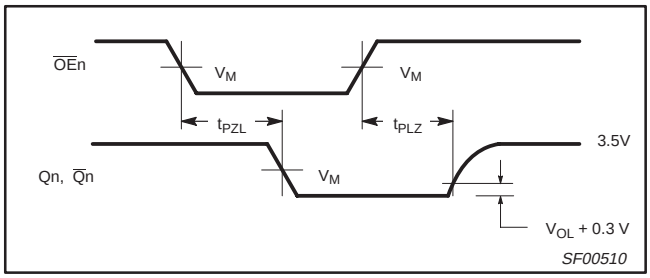
Waveform 2. Propagation delay, inverting path



Waveform 3. Data set-up and hold times

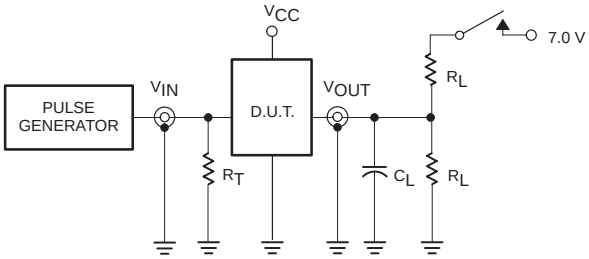


Waveform 4. 3-State Output Enable time to HIGH level and Output Disable time from HIGH level

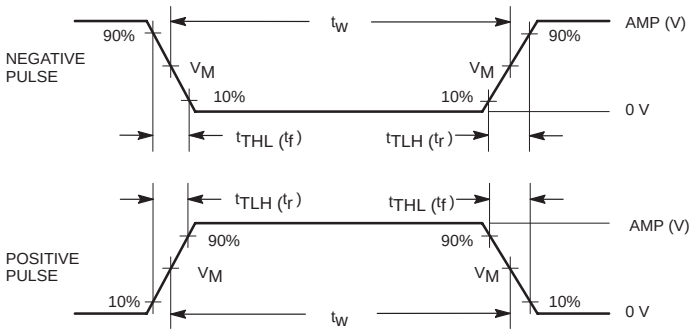


Waveform 5. 3-State Output Enable time to LOW level and Output Disable time from LOW level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

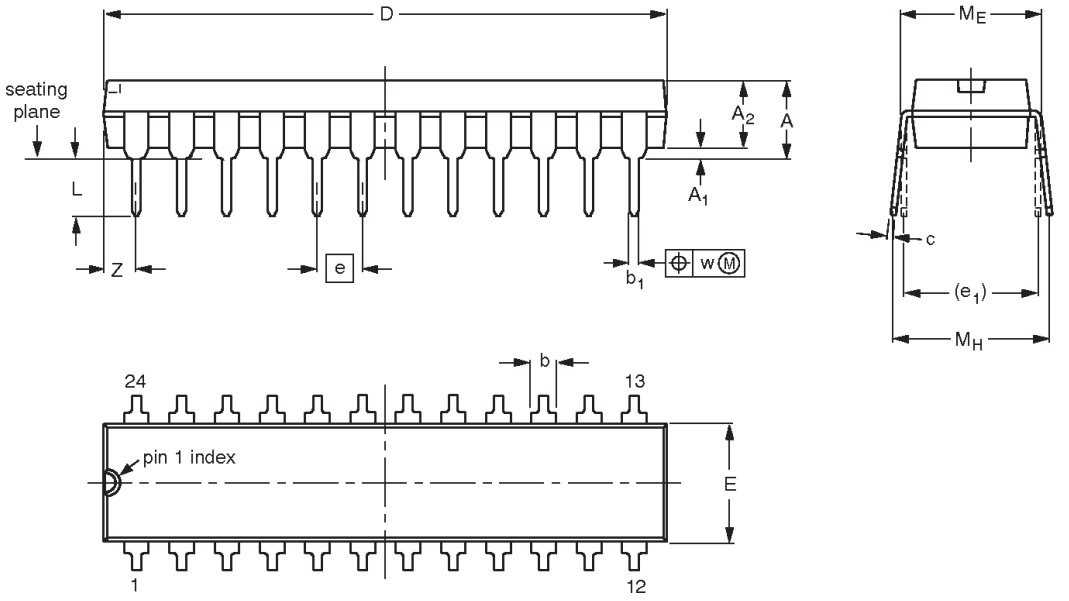
C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

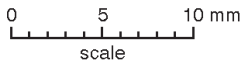
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0 V	1.5 V	1 MHz	500 ns	2.5 ns	2.5 ns

SF00777

DIP24: plastic dual in-line package; 24 leads (300 mil) **SOT222-1**





DIMENSIONS (mm dimensions are derived from the original inch dimensions)

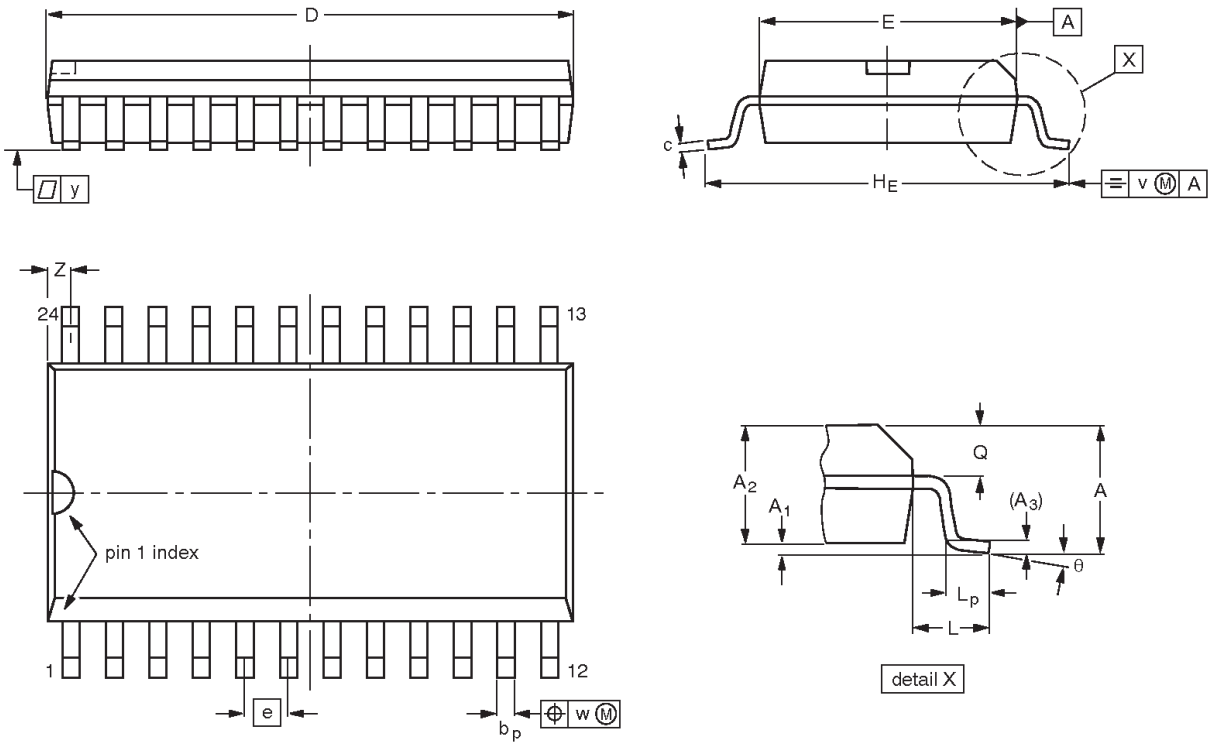
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.7	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.25	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.246	0.1	0.3	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT222-1		MS-001				~~99-12-27~~ 03-03-12

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

10-bit bus interface latches, non-inverting/inverting (3-State) 74F841/74F842

REVISION HISTORY

Rev	Date	Description
_4	20040123	**Product data (9397 750 12746). ECN 853-1208 A15379 of 22 January 2004. Replaces Product specification 74F841/842/843/845/846_3 dated 1999 Jun 23 (9397 750 06143).** Modifications: • Delete all references to 74F843, 74F845, 74F846 (products discontinued).
_3	19990623	**Product specification (9397 750 06143). ECN 853-1208 21851 of 23 June 1999. Replaces datasheet 74F841/842/843/844/845/846 of 1999 Jan 08.**

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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