

# DATA SHEET

## **BST120**

P-channel enhancement mode  
vertical D-MOS transistor

Product specification  
File under Discrete Semiconductors, SC13b

April 1995

# P-channel enhancement mode vertical D-MOS transistor

# BST120

DESCRIPTION

P-channel vertical D-MOS transistor in SOT89 envelope and intended for use in relay, high-speed and line-transformer drivers, using SMD technology.

FEATURES

- Very low  $R_{DS(on)}$
- Direct interface to C-MOS
- High-speed switching
- No second breakdown

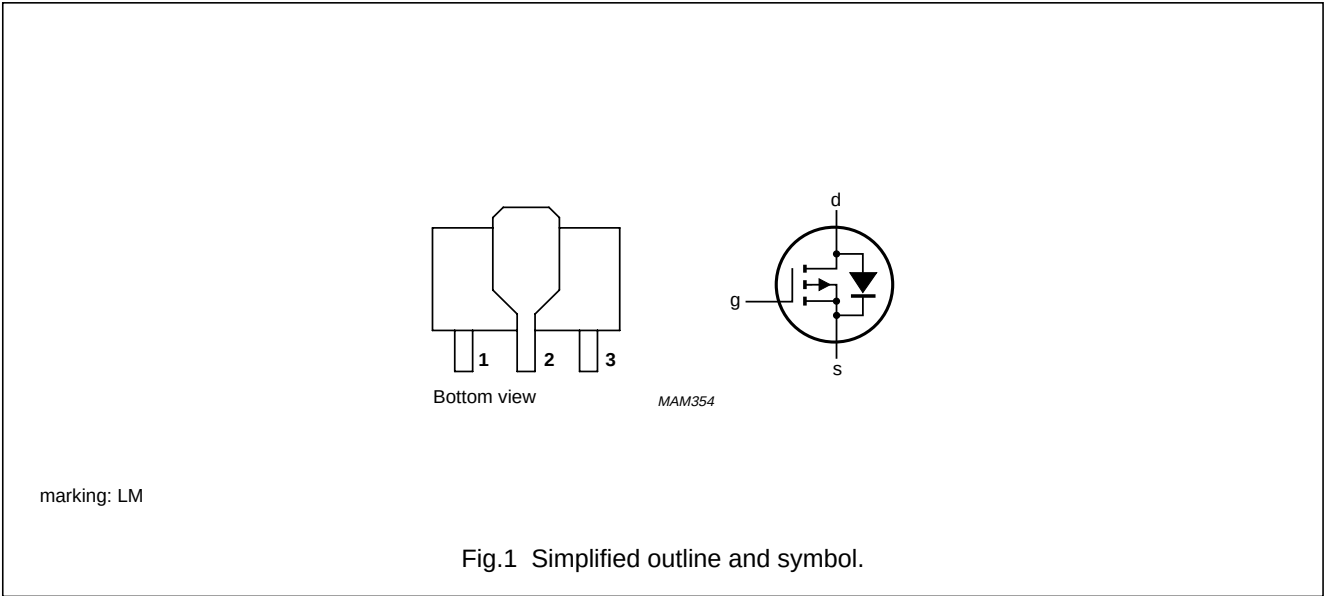
QUICK REFERENCE DATA

|                                                                      |               |      |              |
|----------------------------------------------------------------------|---------------|------|--------------|
| Drain-source voltage                                                 | $-V_{DS}$     | max. | 60 V         |
| Gate-source voltage (open drain)                                     | $\pm V_{GSO}$ | max. | 20 V         |
| Drain current (DC)                                                   | $-I_D$        | max. | 0,3 A        |
| Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$ | $P_{tot}$     | max. | 1 W          |
| Drain-source ON-resistance                                           | $R_{DS(on)}$  | typ. | 4,5 $\Omega$ |
| $-I_D = 200\text{ mA}; -V_{GS} = 10\text{ V}$                        |               | max. | 6 $\Omega$   |
| Transfer admittance                                                  | $ Y_{fs} $    | typ. | 200 mS       |
| $-I_D = 200\text{ mA}; -V_{DS} = 15\text{ V}$                        |               |      |              |

PINNING - SOT89

- 1 = source
- 2 = drain
- 3 = gate

PIN CONFIGURATION



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**BST120****RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

|                                                                               |               |      |                                         |
|-------------------------------------------------------------------------------|---------------|------|-----------------------------------------|
| Drain-source voltage                                                          | $-V_{DS}$     | max. | 60 V                                    |
| Gate-source voltage (open drain)                                              | $\pm V_{GSO}$ | max. | 20 V                                    |
| Drain current (DC)                                                            | $-I_D$        | max. | 0.3 A                                   |
| Drain current (peak)                                                          | $-I_{DM}$     | max. | 0.8 A                                   |
| Total power dissipation up to $T_{amb} = 25\text{ }^{\circ}\text{C}$ (note 1) | $P_{tot}$     | max. | 1 W                                     |
| Storage temperature range                                                     | $T_{stg}$     |      | $-65$ to $+150\text{ }^{\circ}\text{C}$ |
| Junction temperature                                                          | $T_j$         | max. | $150\text{ }^{\circ}\text{C}$           |

**THERMAL RESISTANCE**

|                                   |               |   |         |
|-----------------------------------|---------------|---|---------|
| From junction to ambient (note 1) | $R_{th\ j-a}$ | = | 125 K/W |
|-----------------------------------|---------------|---|---------|

**Note**

1. Transistor mounted on ceramic substrate: area =  $2,5\text{ cm}^2$  and thickness = 0,7 mm.

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### CHARACTERISTICS

$T_j = 25\text{ }^{\circ}\text{C}$  unless otherwise specified

Drain-source breakdown voltage

$$-I_D = 10\text{ }\mu\text{A}; V_{GS} = 0$$

$$-V_{(BR)DSS} \quad \text{min.} \quad 60\text{ V}$$

Drain-source leakage current

$$-V_{DS} = 48\text{ V}; V_{GS} = 0$$

$$-I_{DSS} \quad \text{max.} \quad 1\text{ }\mu\text{A}$$

Gate-source leakage current

$$-V_{GS} = 20\text{ V}; V_{DS} = 0$$

$$-I_{GSS} \quad \text{max.} \quad 100\text{ nA}$$

Gate threshold voltage

$$-I_D = 1\text{ mA}; V_{DS} = V_{GS}$$

$$-V_{GS(th)} \quad \begin{array}{l} \text{min.} \\ \text{max.} \end{array} \quad \begin{array}{l} 1.5\text{ V} \\ 3.5\text{ V} \end{array}$$

Drain-source ON-resistance

$$-I_D = 200\text{ mA}; -V_{GS} = 10\text{ V}$$

$$R_{DS(on)} \quad \begin{array}{l} \text{typ.} \\ \text{max.} \end{array} \quad \begin{array}{l} 4.5\text{ }\Omega \\ 6\text{ }\Omega \end{array}$$

Transfer admittance

$$-I_D = 200\text{ mA}; -V_{DS} = 15\text{ V}$$

$$|Y_{fs}| \quad \text{typ.} \quad 200\text{ mS}$$

Input capacitance at  $f = 1\text{ MHz}$

$$-V_{DS} = 10\text{ V}; V_{GS} = 0$$

$$C_{iss} \quad \begin{array}{l} \text{typ.} \\ \text{max.} \end{array} \quad \begin{array}{l} 55\text{ pF} \\ 70\text{ pF} \end{array}$$

Output capacitance at  $f = 1\text{ MHz}$

$$-V_{DS} = 10\text{ V}; V_{GS} = 0$$

$$C_{oss} \quad \begin{array}{l} \text{typ.} \\ \text{max.} \end{array} \quad \begin{array}{l} 30\text{ pF} \\ 45\text{ pF} \end{array}$$

Feedback capacitance at  $f = 1\text{ MHz}$

$$-V_{DS} = 10\text{ V}; V_{GS} = 0$$

$$C_{rss} \quad \begin{array}{l} \text{typ.} \\ \text{max.} \end{array} \quad \begin{array}{l} 8\text{ pF} \\ 12\text{ pF} \end{array}$$

Switching times (see Figs 2 and 3)

$$-I_D = 200\text{ mA}; -V_{DD} = 50\text{ V}; -V_{GS} = 0\text{ to }10\text{ V}$$

$$\begin{array}{l} t_{on} \\ t_{off} \end{array} \quad \begin{array}{l} \text{typ.} \\ \text{typ.} \end{array} \quad \begin{array}{l} 4\text{ ns} \\ 20\text{ ns} \end{array}$$

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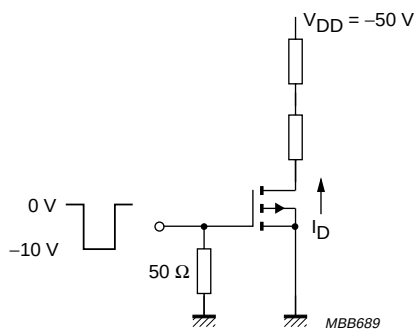


Fig.2 Switching times test circuit.

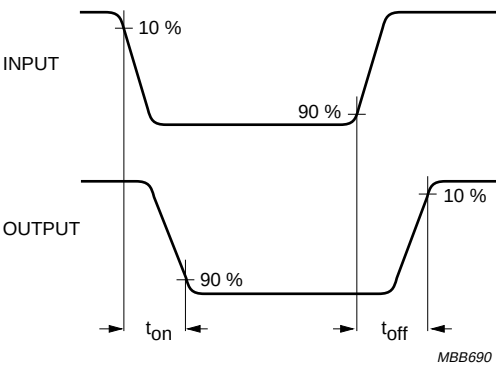


Fig.3 Input and output waveforms.

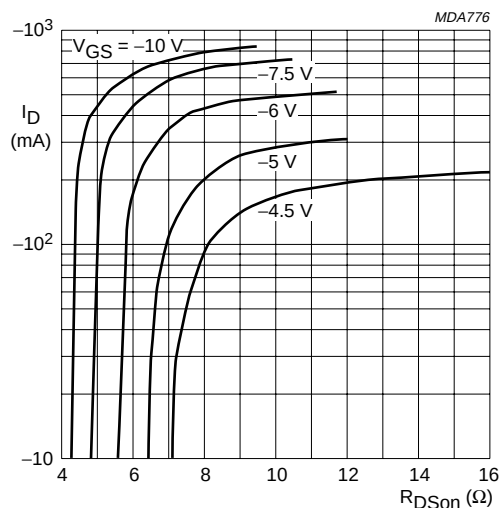


Fig.4 Drain current vs ON-resistance;  
 $T_j = 25\text{ }^{\circ}\text{C}$ ; typical values.

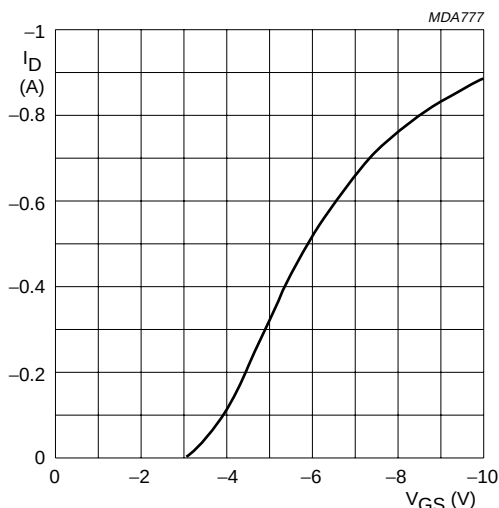


Fig.5 Transfer characteristics;  $T_j = 25\text{ }^{\circ}\text{C}$ ;  
 $-V_{DS} = 10\text{ V}$ ; typical values.

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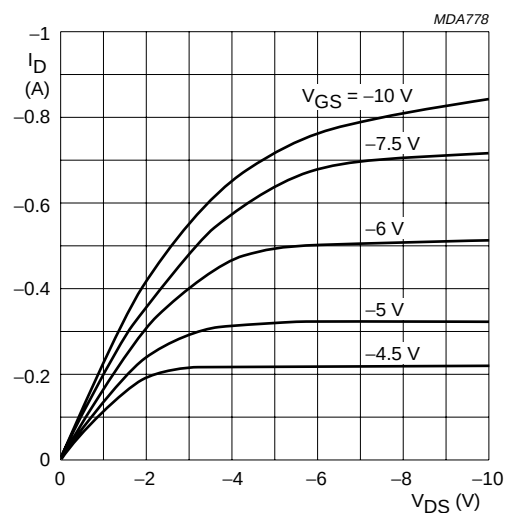


Fig.6 Output characteristics;  $T_j = 25\text{ }^{\circ}\text{C}$ ;  
typical values.

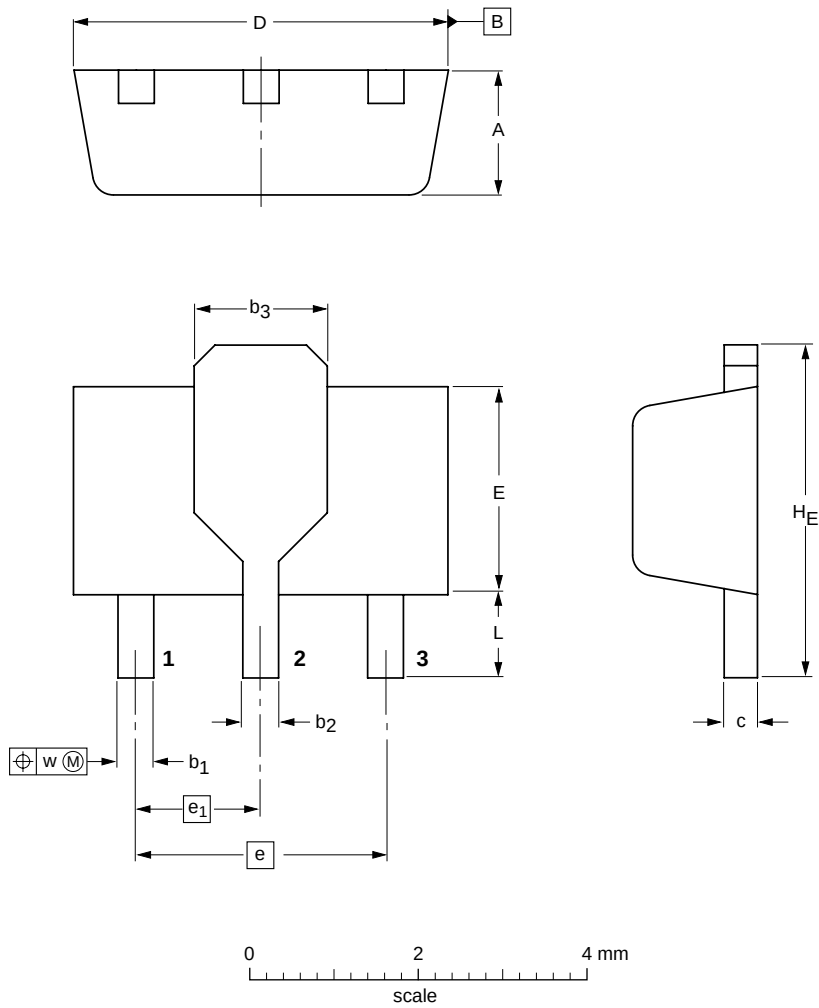
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PACKAGE OUTLINES

Plastic surface mounted package; collector pad for good heat transfer; 3 leads

SOT89



DIMENSIONS (mm are the original dimensions)

| UNIT | A          | b <sub>1</sub> | b <sub>2</sub> | b <sub>3</sub> | c            | D          | E          | e   | e <sub>1</sub> | H <sub>E</sub> | L<br>min. | w    |
|------|------------|----------------|----------------|----------------|--------------|------------|------------|-----|----------------|----------------|-----------|------|
| mm   | 1.6<br>1.4 | 0.48<br>0.35   | 0.53<br>0.40   | 1.8<br>1.4     | 0.44<br>0.37 | 4.6<br>4.4 | 2.6<br>2.4 | 3.0 | 1.5            | 4.25<br>3.75   | 0.8       | 0.13 |

| OUTLINE<br>VERSION | REFERENCES |       |      |  | EUROPEAN<br>PROJECTION                                                                | ISSUE DATE |
|--------------------|------------|-------|------|--|---------------------------------------------------------------------------------------|------------|
|                    | IEC        | JEDEC | EIAJ |  |                                                                                       |            |
| SOT89              |            |       |      |  |  | 97-02-28   |

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**BST120****DEFINITIONS**

| <b>Data sheet status</b>                                                                            |                                                                                       |
|-----------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|
| Objective specification                                                                             | This data sheet contains target or goal specifications for product development.       |
| Preliminary specification                                                                           | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification                                                                               | This data sheet contains final product specifications.                                |
| <b>Application information</b>                                                                      |                                                                                       |
| Where application information is given, it is advisory and does not form part of the specification. |                                                                                       |

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**NOTES**

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**NOTES**

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Printed in The Netherlands

137107/00/01/pp12

Date of release: April 1995

Document order number: 9397 750 02494

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