

NTLMS4502N

Advance Information

Power MOSFET

17 A, 24 V N-Channel SO-8 Leadless

The SO-8LL (Leadless) package uses the power QFN package technology. It's footprint matches that of the standard SO-8 single die device. This Leadless SO-8 package provides low parasitic inductance compared to the standard SO-8 package allowing for higher frequency operation.

Features

- Planar HD3E Process for Fast Switching Performance
- Low $R_{DS(on)}$ to Minimize Conduction Loss
- Low C_{iss} to Minimize Driver Loss
- Low Gate Charge
- Surface Mount
- Fast Switching

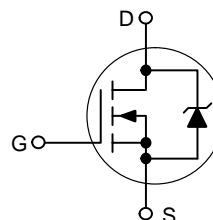
Product Summary

Symbol	Value
V_{DS}	24 V
$R_{DS(on)}$ @ 10 V	8 m Ω
Q_g	8 nC
I_D	17 A
Q_{gd}	3 nC

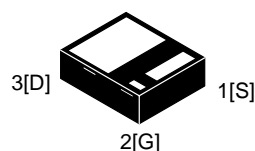


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MARKING DIAGRAM



SO-8 Leadless
CASE 751S

xxxxx = Specific Device Code
Y = Year
WW = Work Week

PIN ASSIGNMENT

PIN	FUNCTION
1	S – SOURCE
2	G – GATE
3	D – DRAIN

ORDERING INFORMATION

Device	Package	Shipping
NTLMS4502N	SO-8 Leadless	2500 Tape & Reel

This document contains information on a new product. Specifications and information herein are subject to change without notice.

NTLMS4502N

MAXIMUM RATINGS (T_J = 25°C Unless otherwise specified)

Parameter	Symbol	Value	Units
Drain-to-Source Voltage	V _{DSS}	24	V _{dc}
Gate-to-Source Voltage Continuous	V _{GS}	±20	V _{dc}
Drain Current Continuous @ T _A = 25°C (Note 1)	I _D	12	A
Continuous @ T _A = 25°C (Note 2)	I _{DM}	17	A
Single Pulse (t _p = 10 μs) (Note 4)	I _{DM}	40	A
Maximum Power Dissipation (Steady State) @ T _A = 25°C (Note 1)	P _D	2.3	W
Single Pulse (t _p = 10 Secs) T _A = 25°C (Note 2)	P _D	5.0	W
Operating and Storage Temperature	T _J and T _{stg}	–55 to 150	°C
Single Pulse Drain-to Source Avalanche Energy – Starting T _J = 25°C	E _{AS}	220	mJ
Thermal Resistance Junction-to-Ambient (Note 1)	R _{θJA}	55	°C/W
Junction-to-Ambient (Note 2)	R _{θJA}	25	
Junction-to-Ambient (Note 3)	R _{θJA}	110	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 Secs	T _L	260	°C

1. When surface mounted to an FR4 board using 1" pad size, (Cu Area 1.127 in²).
2. 1" pad (Cu Area 0.911 in²), t < 10 sec.
3. When surface mounted to an FR4 board using minimum recommended pad size, (Cu Area 0.412 in²).
4. Chip current capability limited by package.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless otherwise specified)

Characteristics	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 5) (V _{GS} = 0 V _{dc} , I _D = 250 μA _{dc}) Temperature Coefficient (Positive)	V _{(br)DSS}	24 –	28 25	– –	V _{dc} mV/°C
Zero Gate Voltage Drain Current (V _{DS} = 20 V _{dc} , V _{GS} = 0 V _{dc}) (V _{DS} = 20 V _{dc} , V _{GS} = 0 V _{dc} , T _J = 150 °C)	I _{DSS}	– –	– –	0.8 10	μA _{dc}
Gate-Body Leakage Current (V _{GS} = ±20 V _{dc} , V _{DS} = 0 V _{dc})	I _{GSS}	–	–	±100	nA _{dc}

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage (Note 5) (V _{DS} = V _{GS} , I _D = 250 μA _{dc}) Threshold Temperature Coefficient (Negative)	V _{GS(th)}	1.0 –	1.5 –4.0	2.0 –	V _{dc} mV/°C
Static Drain-to-Source On-Resistance (Note 5) V _{GS} = 10 V _{dc} , I _D = 17 A _{dc} V _{GS} = 4.5 V _{dc} , I _D = 15 A _{dc}	R _{DS(on)}	– –	8.0 12	10.8 14.8	mΩ
Forward Transconductance (Note 5) (V _{DS} = 10 V _{dc} , I _D = 17 A _{dc})	g _{FS}	–	20	–	Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 20 V _{dc} , V _{GS} = 0 V, f = 1 MHz)	C _{iss}	–	1150	1190	pF
Output Capacitance		C _{oss}	–	435	460	
Transfer Capacitance		C _{rss}	–	110	25	

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	(V _{GS} = 10 V _{dc} , V _{DD} = 15 V _{dc} , I _D = 17 A _{dc} , R _G = 2.5 Ω)	t _{d(on)}	–	7	9	ns
Rise Time		t _r	–	21	25	
Turn-Off Delay Time		t _{d(off)}	–	20	22	
Fall Time		t _f	–	3.5	5	
Gate Charge	(V _{GS} = 4.5 V _{dc} , I _D = 17 A _{dc} , V _{ds} = 10 V)	Q _{T(g)}	–	8	9.5	nC
		Q _{1(gs)}	–	2.0	–	
		Q _{2(gd)}	–	3.0	–	
		Q _{sw}	–	TBD	–	
		Q _{oss}	–	TBD	–	

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I _S = 8 A _{dc} , V _{GS} = 0 V _{dc}) (Note 5) (I _S = 1.5 A _{dc} , V _{GS} = 0 V _{dc} , T _J = 150°C)	V _{SD}	–	0.95 0.8	1.2 –	V _{dc}
Reverse Recovery Time	(I _S = 8 A _{dc} , V _{GS} = 0 V _{dc} , di _S /dt = 100 A/μs) (Note 5)	t _{rr}	–	33	45	ns
		t _a	–	15	–	
		t _b	–	18	–	
Reverse Recovery Stored Charge		Q _{RR}	–	0.025	–	μC

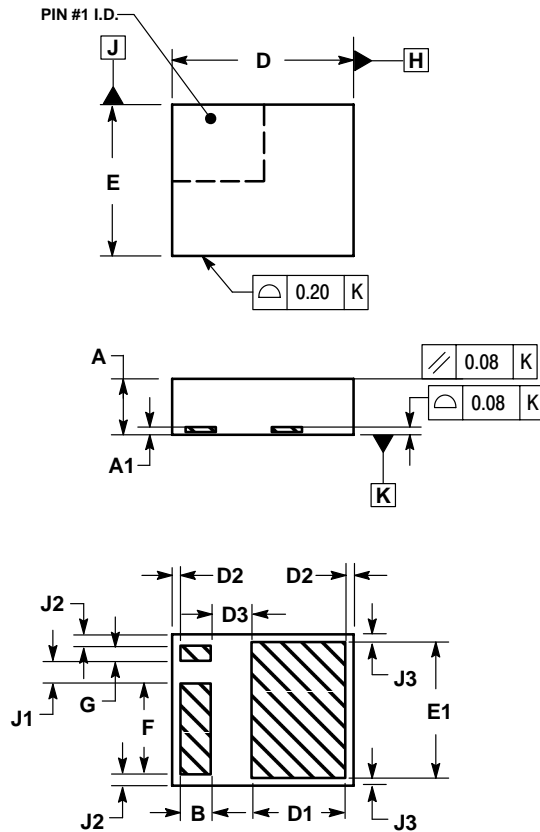
5. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

6. Switching characteristics are independent of operating junction temperatures.

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PACKAGE DIMENSIONS

SO-8 Leadless
CASE 751S-02
ISSUE A



- NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS	
	MIN	MAX
A	1.750	1.950
A1	0.254 REF	
B	0.900	1.100
D	6.000 BSC	
D1	3.046	3.246
D2	0.154	0.354
D3	1.246	1.446
E	5.000 BSC	
E1	4.392	4.592
F	2.940	3.140
G	0.400	0.600
J1	0.680	0.880
J2	0.250	0.450
J3	0.154	0.354

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