

# MJD200 (NPN) MJD210 (PNP)

## Complementary Plastic Power Transistors

### NPN/PNP Silicon DPAK For Surface Mount Applications

Designed for low voltage, low-power, high-gain audio amplifier applications.

#### Features

- Collector–Emitter Sustaining Voltage –  
 $V_{CE(sus)} = 25 \text{ Vdc (Min) @ } I_C = 10 \text{ mAdc}$
- High DC Current Gain –  $h_{FE} = 70 \text{ (Min) @ } I_C = 500 \text{ mAdc}$   
 $= 45 \text{ (Min) @ } I_C = 2 \text{ Adc}$   
 $= 10 \text{ (Min) @ } I_C = 5 \text{ Adc}$
- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Low Collector–Emitter Saturation Voltage –  
 $V_{CE(sat)} = 0.3 \text{ Vdc (Max) @ } I_C = 500 \text{ mAdc}$   
 $= 0.75 \text{ Vdc (Max) @ } I_C = 2.0 \text{ Adc}$
- High Current–Gain – Bandwidth Product –  
 $f_T = 65 \text{ MHz (Min) @ } I_C = 100 \text{ mAdc}$
- Annular Construction for Low Leakage –  
 $I_{CBO} = 100 \text{ nAdc @ Rated } V_{CB}$
- Epoxy Meets UL 94 V–0 @ 0.125 in
- ESD Ratings: Human Body Model, 3B > 8000 V  
Machine Model, C > 400 V
- Pb–Free Packages are Available

#### MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector–Base Voltage	$V_{CB}$	40	Vdc
Collector–Emitter Voltage	$V_{CEO}$	25	Vdc
Emitter–Base Voltage	$V_{EB}$	8.0	Vdc
Collector Current – Continuous – Peak	$I_C$	5.0 10	Adc
Base Current	$I_B$	1.0	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	12.5 0.1	W W/ $^\circ\text{C}$
Total Power Dissipation (Note 1) @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	1.4 0.011	W W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	–65 to +150	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

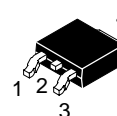
1. These ratings are applicable when surface mounted on the minimum pad sizes recommended.



ON Semiconductor®

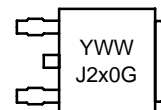
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**SILICON  
POWER TRANSISTORS  
5 AMPERES  
25 VOLTS, 12.5 WATTS**



**DPAK  
CASE 369C  
STYLE 1**

#### MARKING DIAGRAM



Y = Year  
WW = Work Week  
x = 1 or 0  
G = Pb–Free Package

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

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## THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	10	$^{\circ}\text{C/W}$
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	89.3	$^{\circ}\text{C/W}$

2. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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### OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (Note 3), ( $I_C = 10 \text{ mAdc}$ , $I_B = 0$ )	$V_{CE(sus)}$	25	–	Vdc
Collector Cutoff Current ( $V_{CB} = 40 \text{ Vdc}$ , $I_E = 0$ ) ( $V_{CB} = 40 \text{ Vdc}$ , $I_E = 0$ , $T_J = 125^{\circ}\text{C}$ )	$V_{CBO}$	–	100	nAdc $\mu\text{Adc}$
Emitter Cutoff Current ( $V_{BE} = 8 \text{ Vdc}$ , $I_C = 0$ )	$V_{EBO}$	–	100	nAdc

### ON CHARACTERISTICS

DC Current Gain (Note 3), ( $I_C = 500 \text{ mAdc}$ , $V_{CE} = 1 \text{ Vdc}$ ) ( $I_C = 2 \text{ Adc}$ , $V_{CE} = 1 \text{ Vdc}$ ) ( $I_C = 5 \text{ Adc}$ , $V_{CE} = 2 \text{ Vdc}$ )	$h_{FE}$	70 45 10	– 180 –	–
Collector-Emitter Saturation Voltage (Note 3) ( $I_C = 500 \text{ mAdc}$ , $I_B = 50 \text{ mAdc}$ ) ( $I_C = 2 \text{ Adc}$ , $I_B = 200 \text{ mAdc}$ ) ( $I_C = 5 \text{ Adc}$ , $I_B = 1 \text{ Adc}$ )	$V_{CE(sat)}$	– – –	0.3 0.75 1.8	Vdc
Base-Emitter Saturation Voltage (Note 3), ( $I_C = 5 \text{ Adc}$ , $I_B = 1 \text{ Adc}$ )	$V_{BE(sat)}$	–	2.5	Vdc
Base-Emitter On Voltage (Note 3), ( $I_C = 2 \text{ Adc}$ , $V_{CE} = 1 \text{ Vdc}$ )	$V_{BE(on)}$	–	1.6	Vdc

### DYNAMIC CHARACTERISTICS

Current-Gain – Bandwidth Product (Note 4) ( $I_C = 100 \text{ mAdc}$ , $V_{CE} = 10 \text{ Vdc}$ , $f_{test} = 10 \text{ MHz}$ )	$f_T$	65	–	MHz
Output Capacitance ( $V_{CB} = 10 \text{ Vdc}$ , $I_E = 0$ , $f = 0.1 \text{ MHz}$ )	$C_{ob}$	–	80 120	pF

3. Pulse Test: Pulse Width = 300  $\mu\text{s}$ , Duty Cycle  $\approx 2\%$ .

4.  $f_T = |h_{fe}| \cdot f_{test}$ .

## ORDERING INFORMATION

Device	Package Type	Shipping†
MJD200	DPAK	75 Units / Rail
MJD200G	DPAK (Pb-Free)	
MJD200RL	DPAK	1800 / Tape & Reel
MJD200RLG	DPAK (Pb-Free)	
MJD200T4	DPAK	2500 / Tape & Reel
MJD200T4G	DPAK (Pb-Free)	
MJD210	DPAK	75 Units / Rail
MJD210G	DPAK (Pb-Free)	
MJD210RL	DPAK	1800 / Tape & Reel
MJD210RLG	DPAK (Pb-Free)	
MJD210T4	DPAK	2500 / Tape & Reel
MJD210T4G	DPAK (Pb-Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MJD200 (NPN) MJD210 (PNP)

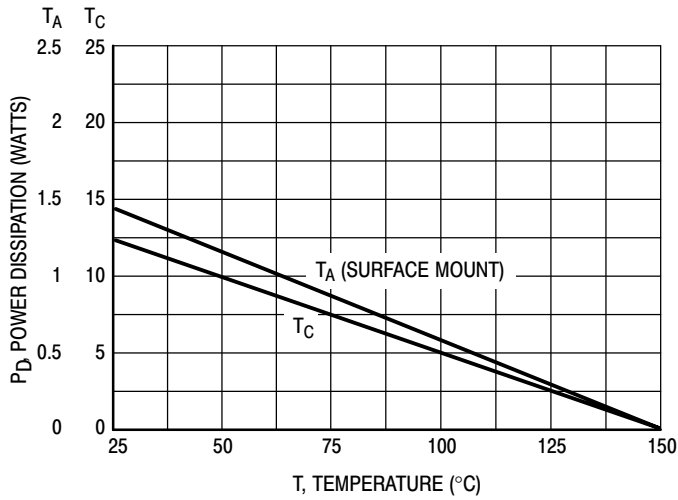
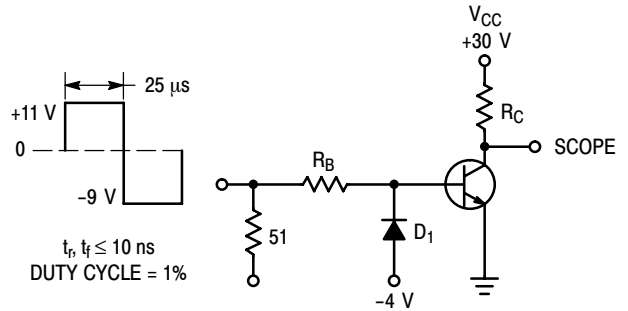


Figure 1. Power Derating



$R_B$  and  $R_C$  VARIED TO OBTAIN DESIRED CURRENT LEVELS  
 $D_1$  MUST BE FAST RECOVERY TYPE, e.g.:  
 1N5825 USED ABOVE  $I_B \approx 100$  mA FOR PNP TEST CIRCUIT,  
 MSD6100 USED BELOW  $I_B \approx 100$  mA REVERSE ALL POLARITIES

Figure 2. Switching Time Test Circuit

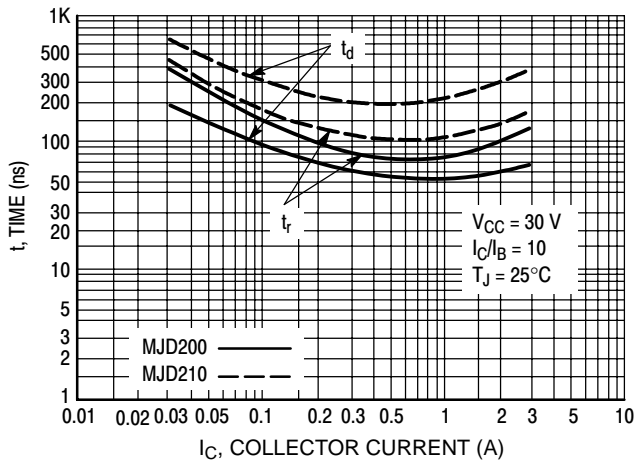


Figure 3. Turn-On Time

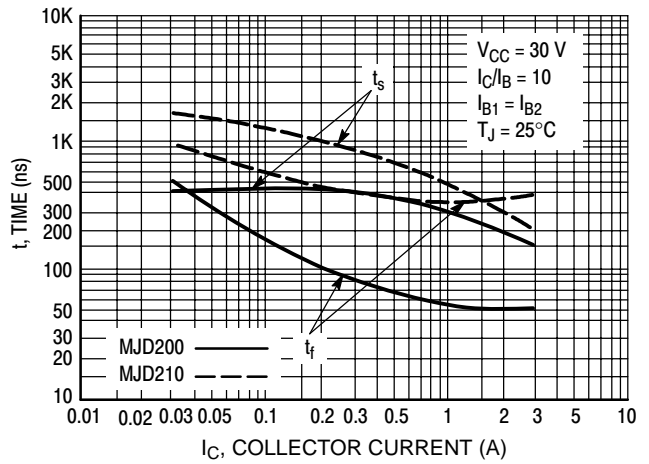


Figure 4. Turn-Off Time

# MJD200 (NPN) MJD210 (PNP)

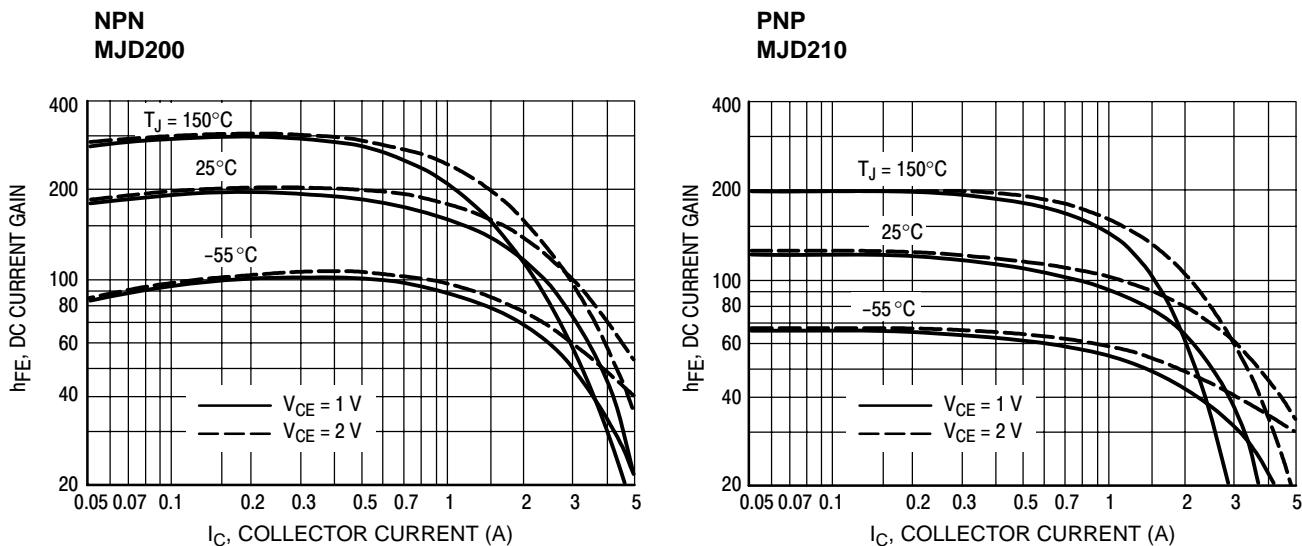


Figure 5. DC Current Gain

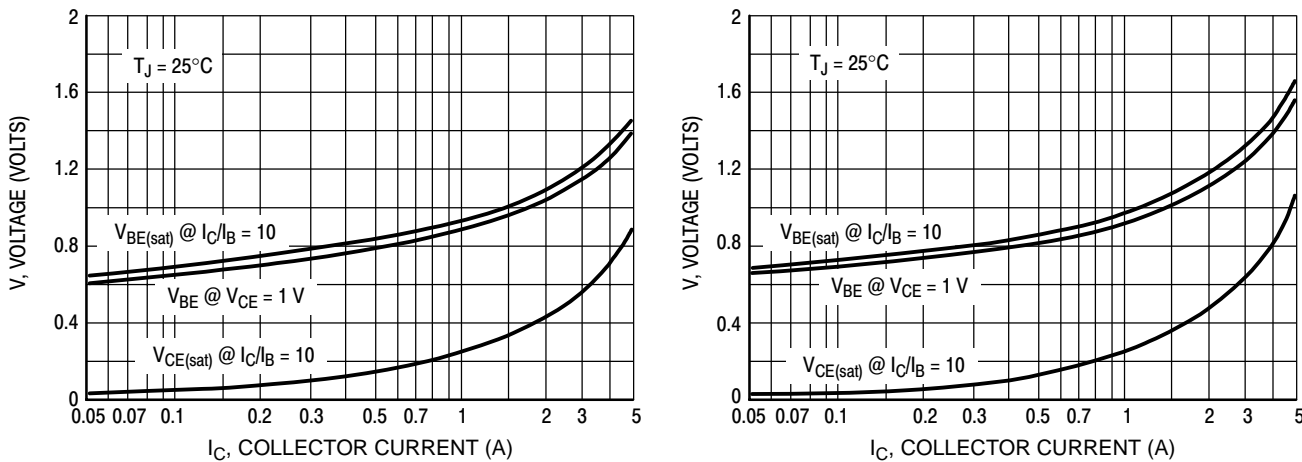


Figure 6. "On" Voltage

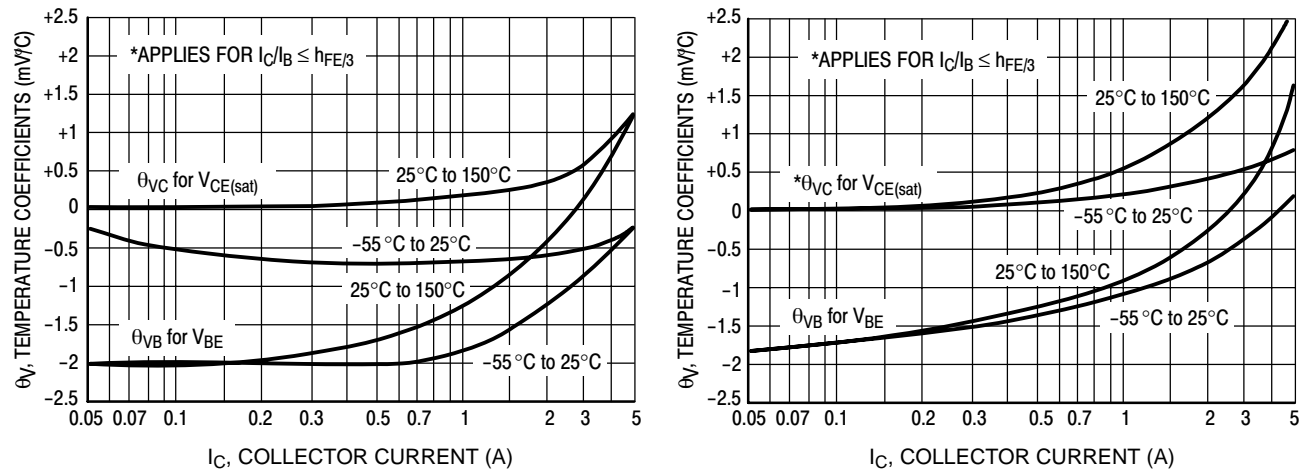


Figure 7. Temperature Coefficients

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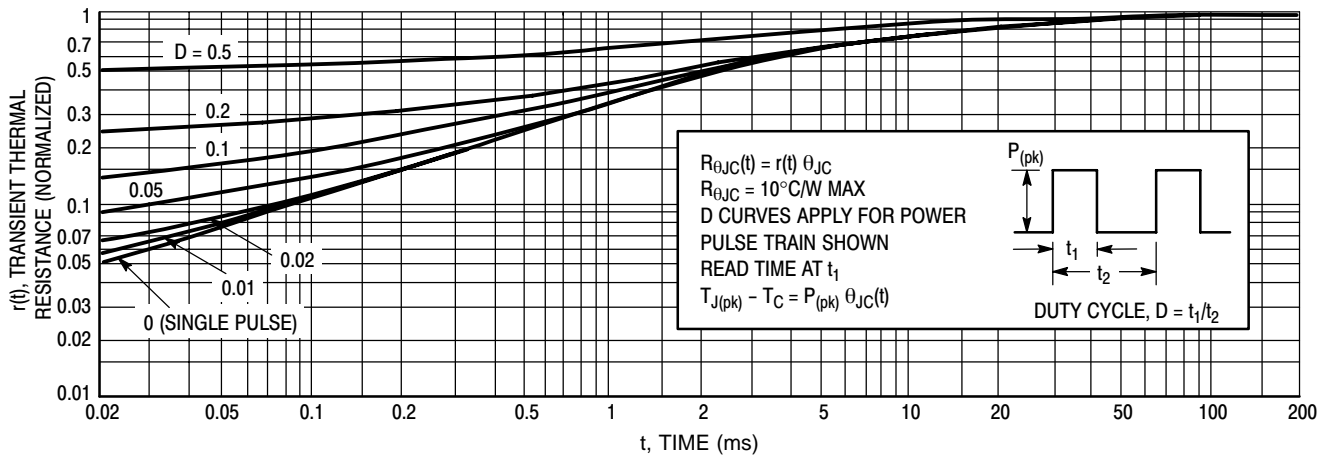


Figure 8. Thermal Response

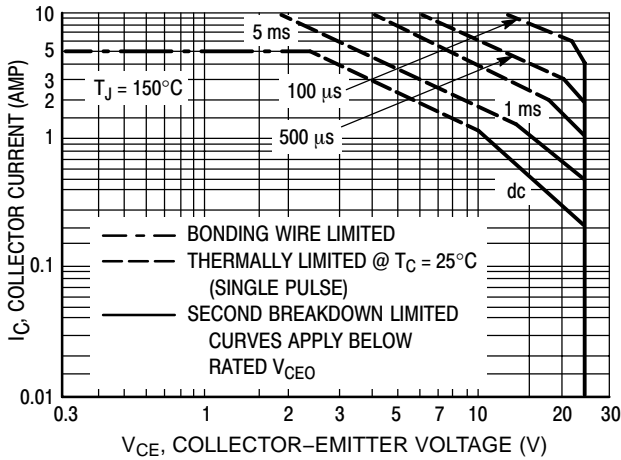


Figure 9. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 9 is based on  $T_{J(pk)} = 150^{\circ}\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^{\circ}\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 8. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

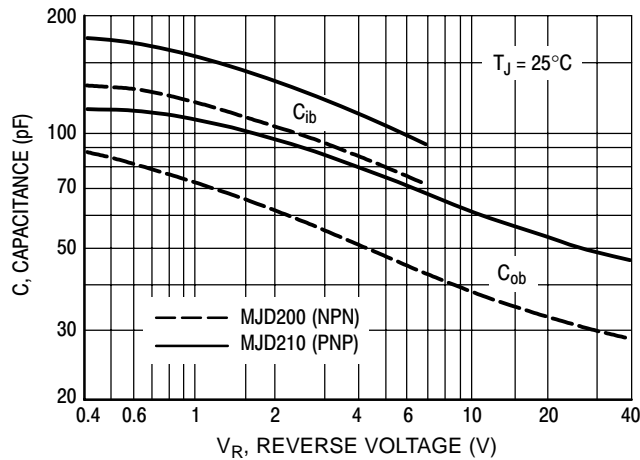
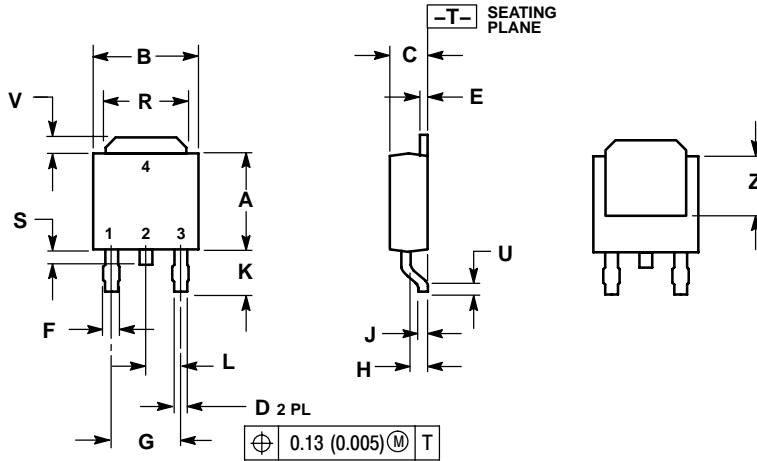


Figure 10. Capacitance

# MJD200 (NPN) MJD210 (PNP)

## PACKAGE DIMENSIONS

### DPAK CASE 369C ISSUE O



**NOTES:**

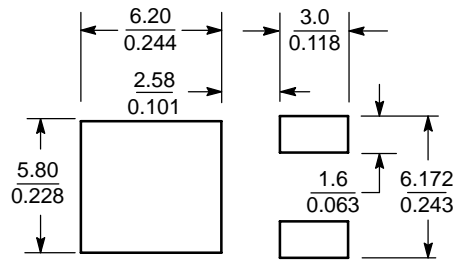
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

**STYLE 1:**

1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

### SOLDERING FOOTPRINT\*



SCALE 3:1  $\left( \frac{\text{mm}}{\text{inches}} \right)$

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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