LP2996 Evaluation Board

National Semiconductor
Application Note 1268
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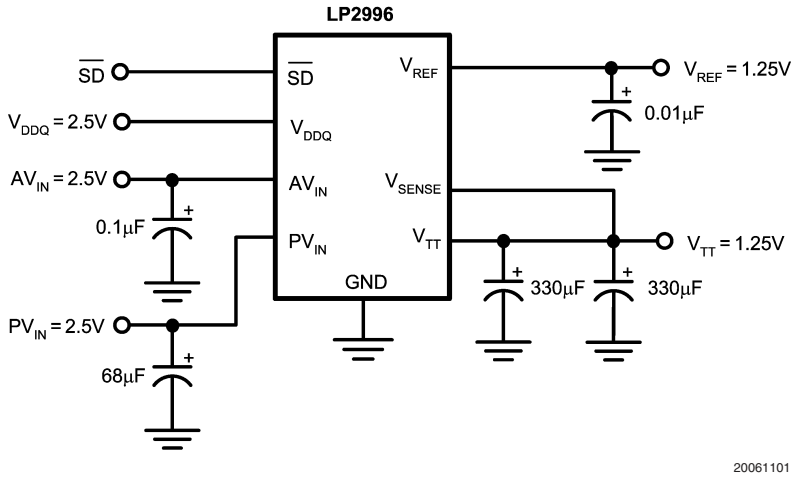
The LP2996 evaluation board is designed to provide the design engineer with a fully functional prototype system in which to evaluate the LP2996 in both a static environment and with a complete memory system. There are two versions of the board, while identical in functionality they differ in the package implemented, either a PSOP-8 or LLP-16 is used. This application note contains information regarding the board, for more information regarding the LP2996 please refer to the datasheet.

Schematic

The following schematic was used to create the layout.



Bill of Materials

Name	Value	Description	Manufacturer	Model Number
U1		LP2996 DDR Linear Regulator	National Semiconductor	LP2996MR or LP2996LQ
CAVIN	0.1µF	1206 Ceramic Capacitor X7R 25V	Vishay Vitrammon	VJ1206Y104KXXAT
COUT1	330µF	6.3V Electrolytic Radial FC Series	Panasonic	EEU-FC0J331S
COUT2	330µF	6.3V Electrolytic Radial FC Series	Panasonic	EEU-FC0J331S
CREF	0.01µF	1206 Ceramic Capacitor X7R 25V	Vishay Vitrammon	VJ1206Y103KXXAT
CPVIN	68µF	6.3V Electrolytic Radial FC series	Panasonic	EEU-FC0J680

Application

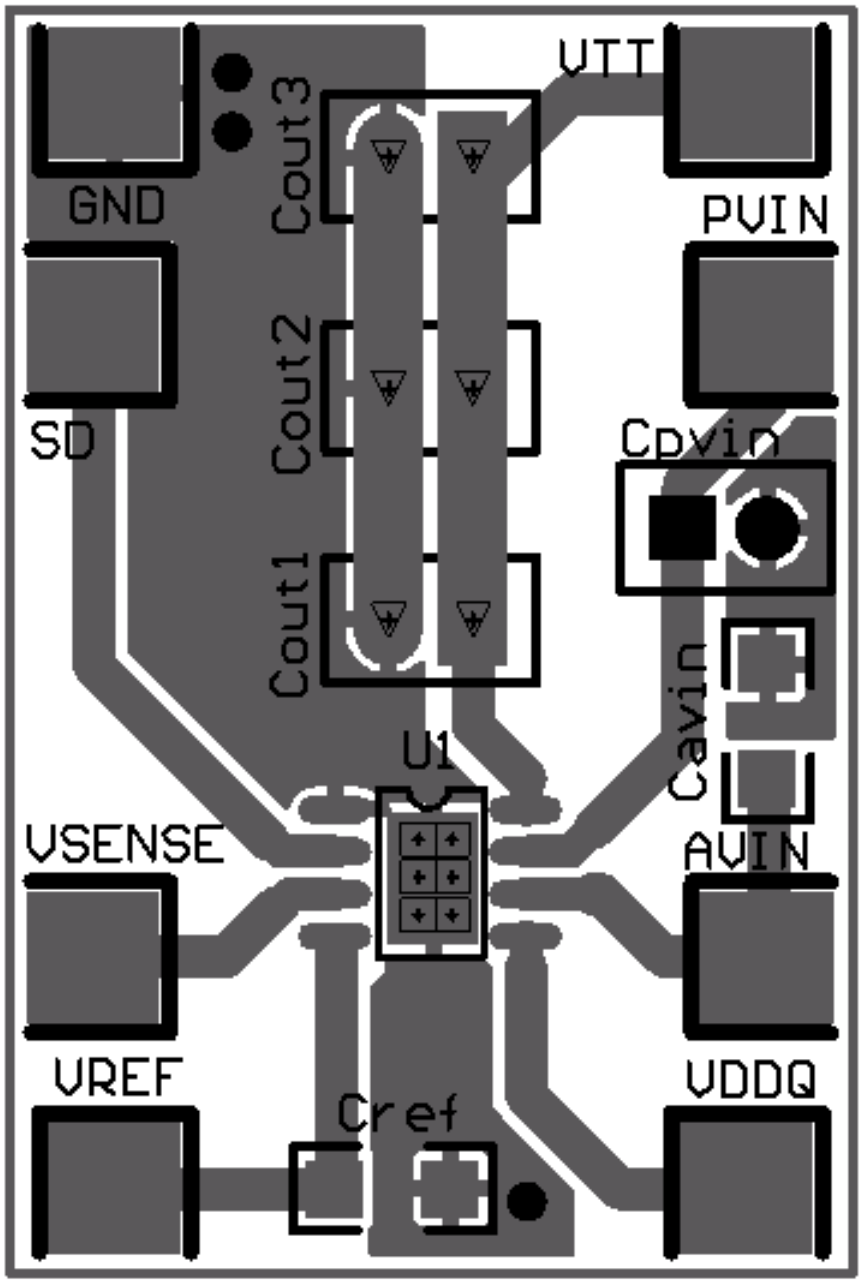
The LP2996 evaluation board can be used immediately in either a static test environment to check functionality or in a memory termination scheme on a motherboard. In either implementation the following steps should be taken to ensure correct operation.

1. Connect leads from the evaluation board. The board layout has been designed to allow banana jack sockets to be directly soldered.
2. AVIN and PVIN should be connected to a 2.5V power supply.
3. The VDDQ input provides the internal divide by two reference voltage. Both VREF and VTT will track this internal voltage, nominally a 2.5V will be applied.
4. The VREF pad is the output for the VREF from the LP2996 after being bypassed by a ceramic capacitor. This can be connected either to a multimeter for confirmation or directly to the memory controller and DIMMS.
5. The SD pin can be initially left floating as it has an internal pull-up
6. The remaining two pads are for the force and sense leads of the VTT output. These should be connected directly to the termination plane or a multimeter if interested in verification. The output will be regulated where the VSENSE leads connect to the VTT leads permitting the connection to a motherboard without suffering from large resistance drops.

Performance

The LP2996 has been designed to accommodate several different capacitor options to allow the designer to optimize the solution for the specific application. For most desktop systems large aluminum electrolytic capacitors will be used for their low cost. However, in height limited situations such as laptops fewer high performance capacitors might be implemented such as specialty polymers. The table below lists some of the capacitors that can be used and a vendor that offers that product line.

Capacitor Series	Vendor	Vendor Phone Number
Oscon	Vishay	(207)-324-4140
SP	Panasonic	(714)-373-7857
MLCC	Taiyo Yuden	(800)-348-2496
Aluminum	Panasonic	(714)-373-7857



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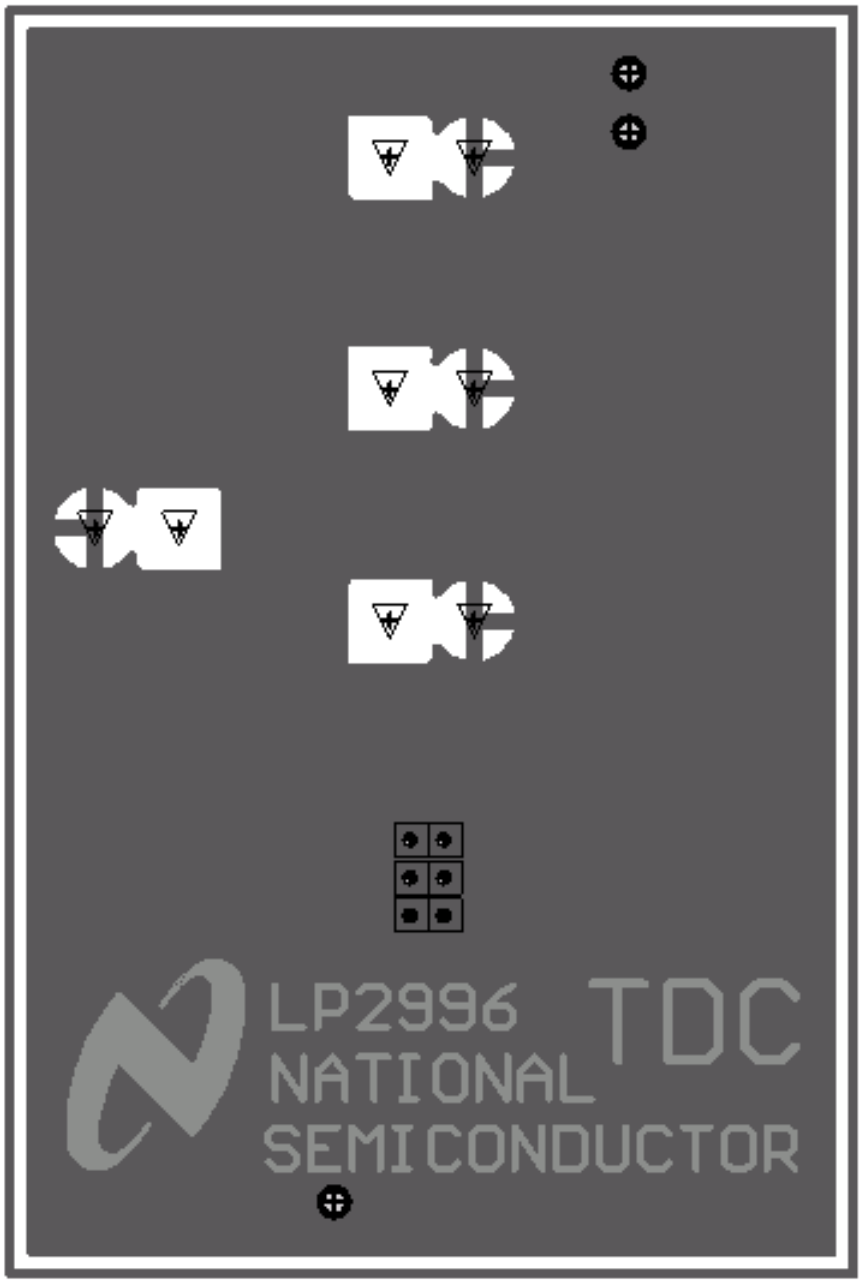
PSOP Top Layer



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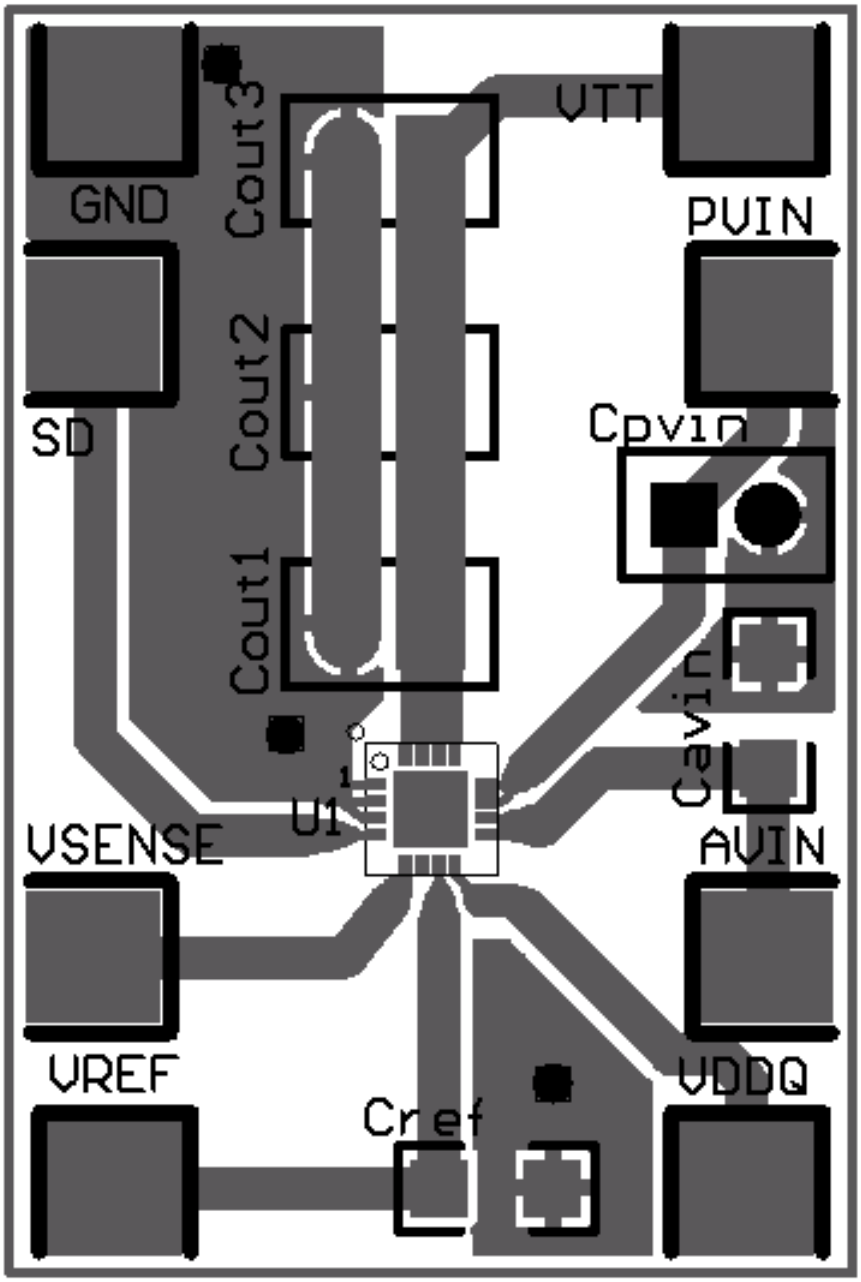
PSOP Bottom Layer



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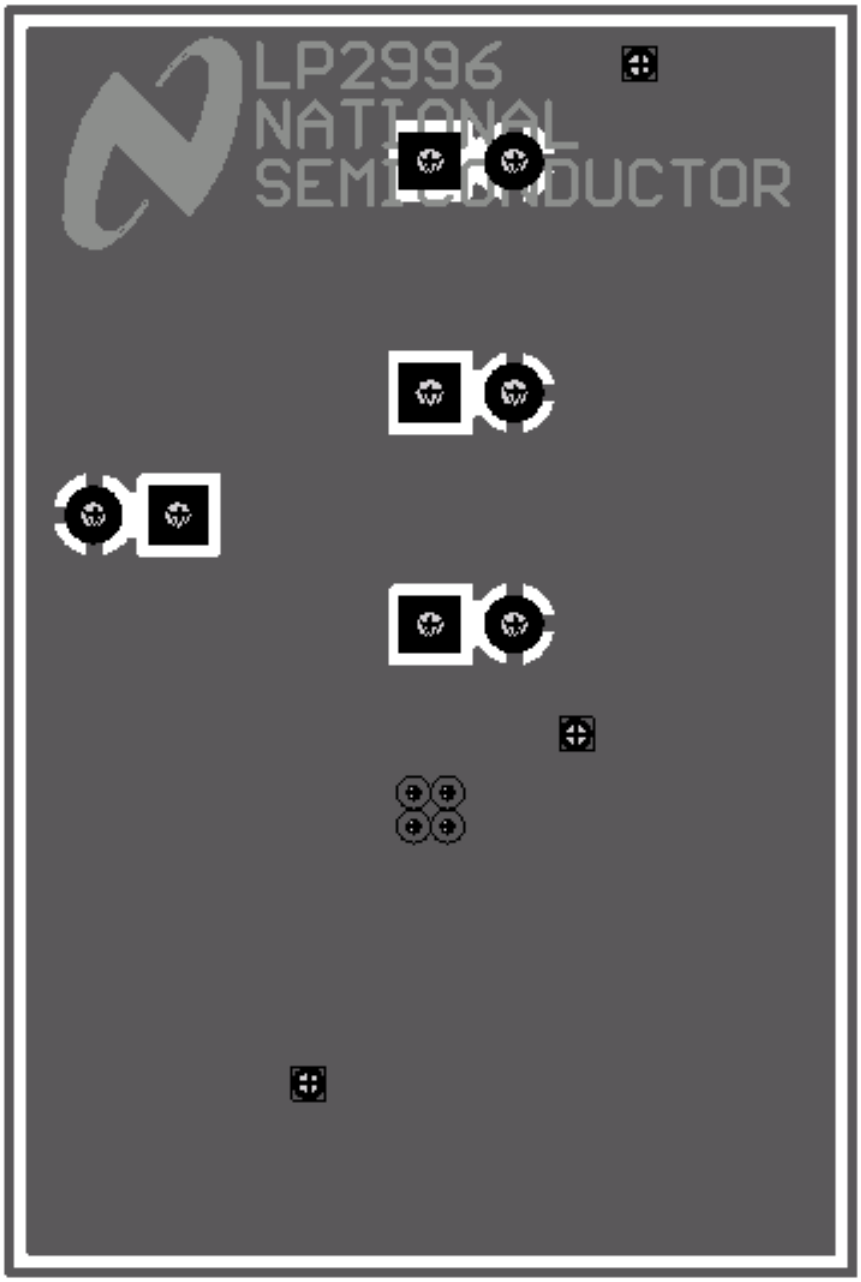
LLP Top Layer



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LLP Bottom Layer

Information	PSOP-8 Board	LLP-16 Board
Board Material	FR4	FR4
Size	1.0 x 1.5 inches	1.0 x 1.5 inches
Board Thickness	0.062 inch	0.062 inch
Layers	2	2
Copper Thickness	1oz.	1oz.
Plating	HASL	HASL
Thermal Vias	6	4
Thermal Vias Size	10 mil	13 mil
Board Thickness	0.062 inch	0.062 inch

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