

USB2.0 HOST CONTROLLER



The μ PD720101 complies with the Universal Serial Bus Specification Revision 2.0 and Open Host Controller Interface Specification for full-/low-speed signaling and Intel's Enhanced Host Controller Interface Specification for high-speed signaling and works up to 480 Mbps. The μ PD720101 is integrated 3 host controller cores with PCI interface and USB2.0 transceivers into a single chip.

Detailed function descriptions are provided in the following user's manual. Be sure to read the manual before designing.

μ PD720101 User's Manual: S16336E

FEATURES

- Compliant with Universal Serial Bus Specification Revision 2.0 (Data rate 1.5/12/480 Mbps)
- Compliant with Open Host Controller Interface Specification for USB Rev 1.0a
- Compliant with Enhanced Host Controller Interface Specification for USB Rev 1.0
- PCI multi-function device consists of two OHCI host controller cores for full-/low-speed signaling and one EHCI host controller core for high-speed signaling.
- Root hub with 5 (max.) downstream facing ports which are shared by OHCI and EHCI host controller cores.
- All downstream facing ports can handle high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) transaction.
- Configurable number of downstream facing ports (2 to 5)
- 32-bit 33 MHz host interface compliant to PCI Specification release 2.2
- Supports PCI Mobile Design Guide Revision 1.1
- Supports PCI-Bus Power Management Interface Specification release 1.1
- PCI bus bus-master access
- System clock is generated by 30 MHz X'tal or 48 MHz clock input.
 - System clock frequency should be set from system software (BIOS) or EEPROM. More detail, see μ PD720101 User's Manual.
- Operational registers direct-mapped to PCI memory space
- Legacy support for all downstream facing ports. Legacy support features allow easy migration for motherboard implementation.
- 3.3 V power supply, PCI signal pins have 5 V tolerant circuit.

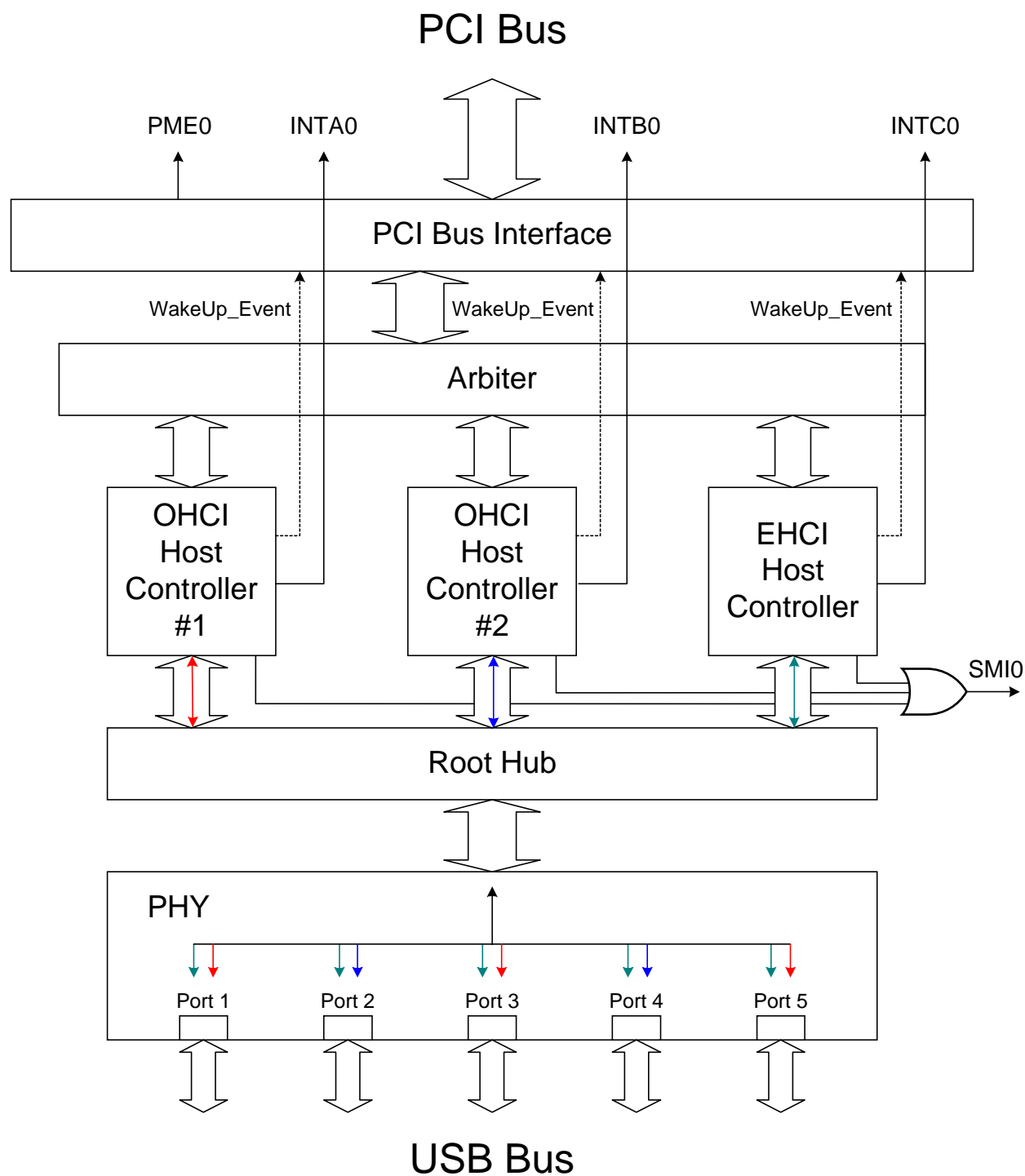
ORDERING INFORMATION

| Part Number | Package |
|----------------------|---|
| μ PD720101GJ-UEN | 144-pin plastic LQFP (Fine pitch) (20 × 20) |
| μ PD720101F1-EA8 | 144-pin plastic FBGA (12 × 12) |

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.

Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.

BLOCK DIAGRAM



Remark INTB0/INTC0 can be shared with INTA0 through BIOS setting. (Planning)

| | |
|-------------------------|--|
| PCI Bus Interface | : handles 32-bit 33 MHz PCI bus master and target function which comply with PCI specification release 2.2. The number of enabled ports is set by bit in configuration space. |
| Arbiter | : arbitrates among two OHCI host controller cores and one EHCI host controller core. |
| OHCI Host Controller #1 | : handles full- (12 Mbps)/low-speed (1.5 Mbps) signaling at port 1, 3, and 5. |
| OHCI Host Controller #2 | : handles full- (12 Mbps)/low-speed (1.5 Mbps) signaling at port 2 and 4. |
| EHCI Host Controller | : handles high- (480 Mbps) signaling at port 1, 2, 3, 4, and 5. |
| Root Hub | : handles USB hub function in host controller and controls connection (routing) between host controller core and port. |
| PHY | : consists of high-speed transceiver, full-/low-speed transceiver, serializer, deserializer, etc. |
| INTA0 | : is the PCI interrupt signal for OHCI Host Controller #1. |
| INTB0 | : is the PCI interrupt signal for OHCI Host Controller #2. |
| INTC0 | : is the PCI interrupt signal for EHCI Host Controller. |
| SMI0 | : is the interrupt signal which is specified by Open Host Controller Interface Specification for USB Rev 1.0a and Enhanced Host Controller Interface Specification Rev 1.0. The SMI signal of each OHCI Host Controller and EHCI Host Controller appears at this signal. |
| PME0 | : is the interrupt signal which is specified by PCI-Bus Power Management Interface Specification release 1.1. Wakeup signal of each host controller core appears at this signal. |

COMPARISON WITH THE μPD720100A

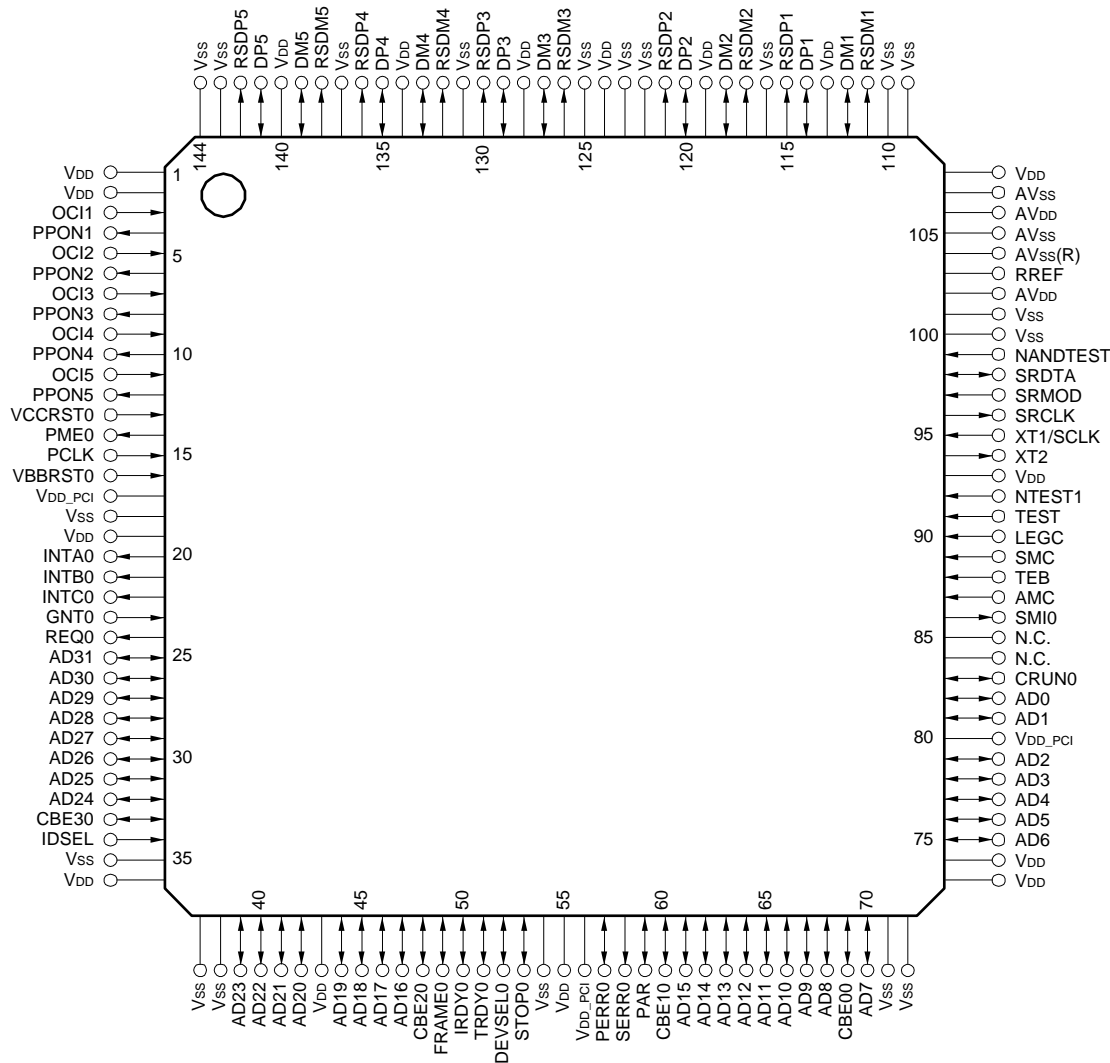
| | μPD720100A | μPD720101 (2nd generation) |
|----------------|----------------------------------|----------------------------------|
| EHCI revision | 0.95 | 1.0 |
| EHCI | 1 | 1 |
| OHCI | 2 | 2 |
| Legacy support | Parallel IRQ out support | No parallel IRQ support |
| Clock | 48 MHz OSC or 30 MHz OSC/X'tal | 48 MHz OSC or 30 MHz X'tal |
| Package | 176-pin BGA (FP) or 160-pin LQFP | 144-pin BGA (FP) or 144-pin LQFP |

PIN CONFIGURATION

- 144-pin plastic LQFP (Fine pitch) (20 × 20)

μPD720101GJ-UEN

Top View



| Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name |
|---------|---------------------|---------|---------------------|---------|---------------------|---------|-----------------|
| 1 | V _{DD} | 37 | V _{SS} | 73 | V _{DD} | 109 | V _{SS} |
| 2 | V _{DD} | 38 | V _{SS} | 74 | V _{DD} | 110 | V _{SS} |
| 3 | OCI1 | 39 | AD23 | 75 | AD6 | 111 | RSDM1 |
| 4 | PPON1 | 40 | AD22 | 76 | AD5 | 112 | DM1 |
| 5 | OCI2 | 41 | AD21 | 77 | AD4 | 113 | V _{DD} |
| 6 | PPON2 | 42 | AD20 | 78 | AD3 | 114 | DP1 |
| 7 | OCI3 | 43 | V _{DD} | 79 | AD2 | 115 | RSDP1 |
| 8 | PPON3 | 44 | AD19 | 80 | V _{DD_PCI} | 116 | V _{SS} |
| 9 | OCI4 | 45 | AD18 | 81 | AD1 | 117 | RSDM2 |
| 10 | PPON4 | 46 | AD17 | 82 | AD0 | 118 | DM2 |
| 11 | OCI5 | 47 | AD16 | 83 | CRUN0 | 119 | V _{DD} |
| 12 | PPON5 | 48 | CBE20 | 84 | N.C. | 120 | DP2 |
| 13 | VCCRST0 | 49 | FRAME0 | 85 | N.C. | 121 | RSDP2 |
| 14 | PME0 | 50 | IRDY0 | 86 | SMI0 | 122 | V _{SS} |
| 15 | PCLK | 51 | TRDY0 | 87 | AMC | 123 | V _{SS} |
| 16 | VBBRST0 | 52 | DEVSEL0 | 88 | TEB | 124 | V _{DD} |
| 17 | V _{DD_PCI} | 53 | STOP0 | 89 | SMC | 125 | V _{SS} |
| 18 | V _{SS} | 54 | V _{SS} | 90 | LEGC | 126 | RSDM3 |
| 19 | V _{DD} | 55 | V _{DD} | 91 | TEST | 127 | DM3 |
| 20 | INTA0 | 56 | V _{DD_PCI} | 92 | NTEST1 | 128 | V _{DD} |
| 21 | INTB0 | 57 | PERR0 | 93 | V _{DD} | 129 | DP3 |
| 22 | INTC0 | 58 | SERR0 | 94 | XT2 | 130 | RSDP3 |
| 23 | GNT0 | 59 | PAR | 95 | XT1/SCLK | 131 | V _{SS} |
| 24 | REQ0 | 60 | CBE10 | 96 | SRCLK | 132 | RSDM4 |
| 25 | AD31 | 61 | AD15 | 97 | SRMOD | 133 | DM4 |
| 26 | AD30 | 62 | AD14 | 98 | SRDTA | 134 | V _{DD} |
| 27 | AD29 | 63 | AD13 | 99 | NANDTEST | 135 | DP4 |
| 28 | AD28 | 64 | AD12 | 100 | V _{SS} | 136 | RSDP4 |
| 29 | AD27 | 65 | AD11 | 101 | V _{SS} | 137 | V _{SS} |
| 30 | AD26 | 66 | AD10 | 102 | AV _{DD} | 138 | RSDM5 |
| 31 | AD25 | 67 | AD9 | 103 | RREF | 139 | DM5 |
| 32 | AD24 | 68 | AD8 | 104 | AV _{SS(R)} | 140 | V _{DD} |
| 33 | CBE30 | 69 | CBE00 | 105 | AV _{SS} | 141 | DP5 |
| 34 | IDSEL | 70 | AD7 | 106 | AV _{DD} | 142 | RSDP5 |
| 35 | V _{SS} | 71 | V _{SS} | 107 | AV _{SS} | 143 | V _{SS} |
| 36 | V _{DD} | 72 | V _{SS} | 108 | V _{DD} | 144 | V _{SS} |

Remark AV_{SS(R)} should be used to connect RREF through 1 % precision reference resistor of 9.1 kΩ.
Pins 84 and 85 must be clamped high on the board.

- 144-pin plastic FBGA (12 × 12)

μPD720101F1-EA8

Bottom View

| | | | | | | | | | | | | | | |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|----|----|----|
| | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 | 35 | 36 | | 14 |
| 24 | 71 | 72 | 73 | 74 | 75 | 76 | 77 | 78 | 79 | 80 | 81 | 82 | 37 | 13 |
| 23 | 70 | 111 | 112 | 113 | 114 | 115 | 116 | 117 | 118 | 119 | 120 | 83 | 38 | 12 |
| 22 | 69 | 110 | | | 137 | 138 | 139 | 140 | | | 121 | 84 | 39 | 11 |
| 21 | 68 | 109 | | | | | | | | | 122 | 85 | 40 | 10 |
| 20 | 67 | 108 | 136 | | | | | | | 141 | 123 | 86 | 41 | 9 |
| 19 | 66 | 107 | 135 | | | | | | | 142 | 124 | 87 | 42 | 8 |
| 18 | 65 | 106 | 134 | | | | | | | 143 | 125 | 88 | 43 | 7 |
| 17 | 64 | 105 | 133 | | | | | | | 144 | 126 | 89 | 44 | 6 |
| 16 | 63 | 104 | | | | | | | | | 127 | 90 | 45 | 5 |
| 15 | 62 | 103 | | | 132 | 131 | 130 | 129 | | | 128 | 91 | 46 | 4 |
| 14 | 61 | 102 | 101 | 100 | 99 | 98 | 97 | 96 | 95 | 94 | 93 | 92 | 47 | 3 |
| 13 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 2 |
| | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | | 1 |
| P | N | M | L | K | J | H | G | F | E | D | C | B | A | |

| Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name | Pin No. | Pin Name |
|---------|------------------|---------|----------------------|---------|---------------------|---------|---------------------|
| 1 | V _{SS} | 37 | V _{DD} | 73 | V _{DD} | 109 | NANDTEST |
| 2 | AD23 | 38 | V _{DD} | 74 | RSDP1 | 110 | V _{SS} |
| 3 | AD20 | 39 | PPON2 | 75 | V _{DD} | 111 | AV _{SS} |
| 4 | AD18 | 40 | OCI4 | 76 | V _{DD} | 112 | V _{SS} |
| 5 | CBE20 | 41 | PPON5 | 77 | DP3 | 113 | DM2 |
| 6 | TRDY0 | 42 | PCLK | 78 | V _{DD} | 114 | RSDP2 |
| 7 | SERR0 | 43 | INTC0 | 79 | RSMD5 | 115 | V _{SS} |
| 8 | AD15 | 44 | AD31 | 80 | V _{DD} | 116 | V _{DD} |
| 9 | AD12 | 45 | AD28 | 81 | DP5 | 117 | RSMD4 |
| 10 | AD9 | 46 | AD25 | 82 | V _{SS} | 118 | DP4 |
| 11 | AD7 | 47 | V _{DD} | 83 | OCI1 | 119 | V _{SS} |
| 12 | V _{SS} | 48 | V _{SS} | 84 | OCI2 | 120 | PPON1 |
| 13 | V _{DD} | 49 | V _{SS} | 85 | OCI3 | 121 | PPON3 |
| 14 | V _{DD} | 50 | AD22 | 86 | OCI5 | 122 | PPON4 |
| 15 | AD3 | 51 | AD21 | 87 | VBBRST0 | 123 | VCCRST0 |
| 16 | AD1 | 52 | V _{DD} | 88 | INTB0 | 124 | V _{DD_PCI} |
| 17 | N.C. | 53 | AD16 | 89 | AD30 | 125 | INTA0 |
| 18 | AMC | 54 | DEVSEL0 | 90 | AD26 | 126 | REQ0 |
| 19 | XT2 | 55 | PERR0 | 91 | AD24 | 127 | AD29 |
| 20 | SRMOD | 56 | AD14 | 92 | IDSEL | 128 | AD27 |
| 21 | V _{SS} | 57 | AD10 | 93 | CBE30 | 129 | IRDY0 |
| 22 | RREF | 58 | AD8 | 94 | AD19 | 130 | V _{SS} |
| 23 | V _{DD} | 59 | CBE00 | 95 | AD17 | 131 | V _{DD} |
| 24 | AV _{SS} | 60 | V _{SS} | 96 | FRAME0 | 132 | PAR |
| 25 | V _{SS} | 61 | AD6 | 97 | STOP0 | 133 | SMI0 |
| 26 | RSMD1 | 62 | AD4 | 98 | V _{DD_PCI} | 134 | LEGC |
| 27 | DP1 | 63 | AD2 | 99 | CBE10 | 135 | TEST |
| 28 | RSMD2 | 64 | CRUN0 | 100 | AD13 | 136 | XT1/SCLK |
| 29 | DP2 | 65 | TEB | 101 | AD11 | 137 | V _{SS} |
| 30 | V _{SS} | 66 | V _{DD} | 102 | AD5 | 138 | RSMD3 |
| 31 | RSDP3 | 67 | SRDTA | 103 | V _{DD_PCI} | 139 | DM3 |
| 32 | DM4 | 68 | AV _{DD} | 104 | AD0 | 140 | V _{SS} |
| 33 | RSDP4 | 69 | AV _{SS} (R) | 105 | N.C. | 141 | PME0 |
| 34 | DM5 | 70 | AV _{DD} | 106 | SMC | 142 | V _{SS} |
| 35 | RSDP5 | 71 | V _{SS} | 107 | NTEST1 | 143 | V _{DD} |
| 36 | V _{SS} | 72 | DM1 | 108 | SRCLK | 144 | GNT0 |

Remark AV_{SS}(R) should be used to connect RREF through 1 % precision reference resistor of 9.1 k Ω .
Pins 17 and 105 must be clamped high on the board.

1. PIN INFORMATION

(1/2)

| Pin Name | I/O | Buffer Type | Active Level | Function |
|--------------|---------|------------------------------|--------------|---|
| AD (31 : 0) | I/O | 5 V PCI I/O | | PCI "AD [31 : 0]" signal |
| CBE (3 : 0)0 | I/O | 5 V PCI I/O | | PCI "C/BE [3 : 0]" signal |
| PAR | I/O | 5 V PCI I/O | | PCI "PAR" signal |
| FRAME0 | I/O | 5 V PCI I/O | | PCI "FRAME#" signal |
| IRDY0 | I/O | 5 V PCI I/O | | PCI "IRDY#" signal |
| TRDY0 | I/O | 5 V PCI I/O | | PCI "TRDY#" signal |
| STOP0 | I/O | 5 V PCI I/O | | PCI "STOP#" signal |
| IDSEL | I | 5 V PCI input | | PCI "IDSEL" signal |
| DEVSEL0 | I/O | 5 V PCI I/O | | PCI "DEVSEL#" signal |
| REQ0 | O | 5 V PCI output | | PCI "REQ#" signal |
| GNT0 | I | 5 V PCI input | | PCI "GNT#" signal |
| PERR0 | I/O | 5 V PCI I/O | | PCI "PERR#" signal |
| SERR0 | O | 5 V PCI N-ch open drain | | PCI "SERR#" signal |
| INTA0 | O | 5 V PCI N-ch open drain | Low | PCI "INTA#" signal |
| INTB0 | O | 5 V PCI N-ch open drain | Low | PCI "INTB#" signal |
| INTC0 | O | 5 V PCI N-ch open drain | Low | PCI "INTC#" signal |
| PCLK | I | 5 V PCI input | | PCI "CLK" signal |
| VBBRST0 | I | 5 V tolerant input | Low | Hardware reset for chip |
| CRUN0 | I/O | 5 V PCI I/O | | PCI "CLKRUN#" signal |
| PME0 | O | 5 V PCI N-ch open drain | Low | PCI "PME#" signal |
| VCCRST0 | I | 5 V tolerant input | Low | Reset for power management |
| SMI0 | O | 5 V tolerant N-ch open drain | Low | System management interrupt output |
| XT1/SCLK | I | Input | | System clock input or oscillator in |
| XT2 | O | Output | | oscillator out |
| DP (5 : 1) | I/O | USB high speed D+ I/O | | USB high speed D+ signal |
| DM (5 : 1) | I/O | USB high speed D- I/O | | USB high speed D- signal |
| RSDP (5 : 1) | O | USB full speed D+ Output | | USB full speed D+ signal |
| RSDM (5 : 1) | O | USB full speed D- Output | | USB full speed D- signal |
| OCI (5 : 1) | I (I/O) | Input | Low | USB root hub port's overcurrent status input |
| PPON (5 : 1) | O (I/O) | Output | High | USB root hub port's power supply control output |
| LEGC | I (I/O) | Input | High | Legacy support switch |
| SRCLK | O | Output | | Serial ROM clock out |
| SRDTA | I/O | I/O | | Serial ROM data |
| SRMOD | I | Input with 50 kΩ pull down R | High | Serial ROM input enable |
| RREF | A | Analog | | Reference resistor |
| NTEST1 | I | Input with 12 kΩ pull down R | High | Test pin |

(2/2)

| Pin Name | I/O | Buffer Type | Active Level | Function |
|---------------------|-----|------------------------------|--------------|------------------------------------|
| SMC | I | Input with 50 kΩ pull down R | High | Scan mode control |
| TEB | I | Input with 50 kΩ pull down R | High | BIST enable |
| AMC | I | Input with 50 kΩ pull down R | High | ATG mode control |
| TEST | I | Input with 50 kΩ pull down R | High | Test control |
| NANDTEST | I | Input with 50 kΩ pull down R | High | NAND tree test enable |
| AV _{DD} | | | | V _{DD} for analog circuit |
| V _{DD} | | | | V _{DD} |
| V _{DD_PCI} | | | | 5 V (5 V PCI) or 3.3 V (3.3 V PCI) |
| AV _{SS} | | | | V _{SS} for analog circuit |
| V _{SS} | | | | V _{SS} |
| N.C. | | | | No connection |

- Remarks 1.** “5 V tolerant“ means that the buffer is 3 V buffer with 5 V tolerant circuit.
- 2.** “5 V PCI” indicates a PCI buffer, which complies with the 3 V PCI standard, has a 5 V tolerant circuit. It does not indicate that this buffer fully complies with 5 V PCI standard. However, this function can be used for evaluating the operation of a device on a 5 V add-in card.
- 3.** The signal marked as “(I/O)” in the above table operates as I/O signals during testing. However, they do not need to be considered in normal use.

2. HOW TO CONNECT TO EXTERNAL ELEMENTS

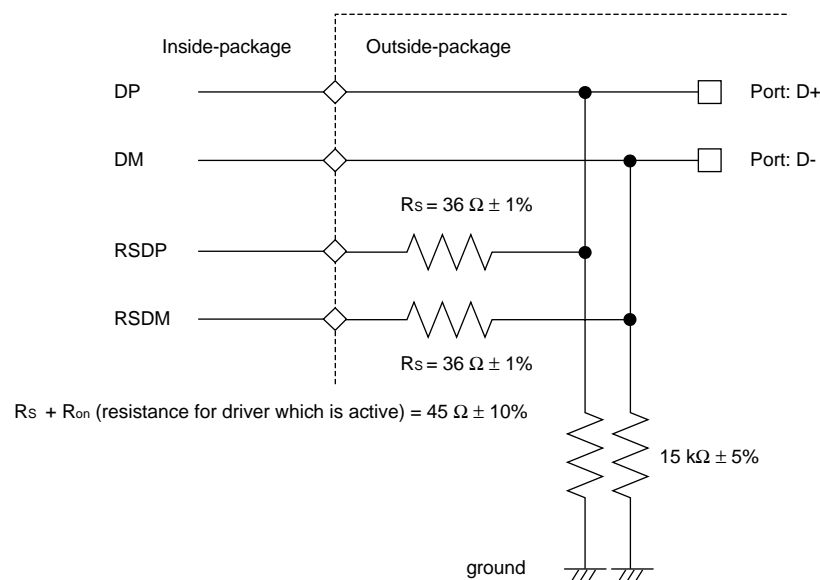
2.1 Handling Unused Pins

To realize less than 5 ports host controller implementation, appropriate value shall be set to Port No field in EXT1 register. And unused pins shall be connected as shown below.

| Pin | Direction | Connection Method |
|-------|-----------|----------------------|
| DPx | I/O | Tied to "low". |
| DMx | I/O | Tied to "low". |
| RSDPx | O | No connection (Open) |
| RSDMx | O | No connection (Open) |
| OCIx | I | "H" clamp |
| PPONx | O | No connection (Open) |

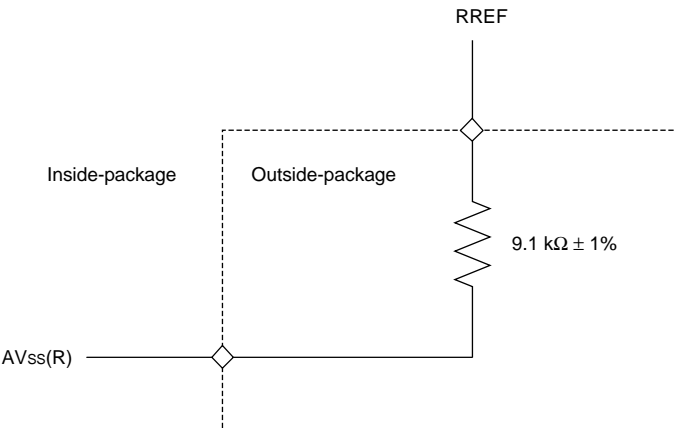
2.2 USB Port Connection

Figure 2-1. USB Downstream Port Connection



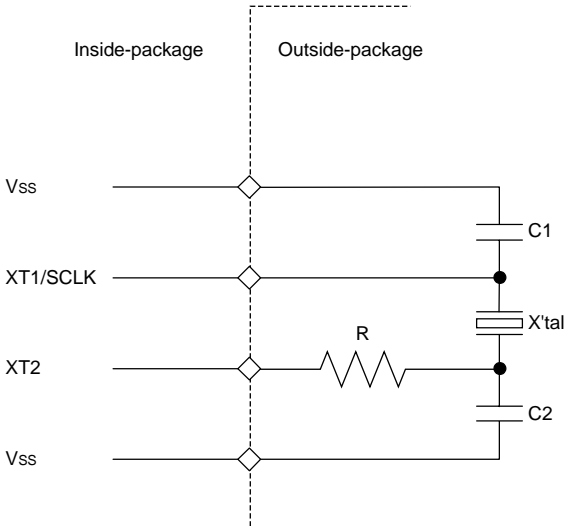
2.3 PLL Capacitor Connection

Figure 2-2. RREF Connection



2.4 X'tal Connection

Figure 2-3. X'tal Connection



The following crystals are evaluated on our reference design board. Table 2-1 shows the external parameters.

Table 2-1. External Parameters

| Vender | X'tal | R | C1 | C2 |
|-----------------------|---------------------|-------|-------|-------|
| KDS ^{Note 1} | AT-49 30.000 MHz | 100 Ω | 12 pF | 10 pF |
| NDK ^{Note 2} | AT-41 30.000 MHz | 100 Ω | 10 pF | 10 pF |
| | AT-41CD2 30.000 MHz | 100 Ω | 10 pF | 10 pF |
| | NX3225DA 30.000 MHz | 100 Ω | 10 pF | 10 pF |
| | NX5032GA 30.000 MHz | 100 Ω | 10 pF | 10 pF |
| | NX8045GB 30.000 MHz | 100 Ω | 10 pF | 10 pF |

Notes 1. DAISHINKU CORP.

2. NIHON DEMPA KOGYO CO., LTD.

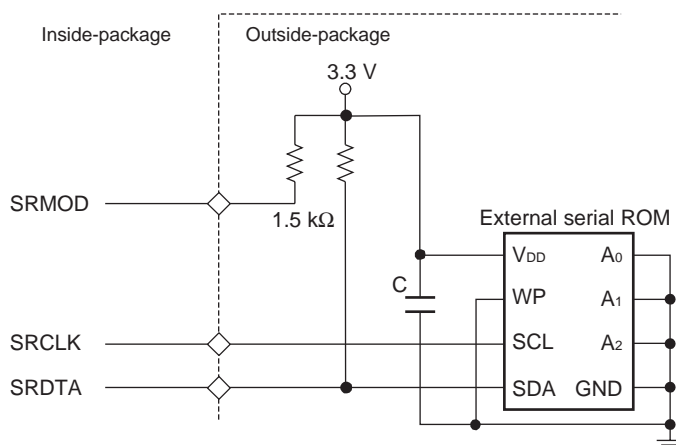
In using these crystals, contact KDS or NDK to get the specification on external components to be used in conjunction with the crystal.

KDS's home page: <http://www.kdsj.co.jp>

NDK's home page: <http://www.ndk-j.co.jp>

★ 2.5 External Serial ROM Connection

Figure 2-4. External Serial ROM Connection



These pins for external serial ROM can be opened, when serial ROM is not necessary on board.

3. ELECTRICAL SPECIFICATIONS

3.1 Buffer List

- 3 V input buffer with pull down resistor
NTEST1, TEST, SRMOD, NANDTEST, SMC, AMC, TEB
- 3 V PCI I_{OL} = 9 mA 3-state output buffer
PPON(5:1), SRCLK
- 3 V I_{OL} = 9 mA bi-directional buffer
LEGC, SRDTA
- 3 V I_{OL} = 9 mA bi-directional buffer with enable (OR type)
OCI(5:1)
- 3 V oscillator interface
XT1/SCLK, XT2
- 5 V input buffer
VBBRST0, VCCRST0
- 5 V I_{OL} = 12 mA N-ch open drain buffer
SMI0, PME0, INTA0, INTB0, INTC0, SERR0
- 5 V PCI input buffer with enable (OR type)
PCLK, GNT0, IDSEL
- 5 V PCI I_{OL} = 12 mA 3-state output buffer
REQ0
- 5 V PCI I_{OL} = 9 mA bi-directional buffer with input enable (OR-type)
AD(31:0), CBE(3:0)0, PAR, FRAME0, IRDY0, TRDY0, STOP0, DEVSEL0, PERR0, CRUN0
- USB interface, analog signal
DP(5:1), DM(5:1), RSDP(5:1), RSDM(5:1), RREF

Above, “5 V” refers to a 3 V buffer with 5 V tolerant circuit. Therefore, it is possible to have a 5 V connection for an external bus, but the output level will be only up to 3 V, which is the V_{DD} voltage. Similarly, “5 V PCI” above refers to a PCI buffer that has a 5 V tolerant circuit, which meets the 3 V PCI standard; it does not refer to a PCI buffer that meets the 5 V PCI standard.

3.2 Terminology

Terms Used in Absolute Maximum Ratings

| Parameter | Symbol | Meaning |
|-------------------------------|---|---|
| Power supply voltage | V_{DD} , AV_{DD} , V_{DD_PCI} | Indicates voltage range within which damage or reduced reliability will not result when power is applied to a V_{DD} pin. |
| Input voltage | V_I | Indicates voltage range within which damage or reduced reliability will not result when power is applied to an input pin. |
| Output voltage | V_O | Indicates voltage range within which damage or reduced reliability will not result when power is applied to an output pin. |
| Operating ambient temperature | T_A | Indicates the ambient temperature range for normal logic operations. |
| Storage temperature | T_{stg} | Indicates the element temperature range within which damage or reduced reliability will not result while no voltage or current are applied to the device. |

Terms Used in Recommended Operating Range

| Parameter | Symbol | Meaning |
|--------------------------|---|---|
| Power supply voltage | V_{DD} , AV_{DD} , V_{DD_PCI} | Indicates the voltage range for normal logic operations occur when $V_{SS} = 0$ V. |
| High-level input voltage | V_{IH} | Indicates the voltage, which is applied to the input pins of the device, is the voltage indicates that the high level states for normal operation of the input buffer. * If a voltage that is equal to or greater than the "Min." value is applied, the input voltage is guaranteed as high level voltage. |
| Low-level input voltage | V_{IL} | Indicates the voltage, which is applied to the input pins of the device, is the voltage indicates that the low level states for normal operation of the input buffer. * If a voltage that is equal to or lesser than the "Max." value is applied, the input voltage is guaranteed as low level voltage. |

Terms Used in DC Characteristics

| Parameter | Symbol | Meaning |
|----------------------------------|----------|--|
| Off-state output leakage current | I_{OZ} | Indicates the current that flows from the power supply pins when the rated power supply voltage is applied when a 3-state output has high impedance. |
| Output short circuit current | I_{OS} | Indicates the current that flows when the output pin is shorted (to GND pins) when output is at high-level. |
| Input leakage current | I_I | Indicates the current that flows when the input voltage is supplied to the input pin. |
| Low-level output current | I_{OL} | Indicates the current that flows to the output pins when the rated low-level output voltage is being applied. |
| High-level output current | I_{OH} | Indicates the current that flows from the output pins when the rated high-level output voltage is being applied. |

3.3 Electrical Specifications

Absolute Maximum Ratings

| Parameter | Symbol | Condition | Rating | Unit |
|-------------------------------|---------------|---|--------------|------|
| Power supply voltage | V_{DD} | | −0.5 to +4.6 | V |
| | AV_{DD} | | −0.5 to +4.6 | V |
| | V_{DD_PCI} | | −0.5 to +6.0 | V |
| Input voltage, 5 V buffer | V_I | $3.0\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ $V_I < V_{DD} + 3.0\text{ V}$ | −0.5 to +6.6 | V |
| Input voltage, 3.3 V buffer | V_I | $3.0\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ $V_I < V_{DD} + 0.5\text{ V}$ | −0.5 to +4.6 | V |
| Output voltage, 5 V buffer | V_O | $3.0\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ $V_O < V_{DD} + 3.0\text{ V}$ | −0.5 to +6.6 | V |
| Output voltage, 3.3 V buffer | V_O | $3.0\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ $V_O < V_{DD} + 0.5\text{ V}$ | −0.5 to +4.6 | V |
| Operating ambient temperature | T_A | | 0 to +70 | °C |
| Storage temperature | T_{stg} | | −65 to +150 | °C |

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameters. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Recommended Operating Ranges

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|--------------------------------|---------------|--------------|------|------|----------|------|
| Operating voltage | V_{DD} | | 3.0 | 3.3 | 3.6 | V |
| | AV_{DD} | | 3.0 | 3.3 | 3.6 | V |
| | V_{DD_PCI} | In 3.3 V PCI | 3.0 | 3.3 | 3.6 | V |
| | | In 5 V PCI | 4.75 | 5.0 | 5.25 | V |
| High-level input voltage | V_{IH} | | | | | |
| 3.3 V high-level input voltage | | | 2.0 | | V_{DD} | V |
| 5.0 V high-level input voltage | | | 2.0 | | 5.5 | V |
| Low-level input voltage | V_{IL} | | | | | |
| 3.3 V low-level input voltage | | | 0 | | 0.8 | V |
| 5.0 V low-level input voltage | | | 0 | | 0.8 | V |

DC Characteristics ($V_{DD} = 3.0$ to 3.6 V, $T_A = 0$ to $+70^\circ\text{C}$)

Control pin block

| Parameter | Symbol | Condition | Min. | Max. | Unit |
|---------------------------------|--------------------------|----------------------------|------|----------|---------------|
| Off-state output current | I_{OZ} | $V_O = V_{DD}$ or V_{SS} | | ± 10 | μA |
| Output short circuit current | I_{OS} ^{Note} | | | -250 | mA |
| Low-level output current | I_{OL} | | | | |
| 3.3 V low-level output current | | $V_{OL} = 0.4$ V | 9.0 | | mA |
| 3.3 V low-level output current | | $V_{OL} = 0.4$ V | 3.0 | | mA |
| 5.0 V low-level output current | | $V_{OL} = 0.4$ V | 12.0 | | mA |
| 5.0 V low-level output current | | $V_{OL} = 0.4$ V | 6.0 | | mA |
| High-level output current | I_{OH} | | | | |
| 3.3 V high-level output current | | $V_{OH} = 2.4$ V | -9.0 | | mA |
| 3.3 V high-level output current | | $V_{OH} = 2.4$ V | -3.0 | | mA |
| 5.0 V high-level output current | | $V_{OH} = 2.4$ V | -2.0 | | mA |
| 5.0 V high-level output current | | $V_{OH} = 2.4$ V | -2.0 | | mA |
| Input leakage current | I_I | | | | |
| 3.3 V buffer | | $V_I = V_{DD}$ or V_{SS} | | ± 10 | μA |
| 3.3 V buffer with 50 kΩ PD | | $V_I = V_{DD}$ | | 191 | μA |
| 5.0 V buffer | | $V_I = V_{DD}$ or V_{SS} | | ± 10 | μA |

Note The output short circuit time is one second or less and is only for one pin on the LSI.

PCI interface block

| Parameter | Symbol | Condition | Min. | Max. | Unit |
|----------------------------|-----------|---|------|------|---------------|
| High-level input voltage | V_{IH} | | 2.0 | 5.25 | V |
| Low-level input voltage | V_{IL} | | 0 | 0.8 | V |
| Low-level output current | I_{OL} | $V_{OL} = 0.4$ V | 12.0 | | mA |
| High-level output current | I_{OH} | $V_{OH} = 2.4$ V | -2.0 | | mA |
| Input high leakage current | I_{IH} | $V_{IN} = 2.7$ V | | 70 | μA |
| Input low leakage current | I_{IL} | $V_{IN} = 0.5$ V | | -70 | μA |
| PME0 leakage current | I_{OFF} | $V_O < 3.6$ V V_{CC} off or floating | | 1 | μA |

USB interface block

| Parameter | Symbol | Conditions | Min. | Max. | Unit |
|---|-------------------------|-------------------------------------|-------|-------|------|
| Serial resistor between DP (DM) and RSDP (RSDM) | R _S | | 35.64 | 36.36 | Ω |
| Output pin impedance | Z _{HSDRV} | Includes R _S resistor | 40.5 | 49.5 | Ω |
| Input Levels for Low-/full-speed: | | | | | |
| High-level input voltage (drive) | V _{IH} | | 2.0 | | V |
| High-level input voltage (floating) | V _{IHZ} | | 2.7 | 3.6 | V |
| Low-level input voltage | V _{IL} | | | 0.8 | V |
| Differential input sensitivity | V _{DI} | (D+) – (D–) | 0.2 | | V |
| Differential common mode range | V _{CM} | Includes V _{DI} range | 0.8 | 2.5 | V |
| Output Levels for Low-/full-speed: | | | | | |
| High-level output voltage | V _{OH} | R _L of 14.25 kΩ to GND | 2.8 | 3.6 | V |
| Low-level output voltage | V _{OL} | R _L of 1.425 kΩ to 3.6 V | 0.0 | 0.3 | V |
| SE1 | V _{OSE1} | | 0.8 | | V |
| Output signal crossover point voltage | V _{CRS} | | 1.3 | 2.0 | V |
| Input Levels for High-speed: | | | | | |
| High-speed squelch detection threshold (differential signal) | V _{HSSQ} | | 100 | 150 | mV |
| High-speed disconnect detection threshold (differential signal) | V _{HSDSC} | | 525 | 625 | mV |
| High-speed data signaling common mode voltage range | V _{HSCM} | | –50 | +500 | mV |
| High-speed differential input signaling level | See Figure 3-4 . | | | | |
| Output Levels for High-speed: | | | | | |
| High-speed idle state | V _{HSOI} | | –10 | +10 | mV |
| High-speed data signaling high | V _{HSOH} | | 360 | 440 | mV |
| High-speed data signaling low | V _{HSOL} | | –10 | +10 | mV |
| Chirp J level (differential signal) | V _{CHIRPJ} | | 700 | 1100 | mV |
| Chirp K level (differential signal) | V _{CHIRPK} | | –900 | –500 | mV |

Figure 3-1. Differential Input Sensitivity Range for Low-/full-speed

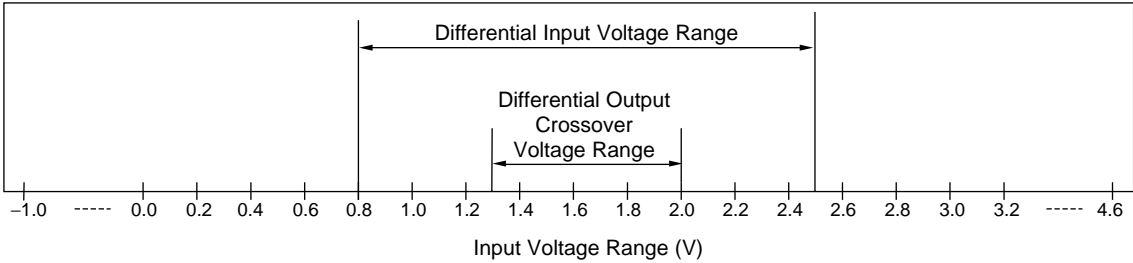


Figure 3-2. Full-speed Buffer V_{OH}/I_{OH} Characteristics for High-speed Capable Transceiver

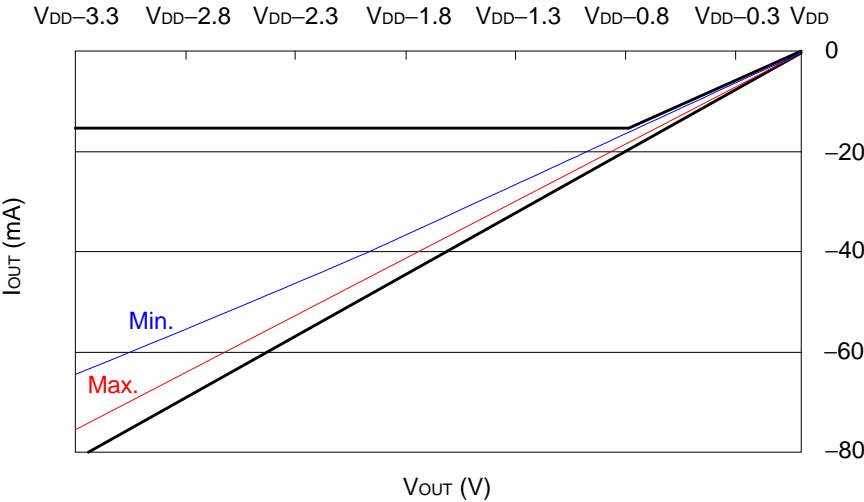


Figure 3-3. Full-speed Buffer V_{OL}/I_{OL} Characteristics for High-speed Capable Transceiver

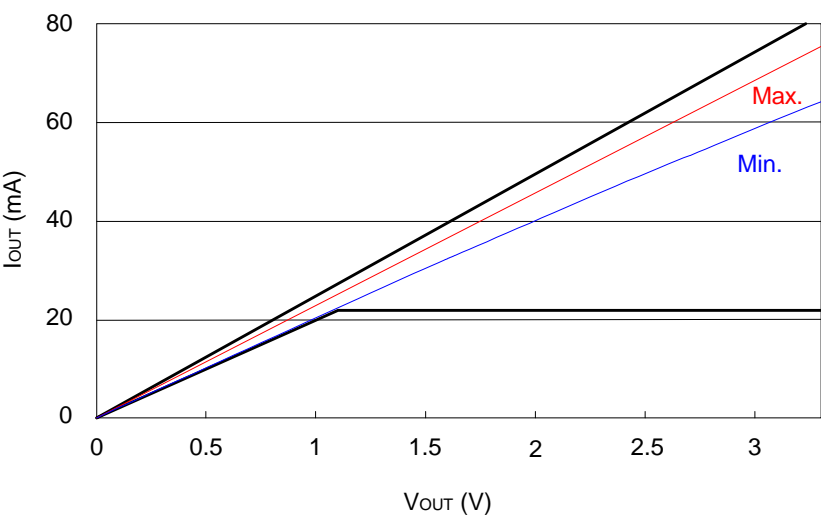


Figure 3-4. Receiver Sensitivity for Transceiver at DP/DM

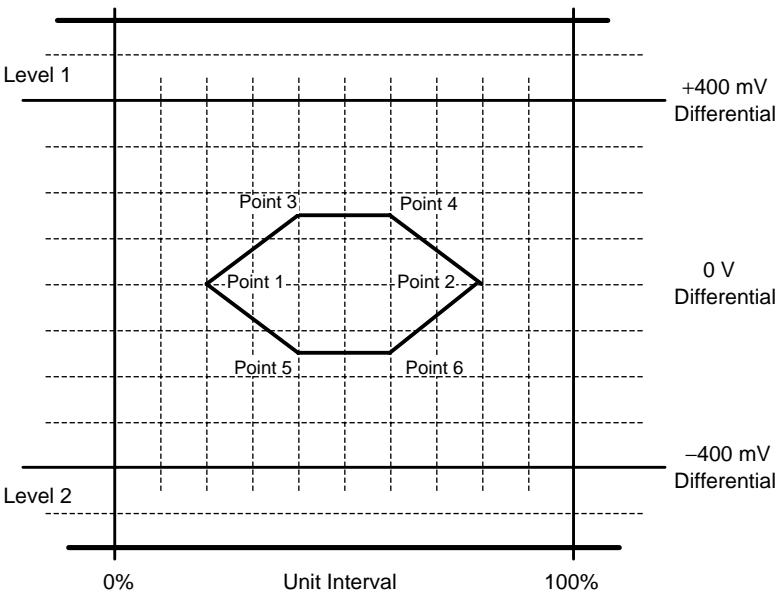
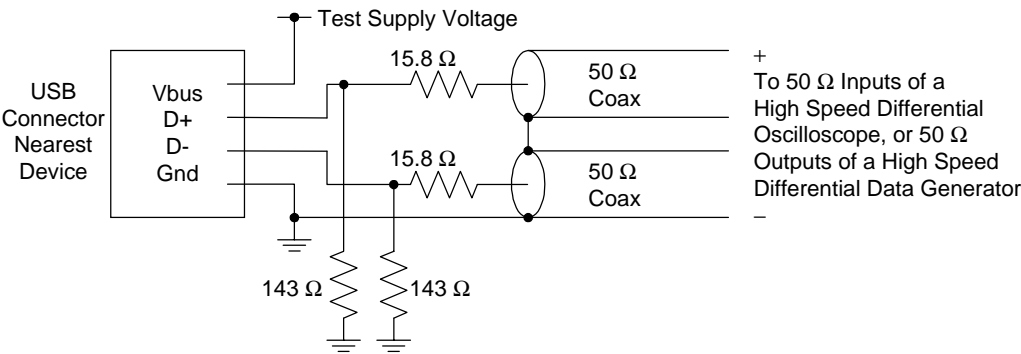


Figure 3-5. Receiver Measurement Fixtures



Pin capacitance

| Parameter | Symbol | Condition | Min. | Max. | Unit |
|---------------------------------|--------------------|---|------|------|------|
| Input capacitance | C _I | V _{DD} = 0 V, T _A = 25°C f _c = 1 MHz Unmeasured pins returned to 0 V | 6 | 8 | pF |
| Output capacitance | C _O | | 10 | 12 | pF |
| I/O capacitance | C _{IO} | | 10 | 12 | pF |
| PCI input pin capacitance | C _{in} | | | 8 | pF |
| PCI clock input pin capacitance | C _{clk} | | 6 | 8 | pF |
| PCI IDSEL input pin capacitance | C _{IDSEL} | | | 8 | pF |

Power consumption

| Parameter | Symbol | Condition | Typ. (30 MHz X'tal) | Typ. (48 MHz OSC) | Unit |
|-------------------|--------|---|------------------------|----------------------|----------|
| Power Consumption | PWD0-0 | Device state = D0, All the ports does not connect to any function, and each OHCI controller is under UsbSuspend and EHCI controller is stopped. ^{Note1} | 31.4 | 10.4 | mA |
| | PWD0-2 | The power consumption under the state without suspend. Device state = D0, The number of active ports is 2. ^{Note2} Full- or low-speed device(s) is (are) on the port. High-speed device(s) is (are) on the port. | 53.1 204.6 | 31.9 204.2 | mA mA |
| | PWD0-3 | The power consumption under the state without suspend. Device state = D0, The number of active ports is 3. ^{Note2} Full- or low-speed device(s) is (are) on the port. High-speed device(s) is (are) on the port. | 55.3 253.8 | 34.2 255.5 | mA mA |
| | PWD0-4 | The power consumption under the state without suspend. Device state = D0, The number of active ports is 4. ^{Note2} Full- or low-speed device(s) is (are) on the port. High-speed device(s) is (are) on the port. | 57.4 301.6 | 36.7 300.1 | mA mA |
| | PWD0-5 | The power consumption under the state without suspend. Device state = D0, The number of active ports is 5. ^{Note2} Full- or low-speed device(s) is (are) on the port. High-speed device(s) is (are) on the port. | 59.8 349.1 | 38.8 345.2 | mA mA |
| | PWD0_C | The power consumption under suspend state during PCI clock is stopped by CRUN0. Device state = D0. | 30.5 | 10.4 | mA |
| | PWD1 | Device state = D1, Analog PLL output is stopped. ^{Note 3} | 7.7 | 10.4 | mA |
| | PWD2 | Device state = D2, Analog PLL output is stopped. ^{Note 3} | 7.7 | 10.4 | mA |
| | PWD3H | Device state = D3 _{hot} , VCCRST0 = High, Analog PLL output is stopped. ^{Note 3} | 7.7 | 10.4 | mA |
| | PWD3C | Device state = D3 _{cold} , VCCRST0 = Low. ^{Note 4} | 0.03 | 3.81 | mA |

Notes 1. When any device is not connected to all the ports of HC, the power consumption for HC does not depend on the number of active ports.

2. The number of active ports is set by the value of Port No Field in PCI configuration space EXT register.

3. This is the case when PCI bus state is B0.

4. This is the case when PCI bus state is B3.

Remark These are estimated value on Windows™ XP environment.

System clock ratings

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|------------------|-------------------|------------------|-------------|------|-------------|------|
| Clock frequency | f _{CLK} | X'tal | −500 ppm | 30 | +500 ppm | MHz |
| | | Oscillator block | −500 ppm | 48 | +500 ppm | MHz |
| Clock duty cycle | t _{DUTY} | | 40 | 50 | 60 | % |

- Remarks** 1. Recommended accuracy of clock frequency is ± 100 ppm.
2. Required accuracy of X'tal or oscillator block is including initial frequency accuracy, the spread of X'tal capacitor loading, supply voltage, temperature, and aging, etc.

AC Characteristics (V_{DD} = 3.0 to 3.6 V, T_A = 0 to +70°C)

PCI interface block

| Parameter | Symbol | Condition | Min. | Max. | Unit |
|--|------------------------|--|------|------|-------|
| PCI clock cycle time | t _{cyc} | | 30 | | ns |
| PCI clock pulse, high-level width | t _{high} | | 11 | | ns |
| PCI clock pulse, low-level width | t _{low} | | 11 | | ns |
| PCI clock, rise slew rate | S _{cr} | 0.2V _{DD} to 0.6V _{DD} | 1 | 4 | V/ns |
| PCI clock, fall slew rate | S _{cf} | 0.2V _{DD} to 0.6V _{DD} | 1 | 4 | V/ns |
| PCI reset active time (vs. power supply stability) | t _{rst} | | 1 | | ms |
| PCI reset active time (vs. CLK start) | t _{rst-clk} | | 100 | | μs |
| Output float delay time (vs. RST0↓) | t _{rst-off} | | | 40 | ns |
| PCI reset rise slew rate | S _{rr} | | 50 | | mV/ns |
| PCI bus signal output time (vs. PCLK↑) | t _{val} | | 2 | 11 | ns |
| PCI point-to-point signal output time (vs. PCLK↑) | t _{val} (ptp) | REQ0 | 2 | 12 | ns |
| Output delay time (vs. PCLK↑) | t _{on} | | 2 | | ns |
| Output float delay time (vs. PCLK↑) | t _{off} | | | 28 | ns |
| Input setup time (vs. PCLK↑) | t _{su} | | 7 | | ns |
| Point-to-point input setup time (vs. PCLK↑) | t _{su} (ptp) | GNT0 | 10 | | ns |
| Input hold time | t _h | | 0 | | ns |

USB interface block

(1/2)

| Parameter | Symbol | Conditions | Min. | Max. | Unit |
|---|---------------|---|---------|---------|------|
| Low-speed Source Electrical Characteristics | | | | | |
| Rise time (10 to 90%) | t_{LR} | $C_L = 200 \text{ to } 600 \text{ pF}$, $R_S = 36 \Omega$ | 75 | 300 | ns |
| Fall time (90 to 10%) | t_{LF} | $C_L = 200 \text{ to } 600 \text{ pF}$, $R_S = 36 \Omega$ | 75 | 300 | ns |
| Differential rise and fall time matching | t_{LRFM} | (t_{LR}/t_{LF}) | 80 | 125 | % |
| Low-speed data rate | $t_{LDRATHS}$ | Average bit rate | 1.49925 | 1.50075 | Mbps |
| Source jitter total (including frequency tolerance): | | | | | |
| To next transition | t_{DDJ1} | | -25 | +25 | ns |
| For paired transitions | t_{DDJ2} | | -14 | +14 | ns |
| Source jitter for differential transition to SE0 transition | t_{LDEOP} | | -40 | +100 | ns |
| Receiver jitter: | | | | | |
| To next transition | t_{UJR1} | | -152 | +152 | ns |
| For paired transitions | t_{UJR2} | | -200 | +200 | ns |
| Source SE0 interval of EOP | t_{LEOPT} | | 1.25 | 1.50 | μs |
| Receiver SE0 interval of EOP | t_{LEOPR} | | 670 | | ns |
| Width of SE0 interval during differential transition | t_{FST} | | | 210 | ns |
| Full-speed Source Electrical Characteristics | | | | | |
| Rise time (10 to 90%) | t_{FR} | $C_L = 50 \text{ pF}$, $R_S = 36 \Omega$ | 4 | 20 | ns |
| Fall time (90 to 10%) | t_{FF} | $C_L = 50 \text{ pF}$, $R_S = 36 \Omega$ | 4 | 20 | ns |
| Differential rise and fall time matching | t_{FRFM} | (t_{FR}/t_{FF}) | 90 | 111.11 | % |
| Full-speed data rate | $t_{FDRATHS}$ | Average bit rate | 11.9940 | 12.0060 | Mbps |
| Frame interval | t_{FRAME} | | 0.9995 | 1.0005 | ms |
| Consecutive frame interval jitter | t_{RFI} | No clock adjustment | | 42 | ns |
| Source jitter total (including frequency tolerance): | | | | | |
| To next transition | t_{DJ1} | | -3.5 | +3.5 | ns |
| For paired transitions | t_{DJ2} | | -4.0 | +4.0 | ns |
| Source jitter for differential transition to SE0 transition | t_{FDEOP} | | -2 | +5 | ns |
| Receiver jitter: | | | | | |
| To next transition | t_{JR1} | | -18.5 | +18.5 | ns |
| For paired transitions | t_{JR2} | | -9 | +9 | ns |
| Source SE0 interval of EOP | t_{FEOPT} | | 160 | 175 | ns |
| Receiver SE0 interval of EOP | t_{FEOPR} | | 82 | | ns |
| Width of SE0 interval during differential transition | t_{FST} | | | 14 | ns |

(2/2)

| Parameter | Symbol | Conditions | Min. | Max. | Unit |
|---|-----------------------|------------|----------|--------------|-----------|
| High-speed Source Electrical Characteristics | | | | | |
| Rise time (10 to 90%) | t _{HSR} | | 500 | | ps |
| Fall time (90 to 10%) | t _{HSF} | | 500 | | ps |
| Driver waveform | See Figure 3-6. | | | | |
| High-speed data rate | t _{HSDRAT} | | 479.760 | 480.240 | Mbps |
| Microframe interval | t _{HSFRAM} | | 124.9375 | 125.0625 | μs |
| Consecutive microframe interval difference | t _{HSRFI} | | | 4 high-speed | Bit times |
| Data source jitter | See Figure 3-6. | | | | |
| Receiver jitter tolerance | See Figure 3-4. | | | | |
| Hub Event Timings | | | | | |
| Time to detect a downstream facing port connect event | t _{DCNN} | | 2.5 | 2000 | μs |
| Time to detect a disconnect event at a hub's downstream facing port | t _{DDIS} | | 2.0 | 2.5 | μs |
| Duration of driving resume to a downstream port | t _{DRSMDN} | Nominal | 20 | | ms |
| Time from detecting downstream resume to rebroadcast | t _{URSM} | | | 1.0 | ms |
| Inter-packet delay for packets traveling in same direction for high-speed | t _{HSIPDSD} | | 88 | | Bit times |
| Inter-packet delay for packets traveling in opposite direction for high-speed | t _{HSIPDOD} | | 8 | | Bit times |
| Inter-packet delay for root hub response for high-speed | t _{HSRSPID1} | | | 192 | Bit times |
| Time for which a Chirp J or Chirp K must be continuously detected during reset handshake | t _{FILT} | | 2.5 | | μs |
| Time after end of device Chirp K by which hub must start driving first Chirp K | t _{WTDCH} | | | 100 | μs |
| Time for which each individual Chirp J or Chirp K in the chirp sequence is driven downstream during reset | t _{DCHBIT} | | 40 | 60 | μs |
| Time before end of reset by which a hub must end its downstream chirp sequence | t _{DCHSE0} | | 100 | 500 | μs |

Figure 3-6. Transmit Waveform for Transceiver at DP/DM

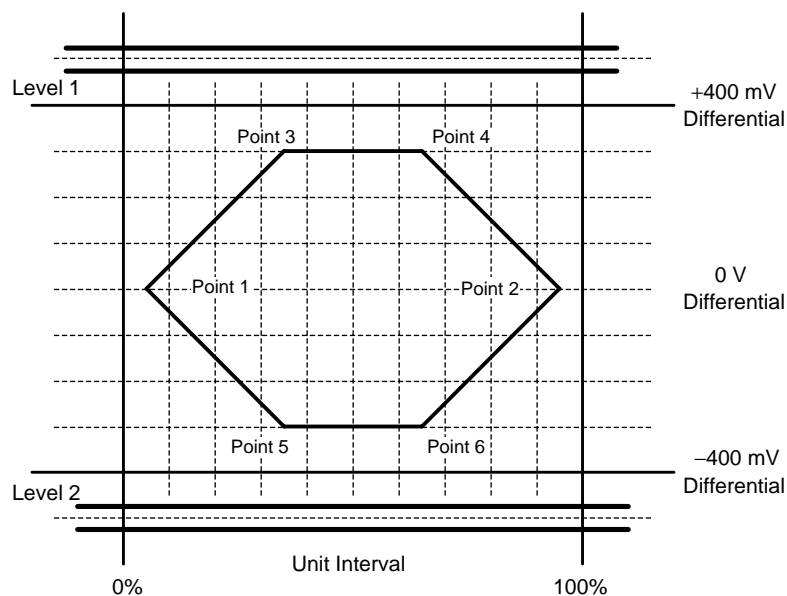
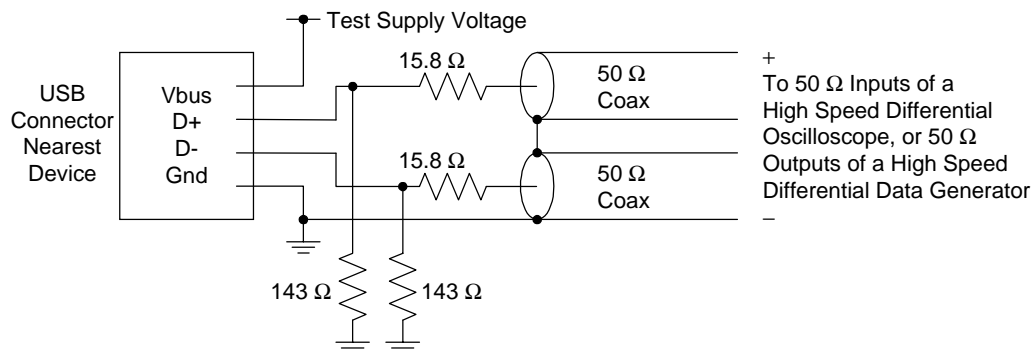
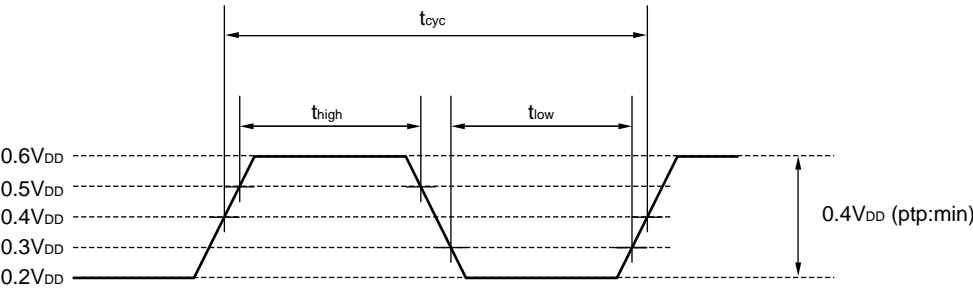


Figure 3-7. Transmitter Measurement Fixtures

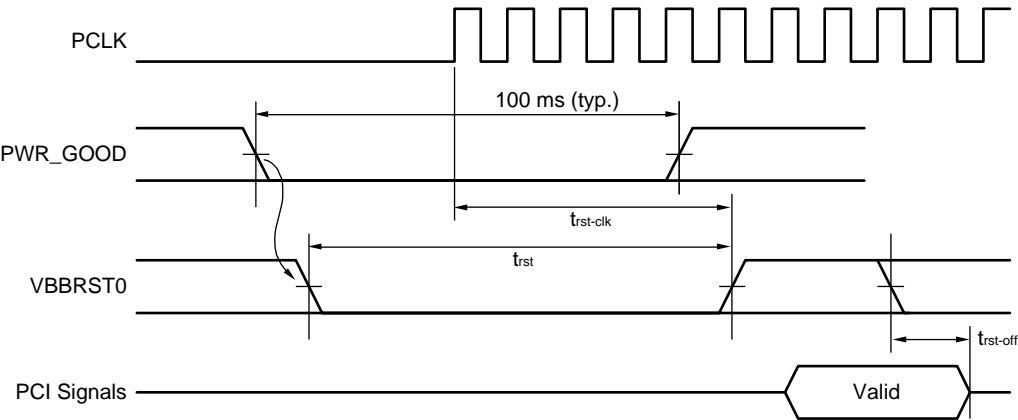


3.4 Timing Diagram

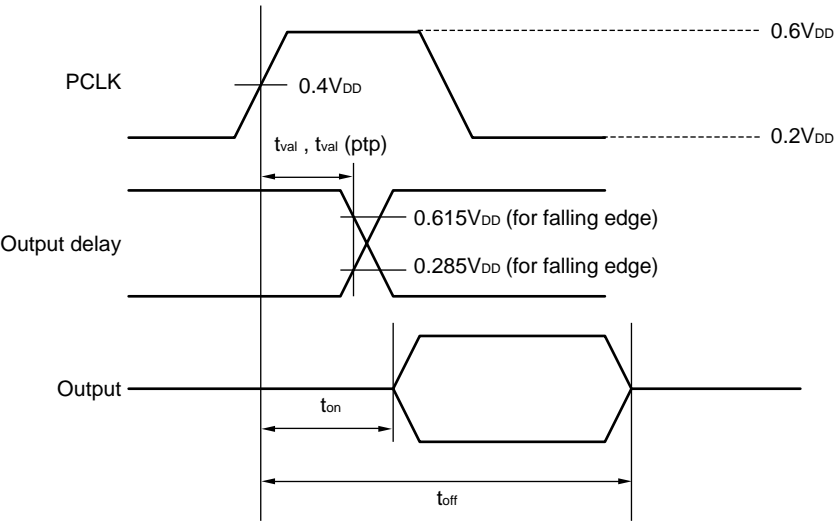
PCI clock



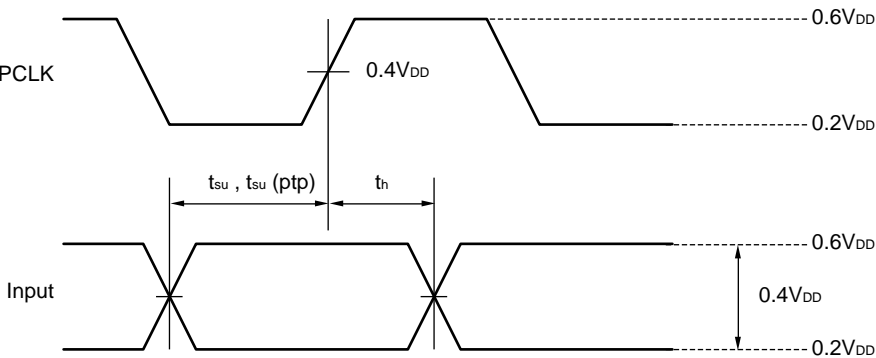
PCI reset



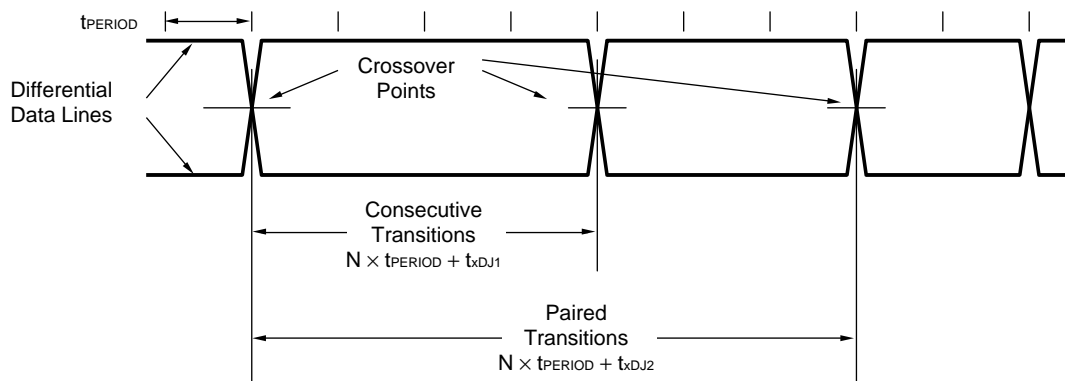
PCI output timing measurement condition



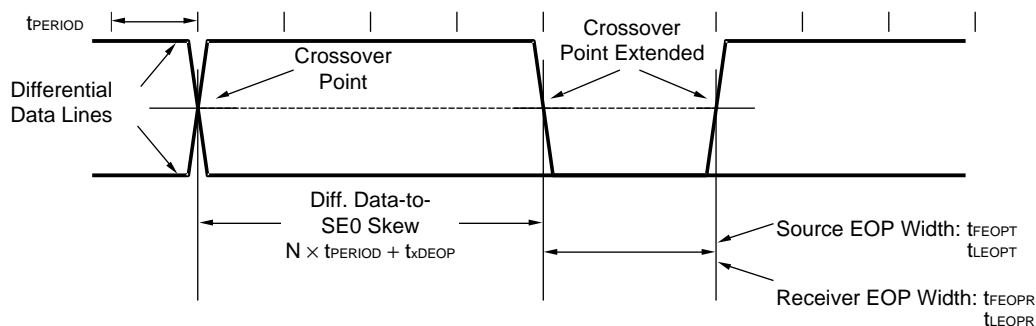
PCI input timing measurement condition



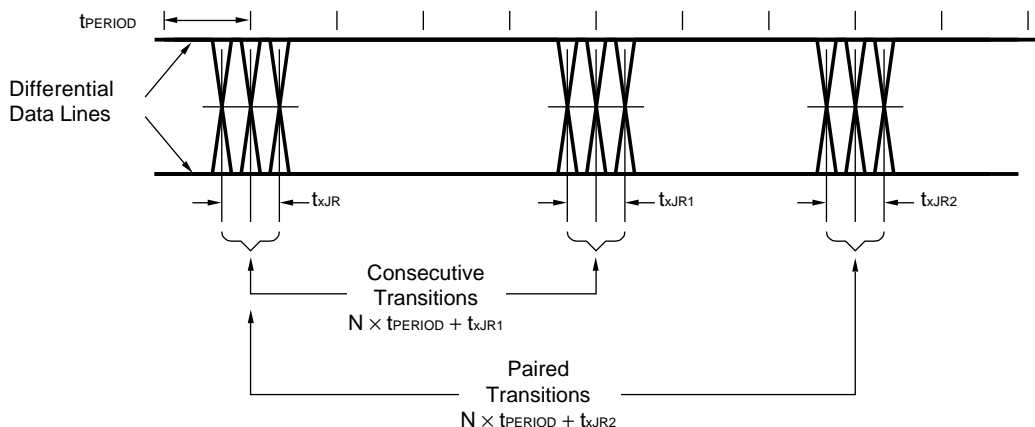
USB differential data jitter for full-speed



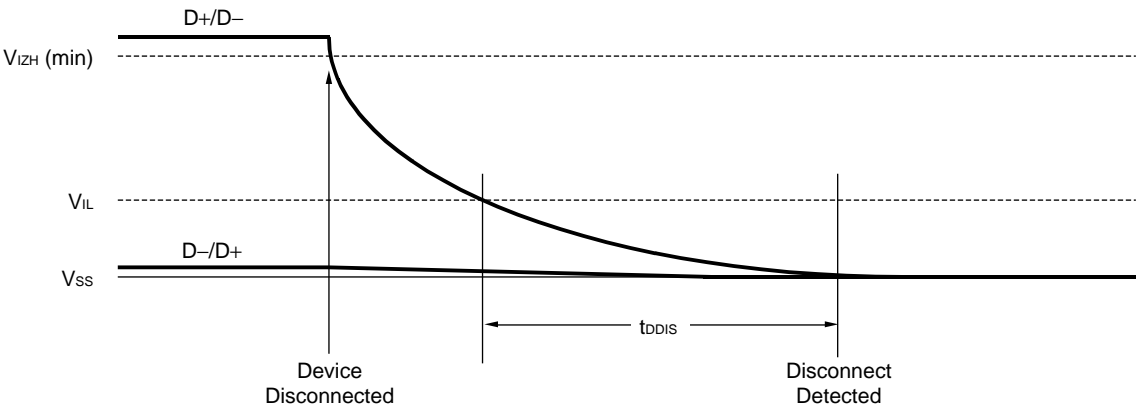
USB differential-to-EOP transition skew and EOP width for low-/full-speed



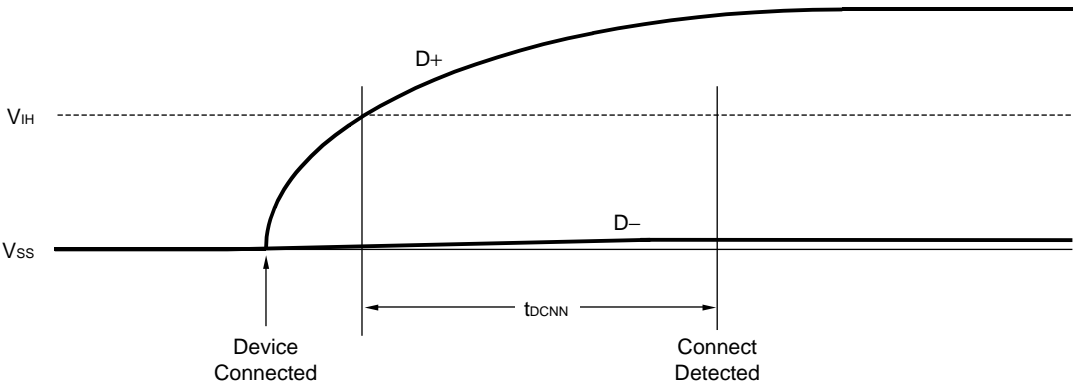
USB receiver jitter tolerance for low-/full-speed



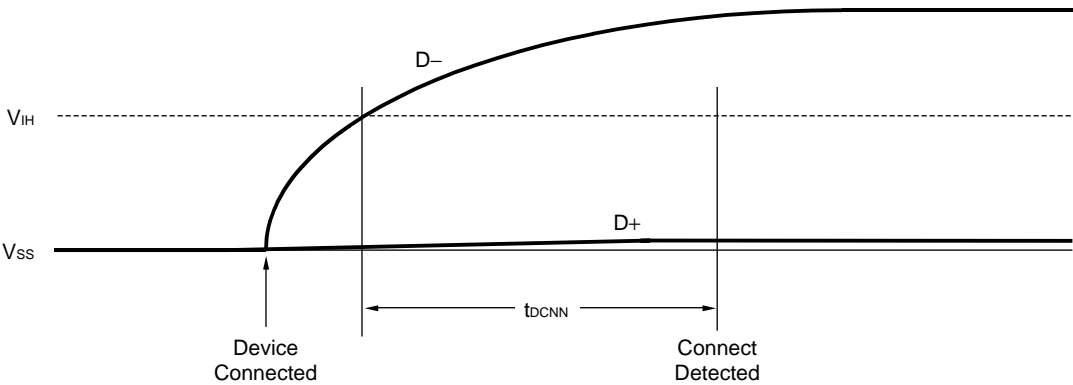
Low-/full-speed disconnect detection



Full-/high-speed device connect detection

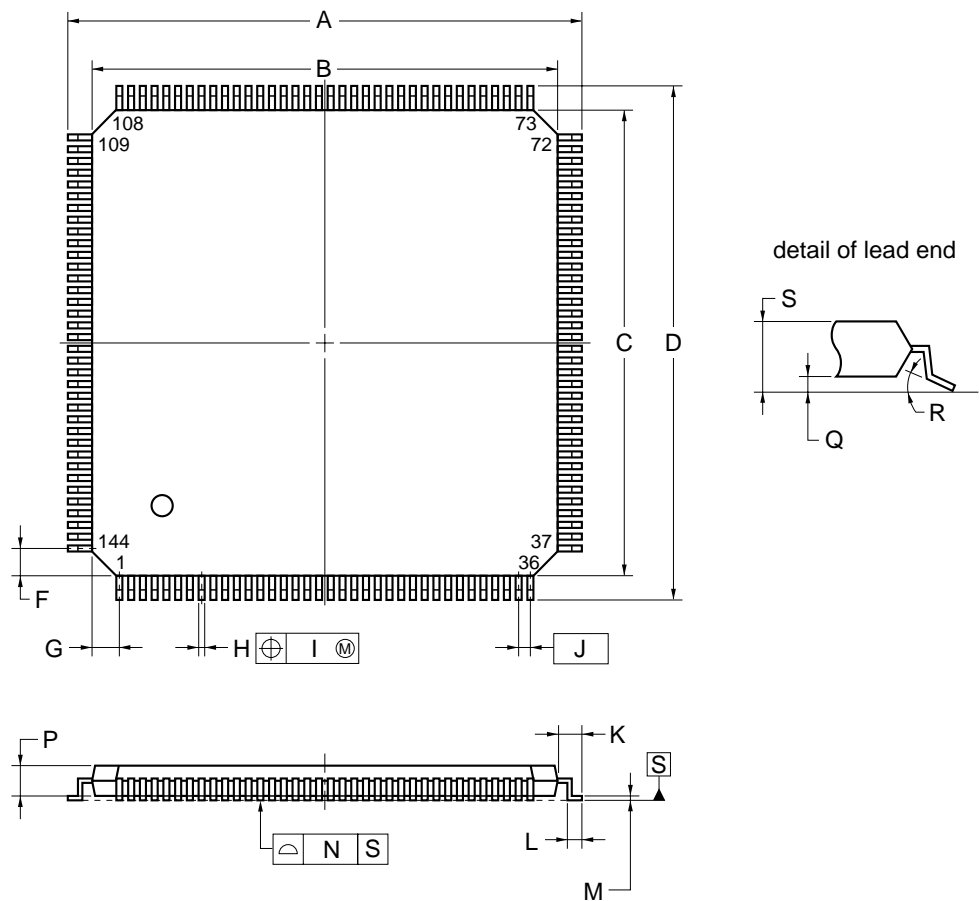


Low-speed device connect detection



4. PACKAGE DRAWINGS

144-PIN PLASTIC LQFP (FINE PITCH) (20x20)



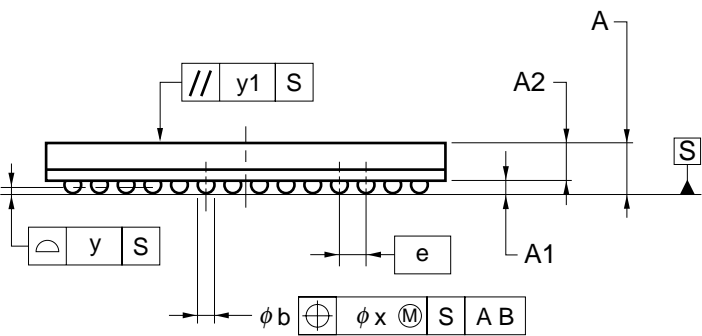
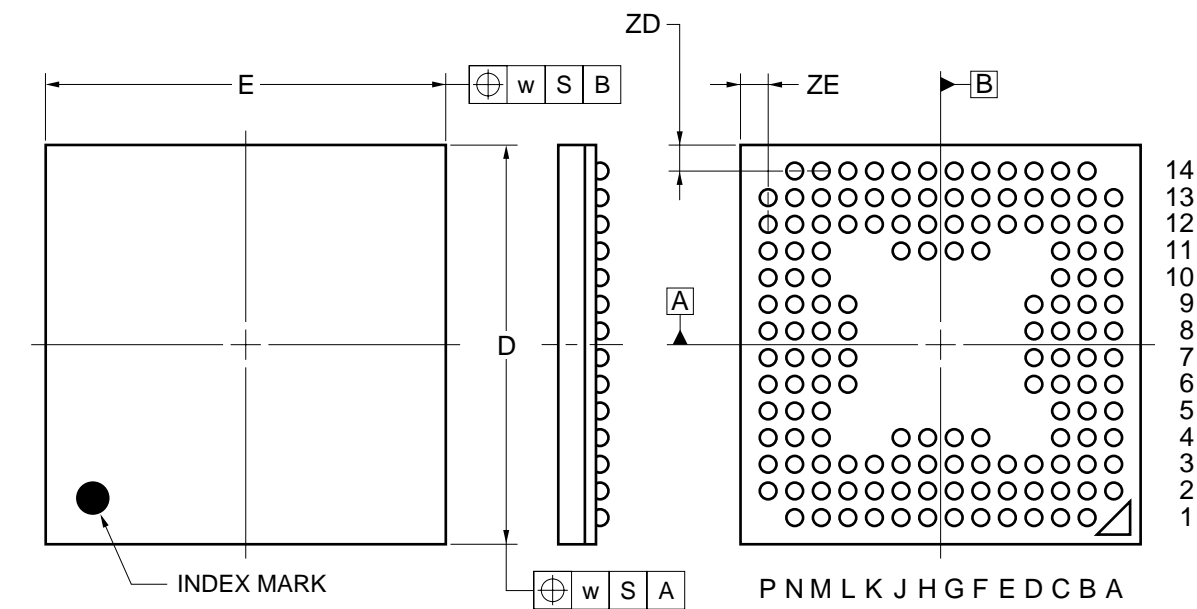
NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS |
|------|--|
| A | 22.0±0.2 |
| B | 20.0±0.2 |
| C | 20.0±0.2 |
| D | 22.0±0.2 |
| F | 1.25 |
| G | 1.25 |
| H | 0.22±0.05 |
| I | 0.08 |
| J | 0.5 (T.P.) |
| K | 1.0±0.2 |
| L | 0.5±0.2 |
| M | 0.17 ^{+0.03} _{-0.07} |
| N | 0.08 |
| P | 1.4 |
| Q | 0.10±0.05 |
| R | 3°+4° -3° |
| S | 1.5±0.1 |

S144GJ-50-UEN

144-PIN PLASTIC FBGA (12x12)



| ITEM | MILLIMETERS |
|------|--|
| D | 12.00±0.10 |
| E | 12.00±0.10 |
| w | 0.20 |
| A | 1.48±0.10 |
| A1 | 0.35±0.06 |
| A2 | 1.13 |
| e | 0.80 |
| b | 0.50 ^{+0.05} _{-0.10} |
| x | 0.08 |
| y | 0.10 |
| y1 | 0.20 |
| ZD | 0.80 |
| ZE | 0.80 |

P144F1-80-EA8

5. RECOMMENDED SOLDERING CONDITIONS

The μPD720101 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (<http://www.necel.com/pkg/en/mount/index.html>)

μPD720101GJ-UEN: 144-pin plastic LQFP (Fine pitch) (20 × 20)

| Soldering Method | Soldering Conditions | Symbol |
|------------------|--|------------|
| Infrared reflow | Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Three times or less Exposure limit: 3 days ^{Note} (after that, prebake at 125°C for 10 hours) | IR35-103-3 |
| Partial heating | Pin temperature: 300°C max., Time: 3 seconds max. (per pin row) | — |

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

μPD720101F1-EA8: 144-pin plastic FBGA (12 × 12)

| Soldering Method | Soldering Conditions | Symbol |
|------------------|--|------------|
| Infrared reflow | Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Three times or less Exposure limit: 7 days ^{Note} (after that, prebake at 125°C for 10 hours) | IR35-107-3 |

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

Purchase of NEC Electronics I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

USB logo is a trademark of USB Implementers Forum, Inc.

Windows is either a registered trademark or a trademark of Microsoft Corporation in the United States and/or other countries.

- **The information in this document is current as of June, 2004. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC Electronics data sheets or data books, etc., for the most up-to-date specifications of NEC Electronics products. Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.**
- No part of this document may be copied or reproduced in any form or by any means without the prior written consent of NEC Electronics. NEC Electronics assumes no responsibility for any errors that may appear in this document.
- NEC Electronics does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from the use of NEC Electronics products listed in this document or any other liability arising from the use of such products. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Electronics or others.
- Descriptions of circuits, software and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software and information in the design of a customer's equipment shall be done under the full responsibility of the customer. NEC Electronics assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.
- While NEC Electronics endeavors to enhance the quality, reliability and safety of NEC Electronics products, customers agree and acknowledge that the possibility of defects thereof cannot be eliminated entirely. To minimize risks of damage to property or injury (including death) to persons arising from defects in NEC Electronics products, customers must incorporate sufficient safety measures in their design, such as redundancy, fire-containment and anti-failure features.
- NEC Electronics products are classified into the following three quality grades: "Standard", "Special" and "Specific".
 The "Specific" quality grade applies only to NEC Electronics products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of an NEC Electronics product depend on its quality grade, as indicated below. Customers must check the quality grade of each NEC Electronics product before using it in a particular application.
 "Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots.
 "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support).
 "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.

The quality grade of NEC Electronics products is "Standard" unless otherwise expressly specified in NEC Electronics data sheets or data books, etc. If customers wish to use NEC Electronics products in applications not intended by NEC Electronics, they must contact an NEC Electronics sales representative in advance to determine NEC Electronics' willingness to support a given application.

(Note)

- (1) "NEC Electronics" as used in this statement means NEC Electronics Corporation and also includes its majority-owned subsidiaries.
- (2) "NEC Electronics products" means any product developed or manufactured by or for NEC Electronics (as defined above).