

DATA SHEET

MOS INTEGRATED CIRCUIT μ PD431000A

1M-BIT CMOS STATIC RAM 128K-WORD BY 8-BIT

Description

The μ PD431000A is a high speed, low power, and 1,048,576 bits (131,072 words by 8 bits) CMOS static RAM.

The μ PD431000A has two chip enable pins (/CE1, CE2) to extend the capacity. And battery backup is available. In addition to this, A and B versions are low voltage operations.

The μ PD431000A is packed in 32-pin PLASTIC DIP, 32-pin PLASTIC SOP and 32-pin PLASTIC TSOP (I) (8 × 13.4 mm) and (8 × 20 mm).

Features

- 131,072 words by 8 bits organization
- Fast access time: 70, 85, 100, 120, 150 ns (MAX.)
- Low voltage operation (A version: Vcc = 3.0 to 5.5 V, B version: Vcc = 2.7 to 5.5 V)
- Operating ambient temperature: T_A = 0 to 70 °C
- Low Vcc data retention: 2.0 V (MIN.)
- Output Enable input for easy application
- Two Chip Enable inputs: /CE1, CE2

Part number	Access time	Operating supply	Operating ambient	Supply current		ent
	ns (MAX.)	voltage V	temperature °C	At operating mA (MAX.)	At standby μA (MAX.)	At data retention μ A (MAX.) ^{Note1}
μPD431000A-xxL	70, 85	4.5 to 5.5	0 to 70	70	100	15
μPD431000A-xxLL					20	3
μPD431000A-Axx	70 ^{Note2} , 100	3.0 to 5.5		35 Note3	13 ^{Note5}	
μPD431000A-Bxx	70 ^{Note2} , 100, 120, 150	2.7 to 5.5		30 Note4	11 Note6	

Notes 1. $T_A \le 40 \ ^{\circ}C$

- **2.** Vcc = 4.5 to 5.5 V
- 3. 70 mA (Vcc > 3.6 V)
- 4. 70 mA (Vcc > 3.3 V)
- **5.** 20 μA (Vcc > 3.6 V)
- **6.** 20 μA (Vcc > 3.3 V)

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Document No. M11657EJDV0DS00 (13th edition) Date Published November 2008 Printed in Japan © NEC Electronics Corporation 1990, 1993, 1995

Ordering Information

(1	I	2)

Part number	Package	Access time	Operating supply	Operating ambient	Remark
		ns (MAX.)	voltage	temperature	
			V	°C	
µPD431000ACZ-70L	32-pin PLASTIC DIP	70	4.5 to 5.5	0 to 70	L version
μPD431000ACZ-85L	(15.24mm (600))	85			
µPD431000ACZ-70LL		70			LL version
μPD431000ACZ-85LL		85			
μPD431000AGW-70L	32-pin PLASTIC SOP	70	4.5 to 5.5		L version
μPD431000AGW-85L	(13.34 mm (525))	85			
μPD431000AGW-70LL		70			LL version
μPD431000AGW-85LL		85			
μPD431000AGW-A10		100	3.0 to 5.5		A version
μPD431000AGW-B12		120	2.7 to 5.5		B version
μPD431000AGW-B15		150			
μPD431000AGZ-70LL-KJH	32-pin PLASTIC TSOP(I)	70	4.5 to 5.5		LL version
μPD431000AGZ-B15-KJH	(8x20) (Normal bent)	150	2.7 to 5.5		B version
μPD431000AGZ-70LL-KKH	32-pin PLASTIC TSOP(I)	70	4.5 to 5.5		LL version
	(8x20) (Reverse bent)				
μPD431000AGU-B10-9JH	32-pin PLASTIC TSOP(I)	100	2.7 to 5.5		B version
μPD431000AGU-B12-9JH	(8x13.4) (Normal bent)	120			
μPD431000AGU-B15-9JH		150			
μPD431000AGU-B10-9KH	32-pin PLASTIC TSOP(I)	100			
	(8x13.4) (Reverse bent)				

Part number	Package	Access time ns (MAX.)	Operating supply voltage V	Operating ambient temperature °C	Remark
μPD431000AGW-70L-A	32-pin PLASTIC SOP	70	4.5 to 5.5	0 to 70	L version
μPD431000AGW-85L-A	(13.34 mm (525))	85			
μPD431000AGW-70LL-A		70			LL version
μPD431000AGW-85LL-A		85			
μPD431000AGW-A10-A		100	3.0 to 5.5		A version
μPD431000AGW-B12-A		120	2.7 to 5.5		B version
μPD431000AGW-B15-A		150			
μPD431000AGZ-70LL-KJH-A	32-pin PLASTIC TSOP(I)	70	4.5 to 5.5		LL version
μPD431000AGZ-B10-KJH-A	(8x20) (Normal bent)	100	2.7 to 5.5		B version
μPD431000AGZ-70LL-KKH-A	32-pin PLASTIC TSOP(I) (8x20) (Reverse bent)	70	4.5 to 5.5		LL version
μPD431000AGU-B10-9JH-A	32-pin PLASTIC TSOP(I)	100	2.7 to 5.5		B version
μPD431000AGU-B12-9JH-A	(8x13.4) (Normal bent)	120			
μPD431000AGU-B15-9JH-A		150			
μΡD431000AGU-B10-9KH-A	32-pin PLASTIC TSOP(I) (8x13.4) (Reverse bent)	100			

Remark Products with -A at the end of the part number are lead-free products.

Pin Configurations (Marking Side)

/xxx indicates active low signal.

	[μPD431000ACZ-xx	LL]	
			1
NC O	1	32	
A16 ○>	2	31	≺────────────────────────
A14 O►	3	30	←───────── CE2
A12 ○	4	29	←O /WE
A7 O>	5	28	←───────────────────────
A6 ○	6	27	←───○ A8
A5 ○>	7	26	 ○ A9
A4 ⊖	8	25	≺ —⊖ A11
A3 ()	9	24	 ⊖ /OE
A2 ⊖	10	23	←────────────────────────────
A1 ⊖	11	22	←) /CE1
A0 ⊖	12	21	 ○ I/O8
I/01 ⊖ >	13	20	←→ ⊖ I/07
I/O2 ⊖ < →	14	19	 ⊖ I/O6
I/O3 ⊖ < →	15	18	←→ ○ I/O5
GND O	16	17	 ⊖ I/O4

32-pin PLASTIC DIP (15.24 mm (600)) [µPD431000ACZ-xxL]

A0 - A16	: Address inputs
I/O1 - I/O8	: Data inputs / outputs
/CE1, CE2	: Chip Enable 1, 2
/WE	: Write Enable
/OE	: Output Enable
Vcc	: Power supply
GND	: Ground
NC	: No connection

Remark Refer to Package Drawings for the 1-pin index mark.

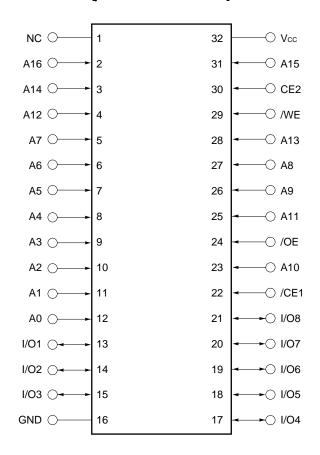
32-pin PLASTIC SOP (13.34 mm (525))

[*µ*PD431000AGW-xxL]

[*µ*PD431000AGW-xxLL]

[*µ*PD431000AGW-Axx]

- [*µ*PD431000AGW-Bxx]
- [*µ*PD431000AGW-xxL-A]
- [*µ*PD431000AGW-xxLL-A]
- [μPD431000AGW-Axx-A] [μPD431000AGW-Bxx-A]

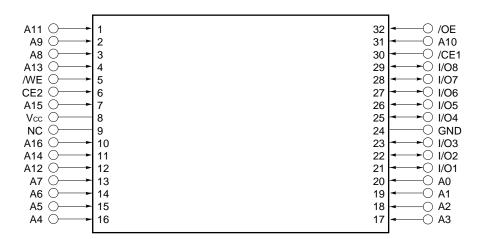


A0 - A16	: Address inputs
I/O1 - I/O8	: Data inputs / outputs
/CE1, CE2	: Chip Enable 1, 2
/WE	: Write Enable
/OE	: Output Enable
Vcc	: Power supply
GND	: Ground
NC	: No connection

Remark Refer to **Package Drawings** for the 1-pin index mark.

Data Sheet M11657EJDV0DS

32-pin PLASTIC TSOP(I) (8x20) (Normal bent) [μPD431000AGZ-xxLL-KJH] [μPD431000AGZ-Bxx-KJH] [μPD431000AGZ-xxLL-KJH-A] [μPD431000AGZ-Bxx-KJH-A]



32-pin PLASTIC TSOP(I) (8x20) (Reverse bent) [μPD431000AGZ-xxLL-KKH] [μPD431000AGZ-xxLL-KKH-A]

$ \begin{array}{c} /OE \bigcirc & 32 \\ A10 \bigcirc & 31 \\ /CE1 \bigcirc & 30 \end{array} $	
/CE1 0→ 30 3 ← 0 A8	
	3
I/O7 ○ ← → 28 5 ← ○ /W	Е
I/O6 ○ ← → 27 6 ← ○ CE	2
I/O5 ○ ← → 26 7 ← ○ A1	
I/O4 ○ ← → 25 8 ─── ∨ ca	С
GND 0 24 9 0 NC	;
I/O3 ○ ← → 23 10 ← ○ A1	6
I/O2 ○ ← → 22 11 ← ○ A1-	4
I/O1 ○ ← → 21 12 ← ○ A1:	2
A0 ○ → 20 13 ← ○ A7	
A1 ○ → 19 14 ← ○ A6	i.
A2 ○ → 18 15 < 0 A5	
A3 (

A0 - A16 : Address inputs	/OE : Output Enable
I/O1 - I/O8: Data inputs / outputs	Vcc : Power supply
/CE1, CE2: Chip Enable 1, 2	GND : Ground
/WE : Write Enable	NC : No connection

Remark Refer to **Package Drawings** for the 1-pin index mark.

32-pin PLASTIC TSOP(I) (8x13.4) (Normal bent) [μPD431000AGU-Bxx-9JH] [μPD431000AGU-Bxx-9JH-A]



32-pin PLASTIC TSOP(I) (8x13.4) (Reverse bent) [μPD431000AGU-Bxx-9KH]

[µPD431000AGU-Bxx-9KH-A]

		7
/OE ○	32 1	← ⊖ A11
A10 ○>	31 2	≺ −−○ A9
/CE1 ○>	30 3	<○ A8
I/O8 ⊖>	29 4	<○ A13
I/07 ⊖ >	28 5	<○ /WE
I/O6 ⊖ >	27 6	
I/O5 ⊖ ≻	26 7	≺ —──○ A15
I/O4 ⊖ >	25 8	O Vcc
	24 9	O NC
I/O3 ⊖ ≻	23 10	≺ —⊖ A16
I/O2 ⊖ >	22 11	≺ —⊖ A14
I/O1 ⊖ ∢ →	21 12	<○ A12
A0 ○>	20 13	≺ —⊖ A7
A1 ()	19 14	≺ —⊖ A6
A2 ()≻	18 15	≺ —⊖ A5
A3 ()►	17 16	≺ —⊖ A4
		J

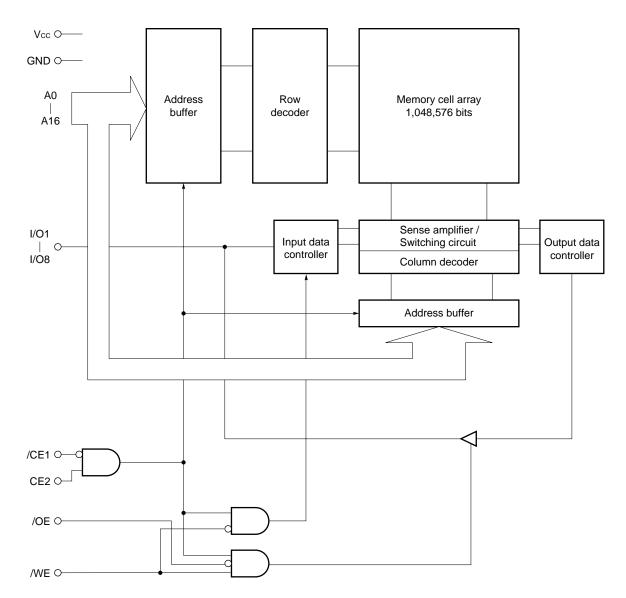
A0 - A16	:	Address inputs
I/O1 - I/O8	:	Data inputs / outputs
/CE1, CE2	:	Chip Enable 1, 2
/WE	:	Write Enable
/OE	:	Output Enable
Vcc	:	Power supply
GND	:	Ground
NC	:	No connection

Remark Refer to Package Drawings for the 1-pin index mark.

Data Sheet M11657EJDV0DS

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Block Diagram



Truth Table

/CE1	CE2	/OE	/WE	Mode	I/O	Supply current
н	×	×	×	Not selected	High impedance	lsв
×	L	×	×			
L	н	Н	н	Output disable		ICCA
L	н	L	н	Read	Dout	
L	н	×	L	Write	Din	

Remark $\times : V_{IH} \text{ or } V_{IL}$

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	Vcc		-0.5 ^{Note} to +7.0	V
Input / Output voltage	VT		-0.5 ^{Note} to Vcc + 0.5	V
Operating ambient temperature	TA		0 to 70	°C
Storage temperature	Tstg		–55 to +125	°C

Note -3.0 V (MIN.) (Pulse width: 30 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	μPD431000A-xxL		μPD431000A-Axx		μPD431000A-Bxx		Unit
			μPD4310	00A-xxLL					
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Supply voltage	Vcc		4.5	5.5	3.0	5.5	2.7	5.5	V
High level input voltage	VIH		2.2	Vcc+0.5	2.2	Vcc+0.5	2.2	Vcc+0.5	V
Low level input voltage	VIL		-0.3 Note	+0.8	-0.3 Note	+0.5	-0.3 Note	+0.5	V
Operating ambient temperature	TA		0	70	0	70	0	70	°C

Note -3.0 V (MIN.) (Pulse width: 30 ns)

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	CIN	V _{IN} = 0 V			6	pF
Input / Output capacitance	Cı/o	V _{1/O} = 0 V			10	pF

Remarks 1. VIN : Input voltage

VI/o : Input / Output voltage

2. These parameters are not 100% tested.

Parameter	Symbol	Test condition		μPD4	431000/	A-xxL	μPD4	31000A	-xxLL	μPD4	31000	A-Axx	Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input leakage	lu	$V_{IN} = 0 V$ to V_{CC}		-1.0		+1.0	-1.0		+1.0	-1.0		+1.0	μA
current													
I/O leakage	Ilo	$V_{I/O} = 0 V$ to V_{CC} ,		-1.0		+1.0	-1.0		+1.0	-1.0		+1.0	μA
current		/CE1 = VIH or CE2 = 1	VIL										
		or /WE = VIL or /OE =	= VIH										
Operating	ICCA1	/CE1 = VIL, CE2 = VIH	н,		40	70		40	70		40	70	mA
supply current		I _{1/0} = 0 mA											
		Minimum cycle time	$V\text{cc} \leq 3.6 \text{ V}$			-			-			35	
	ICCA2	/CE1 = VIL, CE2 = VI	H, II/O = 0 mA,			15			15			15	
		Cycle time = ∞	$Vcc \le 3.6 V$			-			_			8	
	Іссаз	/CE1 \leq 0.2 V, CE2 \geq	Vcc – 0.2 V,			10			10			10	
		Cycle time = 1 μ s, I_{μ} s	o = 0 mA,										
		$V\text{IL} \leq 0.2 \text{ V}, \text{ VIH} \geq V\text{cc}$	– 0.2 V										
			$Vcc \le 3.6 V$			-			_			8	
Standby	lsв	/CE1 = VIH or CE2 = 1	VIL			3			3			3	mA
supply current			$Vcc \le 3.6 V$			-			_			2	
	ISB1	$/CE1 \ge V_{CC} - 0.2 V$,			2	100		1	20		1	20	μA
		$CE2 \geq V_{CC} - 0.2 \; V$	$Vcc \le 3.6 V$			-			-		0.5	13	
	ISB2	$CE2 \le 0.2 V$			2	100		1	20		1	20	
			$Vcc \le 3.6 V$		-	-		_	_		0.5	13	
High level	Voh1	Іон = −1.0 mA, Vcc ≥	4.5 V	2.4			2.4			2.4			V
output voltage		Іон = –0.5 mA		-			_			2.4			
	Voh2	Iон = -0.02 mA		-			_			Vcc-0.1			
Low level	Vol1	lo∟ = 2.1 mA, Vcc ≥ 4	.5 V			0.4			0.4			0.4	V
output voltage		lo∟ = 1.0 mA				-			-			0.4	
	Vol2	IoL = 0.02 mA				-			-			0.1	

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted) (1/2)

Remarks 1. VIN : Input voltage

VI/O : Input / Output voltage

2. These DC characteristics are in common regardless product classification.

Parameter	Symbol	Test condition		μF	PD431000A	-Bxx	Unit
				MIN.	TYP.	MAX.	
Input leakage current	lu	$V_{IN} = 0 V to V_{CC}$		-1.0		+1.0	μA
I/O leakage current	Ilo	$V_{I/O} = 0 V$ to V_{CC} , $/CE1 = V_{IH}$ or $CE2 = V_{IH}$	/1L	-1.0		+1.0	μA
		or /WE = VIL or /OE = VIH					
Operating supply current	ICCA1	/CE1 = VIL, CE2 = VIH, II/0 = 0 mA			40	70	mA
		Minimum cycle time	$V\text{cc} \leq 3.3 \text{ V}$			30	
	ICCA2	/CE1 = VIL, CE2 = VIH, II∕O = 0 mA,				15	
		Cycle time = ∞	$V\text{cc} \leq 3.3 \text{ V}$			7	
	Іссаз	/CE1 \leq 0.2 V, CE2 \geq Vcc – 0.2 V,				10	
		Cycle time = 1 μ s, I ν o = 0 mA,					
		$V_{\text{IL}} \leq 0.2 \text{ V}, \text{ V}_{\text{IH}} \geq V_{\text{CC}} - 0.2 \text{ V}$	$V_{\text{CC}} \leq 3.3 \text{ V}$			7	
Standby supply current	lsв	/CE1 = VIH or CE2 = VIL				3	mA
			$V_{\text{CC}} \leq 3.3 \text{ V}$			2	
	ISB1	/CE1 \ge Vcc - 0.2 V, CE2 \ge Vcc - 0.2 V			1	20	μA
			$V_{\text{CC}} \leq 3.3 \text{ V}$		0.5	11	
	ISB2	$CE2 \le 0.2 V$			1	20	
			$V_{\text{CC}} \leq 3.3 \text{ V}$		0.5	11	
High level output voltage	V _{OH1}	Iон = -1.0 mA, Vcc ≥ 4.5 V		2.4			V
		Iон = –0.5 mA		2.4			
	Vон2	Iон = -0.02 mA		Vcc-0.1			
Low level output voltage	V _{OL1}	I_{OL} = 2.1 mA, $V_{CC} \ge 4.5 V$				0.4	V
		IoL = 1.0 mA				0.4	
	V _{OL2}	IoL = 0.02 mA				0.1	

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted) (2/2)

Remarks 1. VIN : Input voltage

VI/O : Input / Output voltage

2. These DC characteristics are in common regardless product classification.

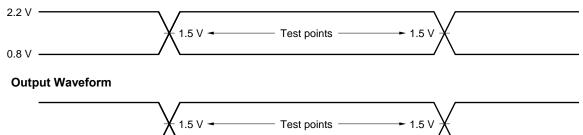
AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

AC Test Conditions

NEC

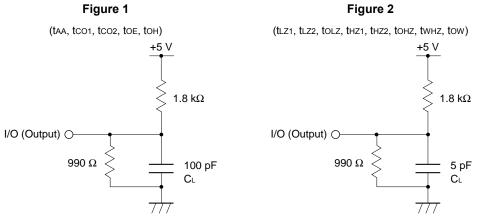
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[μPD431000A-70L, μPD431000A-85L, μPD431000A-70LL, μPD431000A-85LL]
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Input Waveform (Rise and Fall Time \leq 5 ns)



Output Load

AC characteristics should be measured with the following output load conditions.



Remark CL includes capacitance of the probe and jig, and stray capacitance.

[μPD431000A-A10, μPD431000A-B10, μPD431000A-B12, μPD431000A-B15]

Input Waveform (Rise and Fall Time \leq 5 ns) 2.2 V 0.5 V Output Waveform 1.5 V 1.5 VTest points 1.5 V 1.5 V1.5 V

Output Load

AC characteristics should be measured with the following output load conditions.

Part number	Output load condition						
	taa, tco1, tco2, toe, toh	tlz1, tlz2, tolz, thz1, thz2, tohz, twhz, tow					
μPD431000A-A10, μPD431000A-B10, μPD431000A-B12	1TTL + 50 pF	1TTL + 5 pF					
μPD431000A-B15	1TTL + 100 pF	1TTL + 5 pF					

Read Cycle (1/2)

Parameter	Symbol		Vcc ≥	4.5 V		Vcc ≥	3.0 V	Unit	Condition
		<i>μ</i> PD431	000A-70	μPD431	μPD431000A-85		00A-A10		
		<i>μ</i> ΡD4310	000A-Axx						
		<i>μ</i> ΡD4310	000A-Bxx						
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	trc	70		85		100		ns	
Address access time	taa		70		85		100	ns	Note
/CE1 access time	tco1		70		85		100	ns	
CE2 access time	tco2		70		85		100	ns	
/OE to output valid	toe		35		45		50	ns	
Output hold from address change	tон	10		10		10		ns	
/CE1 to output in low impedance	t LZ1	10		10		10		ns	
CE2 to output in low impedance	tLZ2	10		10		10		ns	
/OE to output in low impedance	tolz	5		5		5		ns	
/CE1 to output in high impedance	t HZ1		25		30		35	ns	
CE2 to output in high impedance	t _{HZ2}		25		30		35	ns	
/OE to output in high impedance	tонz		25		30		35	ns	

Note See the output load.

Remark These AC characteristics are in common regardless of package types.

Read Cycle (2/2)

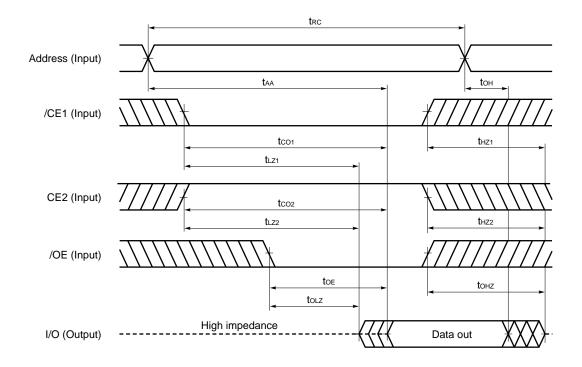
Parameter	Symbol			Vcc≥	2.7 V			Unit	Condition
		μPD4310	PD431000A-B10		μPD431000A-B12		000A-B15		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	trc	100		120		150		ns	
Address access time	taa		100		120		150	ns	Note
/CE1 access time	tco1		100		120		150	ns	
CE2 access time	tco2		100		120		150	ns	
/OE to output valid	toe		50		60		70	ns	
Output hold from address change	tон	10		10		10		ns	
/CE1 to output in low impedance	tLZ1	10		10		10		ns	
CE2 to output in low impedance	tLZ2	10		10		10		ns	
/OE to output in low impedance	tolz	5		5		5		ns	
/CE1 to output in high impedance	t _{HZ1}		35		40		50	ns	
CE2 to output in high impedance	t _{HZ2}		35		40		50	ns	
/OE to output in high impedance	tонz		35		40		50	ns	

Note See the output load.

Remark These AC characteristics are in common regardless of package types.

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Read Cycle Timing Chart



Remark In read cycle, /WE should be fixed to high level.

Write Cycle (1/2)

Parameter	Symbol		Vcc ≥	4.5 V		Vcc≥	3.0 V	Unit	Condition
`		μPD431	μPD431000A-70 μF		μPD431000A-85		000A-A10		
		<i>μ</i> ΡD4310	000A-Axx						
		<i>μ</i> ΡD4310	000A-Bxx						
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t wc	70		85		100		ns	
/CE1 to end of write	tcw1	55		70		80		ns	
CE2 to end of write	tcw2	55		70		80		ns	
Address valid to end of write	taw	55		70		80		ns	
Address setup time	tas	0		0		0		ns	
Write pulse width	twp	50		60		60		ns	
Write recovery time	t wr	5		5		0		ns	
Data valid to end of write	tow	35		35		60		ns	
Data hold time	tон	0		0		0		ns	
/WE to output in high impedance	twнz		25		30		35	ns	Note
Output active from end of write	tow	5		5		5		ns	

Note See the output load.

Remark These AC characteristics are in common regardless package types.

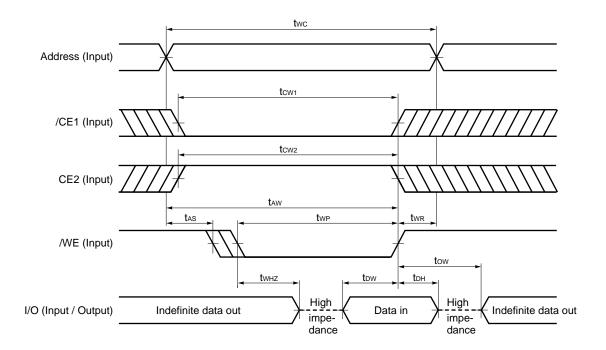
Write Cycle (2/2)

Parameter	Symbol			Vcc≥	2.7 V			Unit	Condition
		μPD4310	PD431000A-B10 µPD		μPD431000A-B12		000A-B15		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t wc	100		120		150		ns	
/CE1 to end of write	tcw1	80		100		120		ns	
CE2 to end of write	tcw2	80		100		120		ns	
Address valid to end of write	taw	80		100		120		ns	
Address setup time	tas	0		0		0		ns	
Write pulse width	tw₽	60		85		100		ns	
Write recovery time	twr	0		0		0		ns	
Data valid to end of write	tow	60		60		80		ns	
Data hold time	tон	0		0		0		ns	
/WE to output in high impedance	twнz		35		40		50	ns	Note
Output active from end of write	tow	5		5		5		ns	

Note See the output load.

Remark These AC characteristics are in common regardless of package types.

Write Cycle Timing Chart 1 (/WE Controlled)

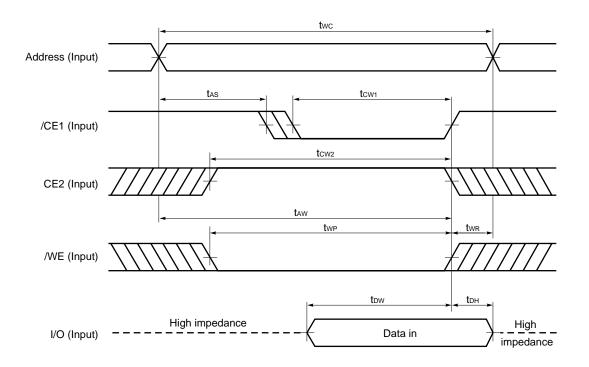


Cautions 1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.2. Do not input data to the I/O pins while they are in the output state.

Remarks 1. Write operation is done during the overlap time of a low level /CE1, /WE and a high level CE2.

- If /CE1 changes to low level at the same time or after the change of /WE to low level, or if CE2 changes to high level at the same time or after the change of /WE to low level, the I/O pins will remain high impedance state.
- 3. When /WE is at low level, the I/O pins are always high impedance. When /WE is at high level, read operation is executed. Therefore /OE should be at high level to make the I/O pins high impedance.

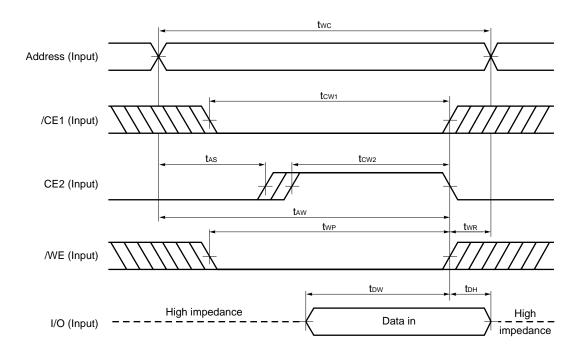
Write Cycle Timing Chart 2 (/CE1 Controlled)



Cautions 1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.2. Do not input data to the I/O pins while they are in the output state.

Remark Write operation is done during the overlap time of a low level /CE1, /WE and a high level CE2.

Write Cycle Timing Chart 3 (CE2 Controlled)



Cautions 1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.2. Do not input data to the I/O pins while they are in the output state.

Remark Write operation is done during the overlap time of a low level /CE1, /WE and a high level CE2.

Parameter	Symbol	Test Condition	<i>µ</i> PD	9431000A	-xxL	μPD	431000A- 0431000A 0431000A	-Axx	Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Data retention	VCCDR1	$/CE1 \ge V_{CC} - 0.2 V$,	2.0		5.5	2.0		5.5	V
supply voltage		$CE2 \geq V_{CC} - 0.2 \ V$							
	VCCDR2	$CE2 \le 0.2 V$	2.0		5.5	2.0		5.5	
Data retention	ICCDR1	V_{CC} = 3.0 V, /CE1 \ge V _{CC} – 0.2 V,		1	50 Note1		0.5	10 Note2	μA
supply current		$CE2 \geq V_{CC} - 0.2 \ V$							
	ICCDR2	V_{CC} = 3.0 V, CE2 \leq 0.2 V		1	50 Note1		0.5	10 Note2	
Chip deselection	t CDR		0			0			ns
to data retention									
mode									
Operation	tR		5			5			ms
recovery time									

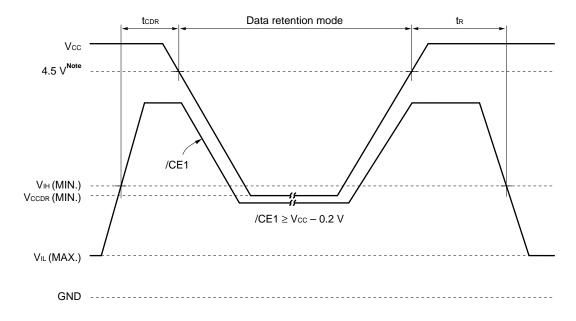
Low Vcc Data Retention Characteristics (T_A = 0 to 70 °C)

Notes 1. 15 μ A (Ta \leq 40 °C)

2. 3 μA (T_A ≤ 40 °C)

Data Retention Timing Chart

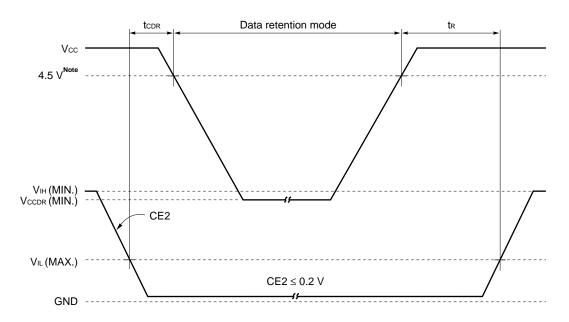
(1) /CE1 Controlled



Note A version : 3.0 V, B version : 2.7 V

RemarkOn the data retention mode by controlling /CE1, the input level of CE2 must be CE2 \ge Vcc - 0.2 V or CE2 \le 0.2 V. The other pins (Address, I/O, /WE, /OE) can be in high impedance state.

(2) CE2 Controlled

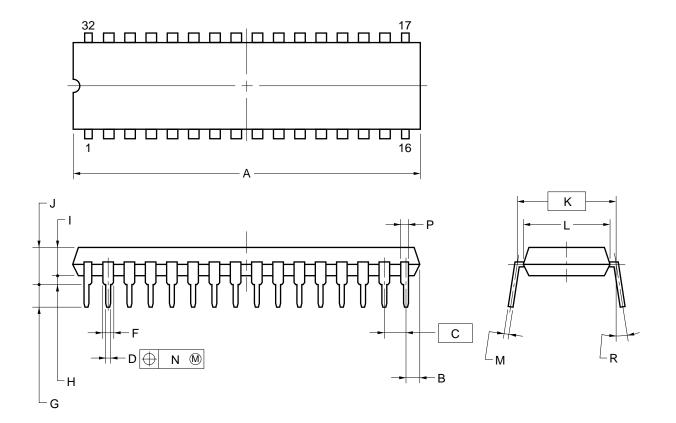


Note A version : 3.0 V, B version : 2.7 V

Remark On the data retention mode by controlling CE2, the other pins (/CE1, Address, I/O, /WE, /OE) can be in high impedance state.

Package Drawings

32-PIN PLASTIC DIP (15.24mm(600))

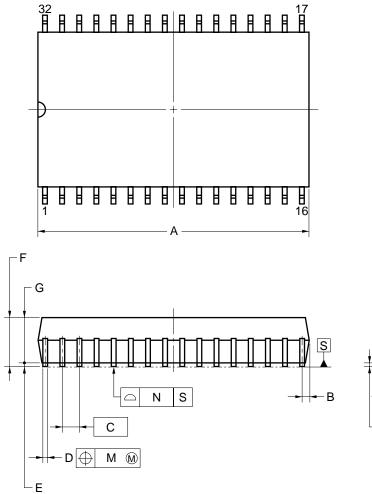


- 1. Each lead centerline is located within 0.25 mm of its true position (T.P.) at maximum material condition.
- 2. Item "K" to center of leads when formed parallel.

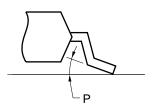
ITEM	MILLIMETERS
А	40.64 MAX.
В	1.27 MAX.
С	2.54 (T.P.)
D	0.50±0.10
F	1.1 MIN.
G	3.2±0.3
Н	0.51 MIN.
I	4.31 MAX.
J	5.08 MAX.
К	15.24 (T.P.)
L	13.2
М	$0.25\substack{+0.10 \\ -0.05}$
Ν	0.25
Р	0.9 MIN.
R	0 - 15°
	D22C 100 600A 2

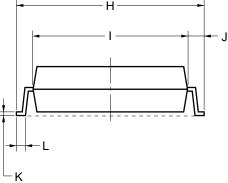
P32C-100-600A-2

32-PIN PLASTIC SOP (13.34 mm (525))



detail of lead end





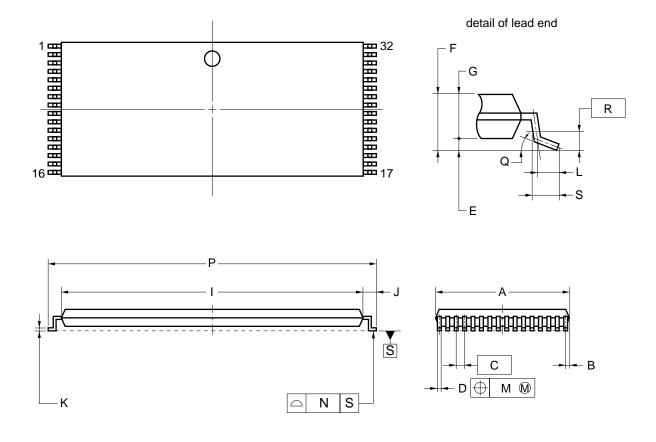
NOTE

Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	20.61 MAX.
В	0.78 MAX.
С	1.27 (T.P.)
D	$0.40\substack{+0.10\\-0.05}$
Е	0.15±0.05
F	2.95 MAX.
G	2.7
Н	14.1±0.3
I	11.3
J	1.4±0.2
К	$0.20^{+0.10}_{-0.05}$
L	0.8±0.2
М	0.12
N	0.10
Р	$3^{\circ + 7^{\circ}}_{-3^{\circ}}$

P32GW-50-525A-1

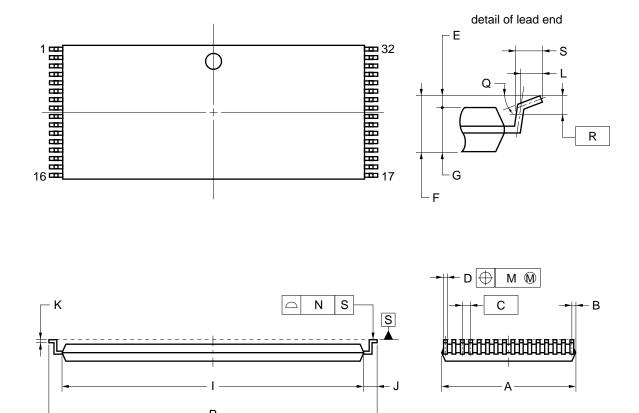
32-PIN PLASTIC TSOP(I) (8x20)



- 1. Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.
- 2. "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX.)

ITEM	MILLIMETERS	
A	8.0±0.1	
В	0.45 MAX.	
С	0.5 (T.P.)	
D	0.22±0.05	
Е	0.1±0.05	
F	1.2 MAX.	
G	0.97±0.08	
I	18.4±0.1	
J	0.8±0.2	
К	0.145±0.05	
L	0.5	
М	0.10	
N	0.10	
Р	20.0±0.2	
Q	3° ^{+5°} -3°	
R	0.25	
S	0.60±0.15	
	S32GZ-50-KJH1-2	

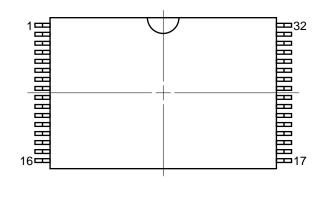
32-PIN PLASTIC TSOP(I) (8x20)

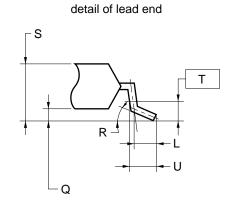


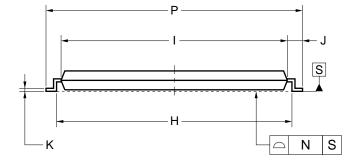
- 1. Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.
- 2. "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX.)

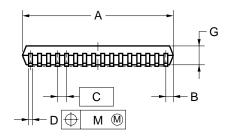
ITEM	MILLIMETERS		
А	8.0±0.1		
В	0.45 MAX.		
С	0.5 (T.P.)		
D	0.22±0.05		
Е	0.1±0.05		
F	1.2 MAX.		
G	0.97±0.08		
I	18.4±0.1		
J	0.8±0.2		
К	0.145±0.05		
L	0.5		
М	0.10		
Ν	0.10		
Р	20.0±0.2		
Q	$3^{\circ}^{+5^{\circ}}_{-3^{\circ}}$		
R	0.25		
S	0.60±0.15		
:	S32GZ-50-KKH1-2		

32-PIN PLASTIC TSOP(I) (8x13.4)





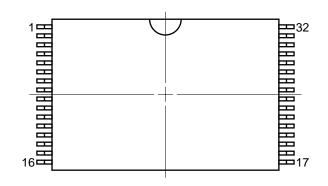




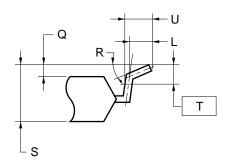
- 1. Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.
- 2. "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX.)

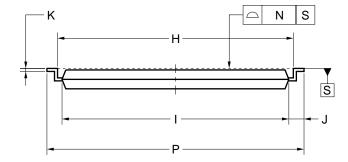
ITEM	MILLIMETERS	
Α	8.0±0.1	
В	0.45 MAX.	
С	0.5 (T.P.)	
D	0.22±0.05	
G	1.0±0.05	
Н	12.4±0.2	
I	11.8±0.1	
J	0.8±0.2	
К	$0.145\substack{+0.025\\-0.015}$	
L	0.5	
М	0.08	
Ν	0.08	
Р	13.4±0.2	
Q	0.1±0.05	
R	$3^{\circ}^{+5^{\circ}}_{-3^{\circ}}$	
S	1.2 MAX.	
Т	0.25	
U	0.6±0.15	
	P32GU-50-9JH-2	

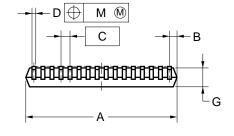
32-PIN PLASTIC TSOP(I) (8x13.4)



detail of lead end







- 1. Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.
- 2. "A" excludes mold flash. (Includes mold flash : 8.3 mm MAX.)

ITEM	MILLIMETERS	
Α	8.0±0.1	
В	0.45 MAX.	
С	0.5 (T.P.)	
D	0.22±0.05	
G	1.0±0.05	
Н	12.4±0.2	
I	11.8±0.1	
J	0.8±0.2	
к	$0.145\substack{+0.025\\-0.015}$	
L	0.5	
М	0.08	
Ν	0.08	
Р	13.4±0.2	
Q	0.1±0.05	
R	$3^{\circ}^{+5^{\circ}}_{-3^{\circ}}$	
S	1.2 MAX.	
Т	0.25	
U	0.6±0.15	
	P32GU-50-9KH-2	

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μ PD431000A.

Types of Surface Mount Device

μPD431000AGW-xxL	: 32-pin PLASTIC SOP (13.34 mm (525))
μ PD431000AGW-xxLL	: 32-pin PLASTIC SOP (13.34 mm (525))
μPD431000AGW-Axx	: 32-pin PLASTIC SOP (13.34 mm (525))
μPD431000AGW-Bxx	: 32-pin PLASTIC SOP (13.34 mm (525))
μPD431000AGZ-xxLL-KJH	: 32-pin PLASTIC TSOP(I) (8x20) (Normal bent)
μPD431000AGZ-xxLL-KKH	: 32-pin PLASTIC TSOP(I) (8x20) (Reverse bent)
μPD431000AGZ-Bxx-KJH	: 32-pin PLASTIC TSOP(I) (8x20) (Normal bent)
μPD431000AGU-Bxx-9JH	: 32-pin PLASTIC TSOP(I) (8x13.4) (Normal bent)
μPD431000AGU-Bxx-9KH	: 32-pin PLASTIC TSOP(I) (8x13.4) (Reverse bent)
μPD431000AGW-xxL-A	: 32-pin PLASTIC SOP (13.34 mm (525))
μ PD431000AGW-xxLL-A	: 32-pin PLASTIC SOP (13.34 mm (525))
μPD431000AGW-Axx-A	: 32-pin PLASTIC SOP (13.34 mm (525))
μPD431000AGW-Bxx-A	: 32-pin PLASTIC SOP (13.34 mm (525))
μPD431000AGZ-xxLL-KJH-A	A : 32-pin PLASTIC TSOP(I) (8x20) (Normal bent)
μPD431000AGZ-xxLL-KKH-	A: 32-pin PLASTIC TSOP(I) (8x20) (Reverse bent)
μPD431000AGZ-Bxx-KJH-A	: 32-pin PLASTIC TSOP(I) (8x20) (Normal bent)
μPD431000AGU-Bxx-9JH-A	: 32-pin PLASTIC TSOP(I) (8x13.4) (Normal bent)
μPD431000AGU-Bxx-9KH-A	: 32-pin PLASTIC TSOP(I) (8x13.4) (Reverse bent)

Types of Through Hole Mount Device

μPD431000ACZ-xxL : 32-pin PLASTIC DIP (15.24 mm (600)) μPD431000ACZ-xxLL : 32-pin PLASTIC DIP (15.24 mm (600))

Soldering process	Soldering conditions
Wave soldering (Only to leads)	Solder temperature: 260 °C or below, Flow time: 10 seconds or below
Partial heating method	Pin temperature : 300 °C or below, Time: 3 seconds or below (Per one lead)

Caution Do not jet molten solder on the surface of package.

Revision History

Edition/	Page		Type of	Description
Date	This	Previous	revision	
	edition	edition		
13th edition/	through	through	Modification	Ordering Information revised.
Nov. 2008				

[MEMO]

NOTES FOR CMOS DEVICES —

1 VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

(2) HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

5 POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

6 INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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- "Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support).
- "Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.

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