Look-Ahead Carry Generators

General Description

These circuits are high-speed, look-ahead carry generators, capable of anticipating a carry across four binary adders or groups of adders. They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as shown in the pin designation table.

When used in conjunction with the 181 arithmetic logic unit, these generators provide high-speed carry look-ahead capability for any word length. Each 182 or S182 generates the look-ahead (anticipated carry) across a group of four ALU's and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading circuits to perform multi-level look-ahead is illustrated under typical application data.

Carry input and output of the ALU's are in their true form, and the carry propagate (P) and carry generate (G) are in negated form; therefore, the carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretations of carry functions, as explained on the 181 data sheet are also applicable to and compatible with the look-ahead generator. Positive logic equations for the 182 and S182 are:

$C_{n+x} = \overline{G}0 + \overline{P}0\, C_n$

$C_{n+y} = \overline{G}1 + \overline{P}1\,\overline{G}0 + \overline{P}1\,\overline{P}0\, C_n$

$C_{n+z} = \overline{G}2 + \overline{P}2\,\overline{G}1 + \overline{P}2\,\overline{P}1\,\overline{G}0 + \overline{P}2\,\overline{P}1\,\overline{P}0\, C_n$

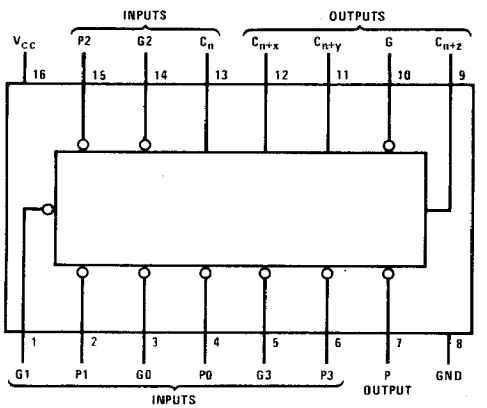
$\overline{G} = \overline{G}3\,(\overline{P}3 + \overline{G}2)\,(\overline{P}3 + \overline{P}2 + \overline{G}1)\,(\overline{P}3 + \overline{P}2 + \overline{P}1 + \overline{G}0)$

$\overline{P} = \overline{P}3\,\overline{P}2\,\overline{P}1\,\overline{P}0$

Features

TYPE	TYPICAL PROPAGATION DELAY TIME	TYPICAL POWER DISSIPATION
182	12 ns	180 mW
S182	7 ns	260 mW

Connection Diagram



54182(J); 74182(J), (N); 74S182(N)

Pin Designations

DESIGNATION	PIN NOS.	FUNCTION
G0, G1, G2, G3	3, 1, 14, 5	ACTIVE LOW CARRY GENERATE INPUTS
P0, P1, P2, P3	4, 2, 15, 6	ACTIVE LOW CARRY PROPAGATE INPUTS
C_n	13	CARRY INPUT
C_{n+x}, C_{n+y}, C_{n+z}	12, 11, 9	CARRY OUTPUTS
G	10	ACTIVE LOW CARRY GENERATE OUTPUT
P	7	ACTIVE LOW CARRY PROPAGATE OUTPUT
V_{CC}	16	SUPPLY VOLTAGE
GND	8	GROUND

74S182 To Be Announced In 1976

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Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			CONDITIONS		DM54/74 182 MIN	DM54/74 182 TYP(1)	DM54/74 182 MAX	DM74S S182 MIN	DM74S S182 TYP(1)	DM74S S182 MAX	UNITS
V_{IH}	High Level Input Voltage				2			2			V
V_{IL}	Low Level Input Voltage						0.8			0.8	V
V_I	Input Clamp Voltage		V_{CC} = Min, I_I = 12 mA				1.5				V
			V_{CC} = Min, I_I = 18 mA							1.2	V
I_{OH}	High Level Output Current						-800			-1000	µA
V_{OH}	High Level Output Voltage		V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = Max	DM54	2.4				N/A		V
				DM74	2.4			2.7	3.4		V
I_{OL}	Low Level Output Current						16			20	mA
V_{OL}	Low Level Output Voltage		V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = Max				0.4			0.5	V
I_I	Input Current at Maximum Input Voltage		V_{CC} = Max, V_I = 5.5V				1			1	mA
I_{IH}	High Level Input Current	C_n Input	V_{CC} = Max, V_I = 2.4V (182), V_I = 2.7V (S182)				80			50	µA
		P3 Input					120			100	µA
		P2 Input					160			150	µA
		P0, P1, or G3 Input					200			200	µA
		G0 or G2 Input					360			350	µA
		G1 Input					400			400	µA
I_{IL}	Low Level Input Current	C_n Input	V_{CC} = Max, V_I = 0.4V (182), V_I = 0.5V (S182)				-3.2			-2	mA
		P3 Input					4.8			4	mA
		P2 Input					-6.4			-6	mA
		P0, P1, or G3 Input					-8.0			-8	mA
		G0 or G2 Input					14.4			-14	mA
		G1 Input					16			16	mA
I_{OS}	Short Circuit Output Current		V_{CC} = Max(2)		-40		-100	-40		-100	mA
I_{CCH}	Supply Current, All Outputs High		V_{CC} = 5V(3)			27			35		mA
I_{CCL}	Supply Current, All Outputs Low		V_{CC} = Max(4)	DM54		45	65		N/A		mA
				DM74		45	72		69	109	mA

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

(3) I_{CCH} is measured with all outputs open, inputs P3 and G3 at 4.5V, and all other inputs grounded.

(4) I_{CCL} is measured with all outputs open; inputs G0, G1, and G2 at 4.5V, and all other inputs grounded.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	DM54/74 182 MIN	DM54/74 182 TYP	DM54/74 182 MAX	DM74S S182 MIN	DM74S S182 TYP	DM74S S182 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	G0, G1, G2, G3, P0, P1, P2, or P3	C_{n+x}, C_{n+y}, or C_{n+z}	R_L = 400Ω, C_L = 15 pF (182)		11	17		4.5	7	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					13	22		4.5	7	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	G0, G1, G2, G3, P1, P2, or P3	G			11	17		5	7.5	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					13	22		7	10.5	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	P0, P1, P2, or P3	P			11	17		4.5	6.5	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					13	22		6.5	10	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_n	C_{n+x}, C_{n+y}, or C_{n+z}	R_L = 280Ω, C_L = 15 pF (S182)		11	17		6.5	10	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					13	22		7	10.5	ns

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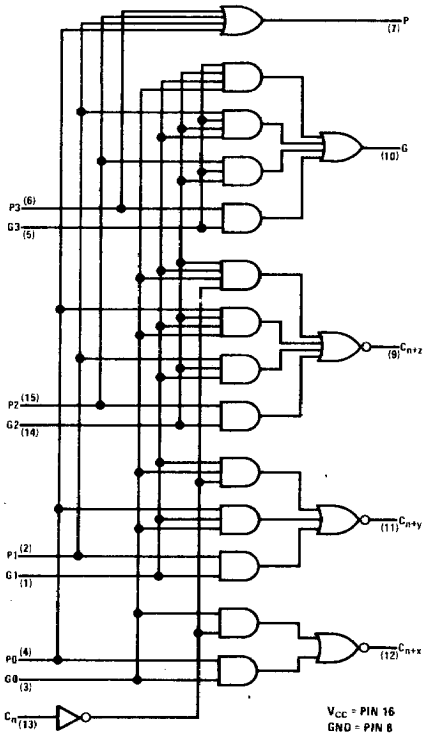
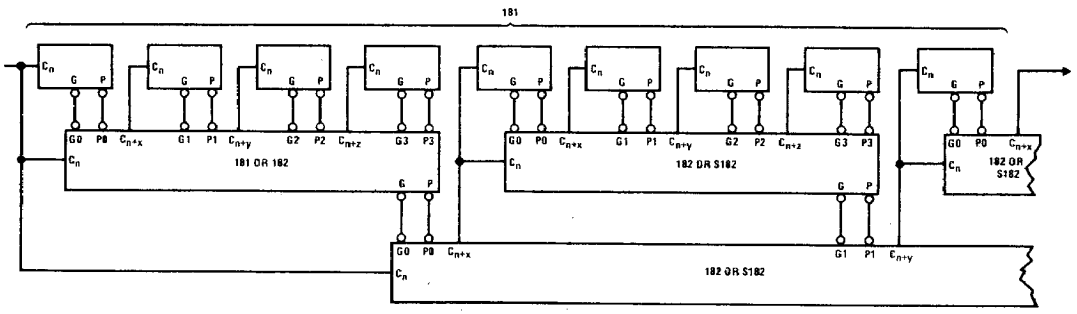
Logic Diagram



Typical Application

64-BIT ALU, FULL-CARRY LOOK AHEAD IN THREE LEVELS



A and B inputs, and F outputs of 181 are not shown.

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