National Semiconductor

# MICROCIRCUIT DATA SHEET

## MNDM54LS74-X REV 1A0

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# DUAL POSITIVE EDGE-TRIGGERED D FLIP-FLOPS with PRESET, CLEAR and COMPLEMENTARY OUTPUTS

## General Description

The 'LS74 is a dual D-type flip-flop with Direct Clear and Set inputs and complementary (Q, $\overline{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be tranferred to the outputs until the next rising edge of the Clock Pulse input.

## Industry Part Number

54LS74

## NS Part Numbers

DM54LS74E/883
DM54LS74J/883
DM54LS74W/883

## Prime Die

L074

## Processing

MIL-STD-883, Method 5004

## Quality Conformance Inspection

MIL-STD-883, Method 5005

| Subgrp | Description | Temp ($^{O}$C) |
|---|---|---|
| 1 | Static tests at | +25 |
| 2 | Static tests at | +125 |
| 3 | Static tests at | -55 |
| 4 | Dynamic tests at | +25 |
| 5 | Dynamic tests at | +125 |
| 6 | Dynamic tests at | -55 |
| 7 | Functional tests at | +25 |
| 8A | Functional tests at | +125 |
| 8B | Functional tests at | -55 |
| 9 | Switching tests at | +25 |
| 10 | Switching tests at | +125 |
| 11 | Switching tests at | -55 |

## Features

-Asynchronous inputs
- Low input to $\overline{SD}$ sets Q to High level
- Low input to $\overline{CD}$ sets Q to Low level
- Clear and Set are independent of clock
- Simultaneous Low on $\overline{CD}$ and $\overline{SD}$ makes both Q and $\overline{Q}$ High

## (Absolute Maximum Ratings)

(Note 1)

| | |
|---|---|
| Storage Temperature | -65 C to +150 C |
| Ambient Temperature under Bias | -55 C to +125 C |
| Input Voltage | -0.5V to +5.5V |
| VCC Pin Potential to Ground Pin | -0.5V to +7.0V |
| Junction Temperature under Bias | -55 C to +175 C |
| Current Applied to Output in LOW state (Max) | twice the rated Iol (ma) |

Note 1: Absolute Maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

## Recommended Operating Conditions

| | |
|---|---|
| Free Air Ambient Temperature | |
| Military | -55 C to +125 C |
| Supply Voltage | |
| Military | +4.5V to +5.5V |

# Electrical Characteristics

## DC PARAMETER

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: VCC 4.5V to 5.5V, Temp range: -55C to 125C

| SYMBOL | PARAMETER | CONDITIONS | NOTES | PIN-NAME | MIN | MAX | UNIT | SUB-GROUPS |
|---|---|---|---|---|---|---|---|---|
| IIH (1) | Input High Current | VCC=5.5V, VM=2.7V, VINH=4.5V, VINL=0.0V | 1, 3 | D1, D2 | | 20.0 | uA | 1, 2, 3 |
| IIH (2) | Input High Current | VCC=5.5V, VM=2.7V, VINH=4.5V, VINL=0.0V | 1, 3 | CP1, SD1, SD2, CP2 | | 40.0 | uA | 1, 2, 3 |
| IIH (3) | Input High Current | VCC=5.5V, VM=2.7V, VINH=4.5V | 1, 3 | CD1, CD2 | | 60.0 | uA | 1, 2, 3 |
| IBVI (1) | Input High Current | VCC=5.5V, VM=5.5V, VINH=4.5V, VINL=0.0V | 1, 3 | INPUT | | 100 | uA | 1, 2, 3 |
| IIL (1) | Input LOW Current | VCC=5.5V, VM=0.4V, VINH=4.5V, VINL=0.0V | 1, 3 | D1, D2 | -0.03 | -0.4 | mA | 1, 2, 3 |
| IIL (2) | Input LOW Current | VCC=5.5V, VM=0.4V, VINH=4.5V, VINL=0.0V | 1, 3 | CP1, CP2, SD1, SD2 | -0.06 | -0.8 | mA | 1, 2, 3 |
| IIL (3) | Input LOW Current | VCC=5.5V, VM=0.4V, VINH=4.5V | 1, 3 | CD1, CD2 | -0.09 | -1.2 | mA | 1, 2, 3 |
| VOL | Output LOW Voltage | VCC=4.5V, VIH=2.0V, IOL=4.0mA, VINH=4.5V, VIL=0.7V | 1, 3 | OUTPUTS | | 0.4 | V | 1, 2, 3 |
| VOH | High Level Output Voltage | VCC=4.5V, VIL=0.7V, VIH=2.0V, VINH=4.5V, IOH=-0.4mA | 1, 3 | OUTPUTS | 2.5 | | V | 1, 2, 3 |
| IOS | Short Circuit Output Current | VCC=5.5V, VINH=4.5V, VINL=0.0V, VOUT=0.0V | 1, 3 | OUTPUT | -20.0 | -100 | mA | 1, 2, 3 |
| VCD | Input Clamp Diode Voltage | VCC=4.5V, IM=-18mA, VINH=4.5V | 1, 3 | INPUTS | | -1.5 | V | 1, 2, 3 |
| ICC | Supply Current | VCC=5.5V, VINL=0.0V, VINH=4.5V | 1, 3 | VCC | | 8.0 | mA | 1, 2, 3 |

# Electrical Characteristics

## AC PARAMETER - 15pF

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: CL=15pF, RL=2k ohms Temp range: +25C

| SYMBOL | PARAMETER | CONDITIONS | | NOTES | PIN-NAME | MIN | MAX | UNIT | SUB-GROUPS |
|---|---|---|---|---|---|---|---|---|---|
| tpLH | Propagation Delay | VCC=5.0V | | 2, 4 | CPn to Qn/$\overline{Q}$n | | 25.0 | ns | 9 |
| tpHL | Propagation Delay | VCC=5.0V | | 2, 4 | CPn to Qn/$\overline{Q}$n | | 35.0 | ns | 9 |
| tpLH (2) | Propagation Delay | VCC=5.0V | CP=High | 2, 4 | $\overline{C}$Dn/$\overline{S}$Dn to Q/ | | 15.0 | ns | 9 |
| tpHL (2) | Propagation Delay | VCC=5.0V | CP=High | 2, 4 | $\overline{C}$Dn/$\overline{S}$Dn to Q/ | | 35.0 | ns | 9 |
| tpLH (3) | Propagation Delay | VCC=5.0V | CP=Low | 2, 4 | $\overline{C}$Dn/$\overline{S}$Dn to Q/ | | 15.0 | ns | 9 |
| tpHL (3) | Propagation Delay | VCC=5.0V | CP=Low | 2, 4 | $\overline{C}$Dn/$\overline{S}$Dn to Q/ | | 24.0 | ns | 9 |
| ts (H) | Setup Time (High) | VCC=5.0V | | 2, 4 | Dn to CPn | 10.0 | | ns | 9 |
| ts (L) | Setup Time (Low) | VCC=5.0V | | 2, 4 | Dn to CPn | 20.0 | | ns | 9 |
| th (H) | Hold Time (High) | VCC=5.0V | | 2, 4 | Dn to CPn | 5.0 | | ns | 9 |
| th (L) | Hold Time (Low) | VCC=5.0V | | 2, 4 | Dn to CPn | 5.0 | | ns | 9 |
| tw (L) | Pulse Width (Low) | VCC=5.0V | | 2, 4 | $\overline{C}$Dn to $\overline{S}$Dn | 15.0 | | ns | 9 |
| tw (H) | Pulse Width (High) | VCC=5.0V | | 2, 4 | CPn | 18.0 | | ns | 9 |
| tw (L) 2 | Pulse Width (Low) | VCC=5.0V | | 2, 4 | CPn | 15.0 | | ns | 9 |
| fMAX | Clock Frequency | VCC=5.0V | | 2, 4 | CPn | 30.0 | | MHZ | 9 |

# Electrical Characteristics

## AC PARAMETER - 50pF

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: CL=50pF, RL=2k ohms Temp range: -55C to +125C

| SYMBOL | PARAMETER | CONDITIONS | NOTES | PIN-NAME | MIN | MAX | UNIT | SUB-GROUPS |
|---|---|---|---|---|---|---|---|---|
| tpLH | Propagation Delay | VCC=5.0V | 5 | CPn to Qn/$\overline{Qn}$ | 2.0 | 30.0 | ns | 9 |
| | | | 5 | CPn to Qn/$\overline{Qn}$ | 2.0 | 39.0 | ns | 10, 11 |
| tpHL | Propagation Delay | VCC=5.0V | 5 | CPn to Qn/$\overline{Qn}$ | 2.0 | 46.0 | ns | 9 |
| | | | 5 | CPn to Qn/$\overline{Qn}$ | 2.0 | 59.0 | ns | 10, 11 |
| tpLH (2) | Propagation Delay | VCC=5.0V CP=High | 5 | $\overline{CDn}$/$\overline{SDn}$ to Q/ | 2.0 | 30.0 | ns | 9 |
| | | | 5 | $\overline{CDn}$/$\overline{SDn}$ to Q/ | 2.0 | 39.0 | ns | 10, 11 |
| tpHL (2) | Propagation Delay | VCC=5.0V CP=High | 5 | $\overline{CDn}$/$\overline{SDn}$ to Q/ | 2.0 | 46.0 | ns | 9 |
| | | | 5 | $\overline{CDn}$/$\overline{SDn}$ to Q/ | 2.0 | 59.0 | ns | 10, 11 |
| tpLH (3) | Propagation Delay | VCC=5.0V CP=Low | 5 | $\overline{CDn}$/$\overline{SDn}$ to Q/ | 2.0 | 30.0 | ns | 9 |
| | | | 5 | $\overline{CDn}$/$\overline{SDn}$ to Q/ | 2.0 | 39.0 | ns | 10, 11 |
| tpHL (3) | Propagation Delay | VCC=5.0V CP=Low | 5 | $\overline{CDn}$/$\overline{SDn}$ to Q/ | 2.0 | 46.0 | ns | 9 |
| | | | 5 | $\overline{CDn}$/$\overline{SDn}$ to Q/ | 2.0 | 59.0 | ns | 10, 11 |
| ts (H) | Setup Time (High) | VCC=5.0V @ Room | 5 | Dn to CPn | 20.0 | | ns | 9, 10, 11 |
| ts (L) | Setup Time (Low) | VCC=5.0V @ Room | 5 | Dn to CPn | 20.0 | | ns | 9, 10, 11 |
| th (H) | Hold Time (High) | VCC=5.0V @ Room | 5 | Dn to CPn | 5.0 | | ns | 9, 10, 11 |
| th (L) | Hold Time (Low) | VCC=5.0V @ Room | 5 | Dn to CPn | 5.0 | | NS | 9, 10, 11 |
| tw (L) | Pulse Width (Low) | VCC=5.0V @ Room | 5 | $\overline{CDn}$ to $\overline{SDn}$ | 35.0 | | ns | 9, 10, 11 |
| tw (H) | Pulse Width (High) | VCC=5.0V @ Room | 5 | CPn | 30.0 | | ns | 9, 10, 11 |
| tw (L) | Pulse Width (Low) | VCC=5.0V @ Room | 5 | CPn | 30.0 | | ns | 9, 10, 11 |
| fMAX | Clock Frequency | VCC=5.0V @ Room | 5 | CPn | 20.0 | | MHZ | 9, 10, 11 |

*(Continued)*

Note 1: Screen tested 100% on each device at -55C, +25C & +125C temperature, subgroups A1, 2, 3, 7 & 8.
Note 2: Screen tested 100% on each device at +25C temperature only, subgroup A9.
Note 3: Sample tested (Method 5005, Table 1) on each MFG. lot at +25C, +125C & -55C temperature, subgroups A1, 2, 3, 7 & 8.
Note 4: Sample tested (Method 5005, Table 1) on each MFG. lot at +25C, subgroup A9.
Note 5: Guaranteed, not tested.

# Revision History

| Rev | ECN # | Rel Date | Originator | Changes |
|---|---|---|---|---|
| 1A0 | M0001611 | 08/24/98 | Linda Collins | Initial MDS release: MNDM54LS74-X Rev. 1A0. Added note 4 to the AC (15pF) notes reference column. Deleted the phrase 'and periodically at +125C & -55C, subgroups 10 & 11' from note 4. |