National Semiconductor

DM54L164A/DM74L164A 8-Bit Serial In/Parallel Out Shift Registers

General Description

These 8-bit shift registers feature gated serial inputs and an asynchronous clear. A low logic level at either input inhibits entry of the new data, and resets the first flip-flop to the low level at the next clock pulse, thus providing complete control over incoming data. A high logic level on either input enables the other input, which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high level transition of the clock input.

Features

- Gated (enable/disable) serial inputs
- Fully buffered clock and serial inputs
- Asynchronous clear
- Typical clock frequency 14 MHz
- Typical power dissipation 30 mW

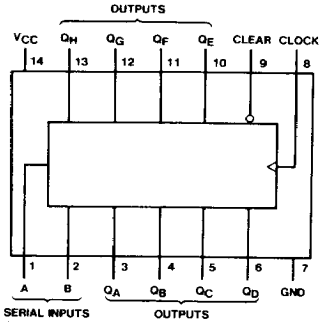
Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6641-1

54L164A (J) **74L164A (N)**

Function Table

Inputs				Outputs			
Clear	Clock	A	B	Q_A	Q_B	...	Q_H
L	X	X	X	L	L	...	L
H	L	X	X	Q_{A0}	Q_{B0}	...	Q_{H0}
H	↑	H	H	H	Q_{An}	...	Q_{Gn}
H	↑	L	X	L	Q_{An}	...	Q_{Gn}
H	↑	X	L	L	Q_{An}	...	Q_{Gn}

H = High Level (steady state), L = Low Level (steady state)

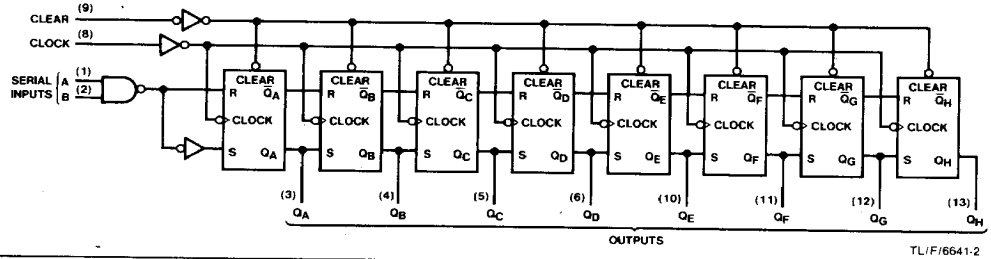
X = Don't Care (any input, including transitions)

↑ = Transition from low to high level

Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Gn} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicates a one-bit shift.

Logic Diagram



TL/F/6641-2

Recommended Operating Conditions

Sym	Parameter		DM54L164A			DM74L164A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.7	V
I_{OH}	High Level Output Current				−0.2			−0.2	mA
I_{OL}	Low Level Output Current				2			3.6	mA
f_{CLK}	Clock Frequency		0		6	0		6	MHz
t_W	Pulse Width	Clock	60	40		60	40		ns
		Clear	60	40		60	40		
t_{SU}	Data Setup Time		40	20		40	20		ns
t_H	Data Hold Time		20	−5		20	−5		ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max V_I = 5.5V	Clear			0.2	mA
			Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Clear			20	μA
			Others			10	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.3V	Clear			−0.36	mA
			Others			−0.18	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			6	9	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

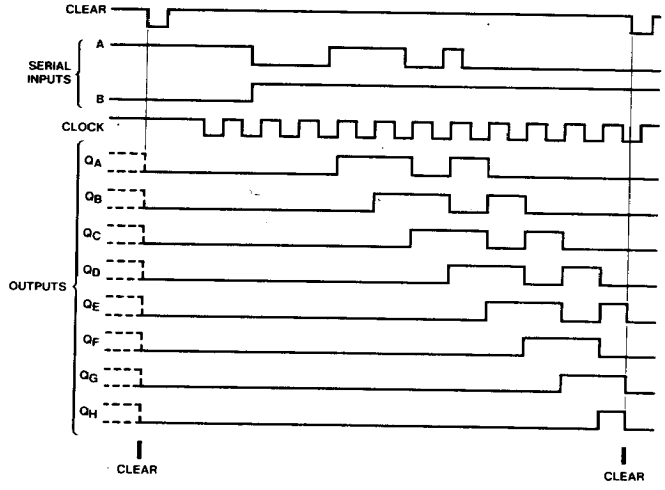
Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with outputs open, SERIAL inputs grounded, the CLOCK input at 2.4V, and a momentary ground, then 4.5V, applied to the CLEAR input.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 4\ k\Omega$, $C_L = 50\ pF$			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		6	14		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Clock to Output		50	85	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clock to Output		90	135	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Output		75	120	ns

Timing Diagram



TL/F/6641-3

7