

## CD4031BM/CD4031BC 64-Stage Static Shift Register

### General Description

The CD4031BM/CD4031BC is an integrated, complementary MOS (CMOS), 64-stage, fully static shift register. Two data inputs, DATA IN and RECIRCULATE IN, and a MODE CONTROL input are provided. Data at the DATA input (when MODE CONTROL is low) or data at the RECIRCULATE input (when MODE CONTROL is high), which meets the setup and hold time requirements, is entered into the first stage of the register and is shifted one stage at each positive transition of the CLOCK.

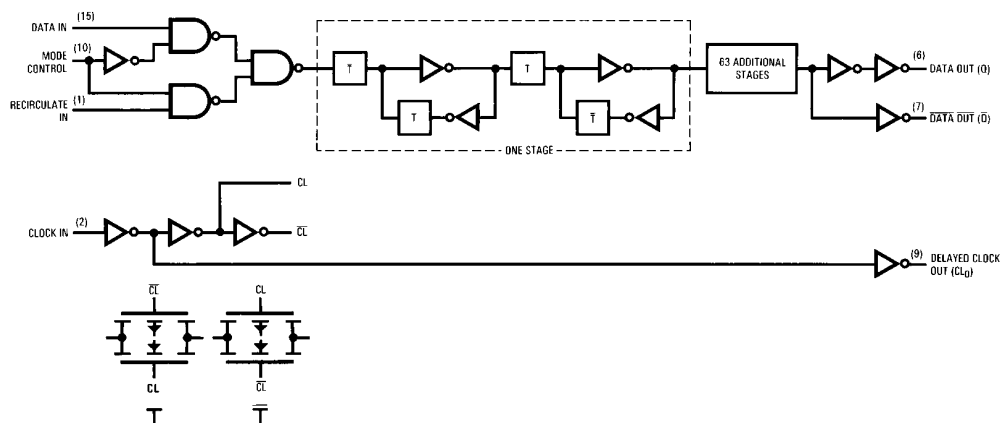
Data output is available in both true and complement forms from the 64th stage. Both the DATA OUT (Q) AND  $\overline{\text{DATA OUT}}$  ( $\overline{Q}$ ) outputs are fully buffered.

The CLOCK input of the CD4031BM/CD4031BC is fully buffered, and present only a standard input load capacitance. However, a DELAYED CLOCK OUTPUT ( $\text{CL}_D$ ) has been provided to allow reduced clock drive fan-out and transition time requirements when cascading packages.

### Features

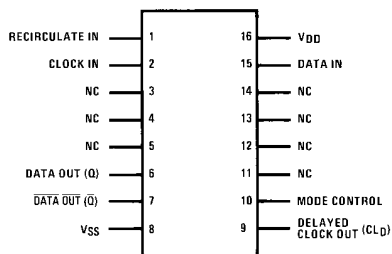
- Wide supply voltage range 3.0V to 15V
- High noise immunity 0.45  $V_{DD}$  (typ.)
- Low power TTL compatibility fan out of 2 driving 74L or 1 driving 74LS
- Fully static operation DC to 8 MHz
- Fully buffered clock input  $V_{DD} = 10V$  (typ.)
- Single phase clocking requirements 5 pF (typ.) input capacitance
- Delayed clock output for reduced clock drive requirements
- Fully buffered outputs
- High current sinking capability 1.6 mA @  $V_{DD} = 5V$  and 25°C
- Q output

### Logic and Connection Diagrams



TL/F/5962-1

### Dual-In-Line Package



Top View

TL/F/5962-2

Order Number CD4031B

**Absolute Maximum Ratings** (Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

|                                           |                          |
|-------------------------------------------|--------------------------|
| Supply Voltage ( $V_{DD}$ )               | −0.5V to +18V            |
| Input Voltage ( $V_{IN}$ )                | −0.5V to $V_{DD}$ + 0.5V |
| Storage Temperature Range ( $T_S$ )       | −65°C to +150°C          |
| Power Dissipation ( $P_D$ )               |                          |
| Dual-In-Line                              | 700 mW                   |
| Small Outline                             | 500 mW                   |
| Lead Temp. ( $T_L$ ) (Soldering, 10 sec.) | 260°C                    |

**Recommended Operating Conditions** (Note 2)

|                                       |                 |
|---------------------------------------|-----------------|
| Supply Voltage ( $V_{DD}$ )           | 3V to 15V       |
| Input Voltage ( $V_{IN}$ )            | 0V to $V_{DD}$  |
| Operating Temperature Range ( $T_A$ ) |                 |
| CD4031BM                              | −55°C to +125°C |
| CD4031BC                              | −40°C to +85°C  |

**DC Electrical Characteristics** (Note 2) CD4031BM

| Symbol   | Parameter                                                       | Conditions                                                                                                                                                    | −55°C                 |                      | +25°C                 |                                       |                      | +125°C                |                      | Units                         |
|----------|-----------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|----------------------|-----------------------|---------------------------------------|----------------------|-----------------------|----------------------|-------------------------------|
|          |                                                                 |                                                                                                                                                               | Min                   | Max                  | Min                   | Typ                                   | Max                  | Min                   | Max                  |                               |
| $I_{DD}$ | Quiescent Device Current                                        | $V_{DD} = 5V, V_{IN} = V_{DD} \text{ or } V_{SS}$<br>$V_{DD} = 10V, V_{IN} = V_{DD} \text{ or } V_{SS}$<br>$V_{DD} = 15V, V_{IN} = V_{DD} \text{ or } V_{SS}$ |                       | 5<br>10<br>20        |                       | 0.01<br>0.01<br>0.02                  | 5<br>10<br>20        |                       | 150<br>300<br>600    | $\mu A$<br>$\mu A$<br>$\mu A$ |
| $V_{OL}$ | Low Level Output Voltage                                        | $V_{DD} = 5V$<br>$V_{DD} = 10V$<br>$V_{DD} = 15V$ } $V_{IH} = V_{DD}, V_{IL} = 0V,  I_O  < 1 \mu A$                                                           |                       | 0.05<br>0.05<br>0.05 |                       | 0<br>0<br>0                           | 0.05<br>0.05<br>0.05 |                       | 0.05<br>0.05<br>0.05 | V<br>V<br>V                   |
| $V_{OH}$ | High Level Output Voltage                                       | $V_{DD} = 5V$<br>$V_{DD} = 10V$<br>$V_{DD} = 15V$ } $V_{IH} = V_{DD}, V_{IL} = 0V,  I_O  < 1 \mu A$                                                           | 4.95<br>9.95<br>14.95 |                      | 4.95<br>9.95<br>14.95 | 5<br>10<br>15                         |                      | 4.95<br>9.95<br>14.95 |                      | V<br>V<br>V                   |
| $V_{IL}$ | Low Level Input Voltage                                         | $V_{DD} = 5V, V_O = 0.5V \text{ or } 4.5V$<br>$V_{DD} = 10V, V_O = 1.0V \text{ or } 9.0V$<br>$V_{DD} = 15V, V_O = 1.5V \text{ or } 13.5V$ } $ I_O  < 1 \mu A$ |                       | 1.5<br>3.0<br>4.0    |                       | 2.25<br>4.5<br>6.75                   | 1.5<br>3.0<br>4.0    |                       | 1.5<br>3.0<br>4.0    | V<br>V<br>V                   |
| $V_{IH}$ | High Level Input Voltage                                        | $V_{DD} = 5V, V_O = 0.5V \text{ or } 4.5V$<br>$V_{DD} = 10V, V_O = 1.0V \text{ or } 9.0V$<br>$V_{DD} = 15V, V_O = 1.5V \text{ or } 13.5V$ } $ I_O  < 1 \mu A$ | 3.5<br>7.0<br>11.0    |                      | 3.5<br>7.0<br>11.0    | 2.75<br>5.5<br>8.25                   |                      | 3.5<br>7.0<br>11.0    |                      | V<br>V<br>V                   |
| $I_{OL}$ | Low Level Output Current, Q Output (Note 3)                     | $V_{DD} = 5V, V_O = 0.4V$<br>$V_{DD} = 10V, V_O = 0.5V$<br>$V_{DD} = 15V, V_O = 1.5V$ } $V_{IH} = V_{DD}$<br>$V_{IL} = 0V$                                    | 2.3<br>5.1<br>10.5    |                      | 1.9<br>4.2<br>8.8     | 3.8<br>8.4<br>17                      |                      | 1.3<br>2.8<br>6.1     |                      | mA<br>mA<br>mA                |
| $I_{OL}$ | Low Level Output Current, $\bar{Q}$ and $CL_D$ Outputs (Note 3) | $V_{DD} = 5V, V_O = 0.4V$<br>$V_{DD} = 10V, V_O = 0.5V$<br>$V_D = 15V, V_O = 1.5V$ } $V_{IH} = V_{DD}$<br>$V_{IL} = 0V$                                       | 0.64<br>1.6<br>4.2    |                      | 0.51<br>1.3<br>3.4    | 0.88<br>2.25<br>8.8                   |                      | 0.36<br>0.9<br>2.4    |                      | mA<br>mA<br>mA                |
| $I_{OH}$ | High Level Output Current, All Outputs (Note 3)                 | $V_{DD} = 5V, V_O = 4.6V$<br>$V_{DD} = 10V, V_O = 9.5V$<br>$V_{DD} = 15V, V_O = 13.5V$ } $V_{IH} = V_{DD}$<br>$V_{IL} = 0V$                                   | −0.64<br>−1.6<br>−4.2 |                      | −0.51<br>−1.3<br>−3.4 | −0.88<br>−2.25<br>−8.8                |                      | −0.36<br>−0.9<br>−2.4 |                      | mA<br>mA<br>mA                |
| $I_{IN}$ | Input Current                                                   | $V_{DD} = 15V, V_{IN} = 0V$<br>$V_{DD} = 15V, V_{IN} = 15V$                                                                                                   |                       | −0.1<br>0.1          |                       | −10 <sup>−5</sup><br>10 <sup>−5</sup> | −0.1<br>0.1          |                       | −1.0<br>1.0          | $\mu A$<br>$\mu A$            |

**Truth Tables****Mode Control (Data Selection)**

| Mode Control | Data In | Recirculate In | Data Into First Stage |
|--------------|---------|----------------|-----------------------|
| 0            | 0       | X              | 0                     |
| 0            | 1       | X              | 1                     |
| 1            | X       | 0              | 0                     |
| 1            | X       | 1              | 1                     |

**Each Stage**

| $D_n$ | CL                                                                                  | $Q_n$ |
|-------|-------------------------------------------------------------------------------------|-------|
| 0     |  | 0     |
| 1     |  | 1     |
| X     |  | NC    |

X = irrelevant    NC = no change     = Low to High level transition     = High to Low level transition

## DC Electrical Characteristics (Note 2) CD4031BC

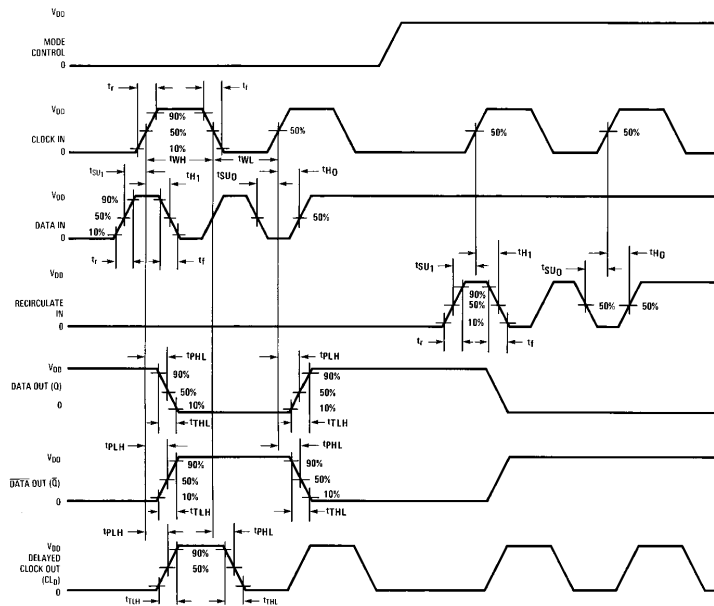
| Symbol   | Parameter                                                       | Conditions                                                                                                                                                     | −40°C                 |                      | +25°C                 |                                       |                      | +85°C                 |                      | Units   |
|----------|-----------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|----------------------|-----------------------|---------------------------------------|----------------------|-----------------------|----------------------|---------|
|          |                                                                 |                                                                                                                                                                | Min                   | Max                  | Min                   | Typ                                   | Max                  | Min                   | Max                  |         |
| $I_{DD}$ | Quiescent Device Current                                        | $V_{DD} = 5V, V_{IN} = V_{DD} \text{ or } V_{SS}$<br>$V_{DD} = 10V, V_{IN} = V_{DD} \text{ or } V_{SS}$<br>$V_{DD} = 15V, V_{IN} = V_{DD} \text{ or } V_{SS}$  |                       | 20<br>40<br>80       |                       | 0.01<br>0.01<br>0.02                  | 20<br>40<br>80       |                       | 150<br>300<br>600    | $\mu A$ |
| $V_{OL}$ | Low Level Output Voltage                                        | $V_{DD} = 5V$<br>$V_{DD} = 10V$<br>$V_{DD} = 15V$<br>$V_{IH} = V_{DD}, V_{IL} = 0V,  I_O  < 1 \mu A$                                                           |                       | 0.05<br>0.05<br>0.05 |                       | 0<br>0<br>0                           | 0.05<br>0.05<br>0.05 |                       | 0.05<br>0.05<br>0.05 | V       |
| $V_{OH}$ | High Level Output Voltage                                       | $V_{DD} = 5V$<br>$V_{DD} = 10V$<br>$V_{DD} = 15V$<br>$V_{IH} = V_{DD}, V_{IL} = 0V,  I_O  < 1 \mu A$                                                           | 4.95<br>9.95<br>14.95 |                      | 4.95<br>9.95<br>14.95 | 5<br>10<br>15                         |                      | 4.95<br>9.95<br>14.95 |                      | V       |
| $V_{IL}$ | Low Level Input Voltage                                         | $V_{DD} = 5V, V_O = 0.5V \text{ or } 4.5V$<br>$V_{DD} = 10V, V_O = 1.0V \text{ or } 9.0V$<br>$V_{DD} = 15V, V_O = 1.5V \text{ or } 13.5V$<br>$ I_O  < 1 \mu A$ |                       | 1.5<br>3.0<br>4.0    |                       | 2.25<br>4.5<br>6.75                   | 1.5<br>3.0<br>4.0    |                       | 1.5<br>3.0<br>4.0    | V       |
| $V_{IH}$ | High Level Input Voltage                                        | $V_{DD} = 5V, V_O = 0.5V \text{ or } 4.5V$<br>$V_{DD} = 10V, V_O = 1.0V \text{ or } 9.0V$<br>$V_{DD} = 15V, V_O = 1.5V \text{ or } 13.5V$<br>$ I_O  < 1 \mu A$ | 3.5<br>7.0<br>11.0    |                      | 3.5<br>7.0<br>11.0    | 2.75<br>5.5<br>8.25                   |                      | 3.5<br>7.0<br>11.0    |                      | V       |
| $I_{OL}$ | Low Level Output Current, Q Output (Note 3)                     | $V_{DD} = 5V, V_O = 0.4V$<br>$V_{DD} = 10V, V_O = 0.5V$<br>$V_{DD} = 15V, V_O = 1.5V$<br>$V_{IH} = V_{DD}$<br>$V_{IL} = 0V$                                    | 1.8<br>4.0<br>8.7     |                      | 1.6<br>3.5<br>7.5     | 3.8<br>8.4<br>17                      |                      | 1.3<br>2.8<br>6.1     |                      | mA      |
| $I_{OL}$ | Low Level Output Current, $\bar{Q}$ and $CL_D$ Outputs (Note 3) | $V_{DD} = 5V, V_O = 0.4V$<br>$V_{DD} = 10V, V_O = 0.5V$<br>$V_{DD} = 15V, V_O = 1.5V$<br>$V_{IH} = V_{DD}$<br>$V_{IL} = 0V$                                    | 0.52<br>1.3<br>3.6    |                      | 0.44<br>1.1<br>3.0    | 0.88<br>2.25<br>8.8                   |                      | 0.36<br>0.9<br>2.4    |                      | mA      |
| $I_{OH}$ | High Level Output Current, All Outputs (Note 3)                 | $V_{DD} = 5V, V_O = 4.6V$<br>$V_{DD} = 10V, V_O = 9.5V$<br>$V_{DD} = 15V, V_O = 13.5V$<br>$V_{IH} = V_{DD}$<br>$V_{IL} = 0V$                                   | −0.52<br>−1.3<br>−3.0 |                      | −0.44<br>−1.1<br>−3.0 | −0.88<br>−2.25<br>−8.8                |                      | −0.36<br>−0.9<br>−2.4 |                      | mA      |
| $I_{IN}$ | Input Current                                                   | $V_{DD} = 15V, V_{IN} = 0V$<br>$V_{DD} = 15V, V_{IN} = 15V$                                                                                                    |                       | −0.3<br>0.3          |                       | −10 <sup>−5</sup><br>10 <sup>−5</sup> | −0.3<br>0.3          |                       | −1.0<br>1.0          | $\mu A$ |

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

**Note 2:**  $V_{SS} = 0V$  unless otherwise specified.

**Note 3:**  $I_{OH}$  and  $I_{OL}$  are tested one output at a time.

## Switching Time Waveforms



TL/F/5962-3

## AC Electrical Characteristics\*

$T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$ ,  $R_L = 200\text{ k}$ , Input  $t_r = t_f = 20\text{ ns}$ , unless otherwise specified

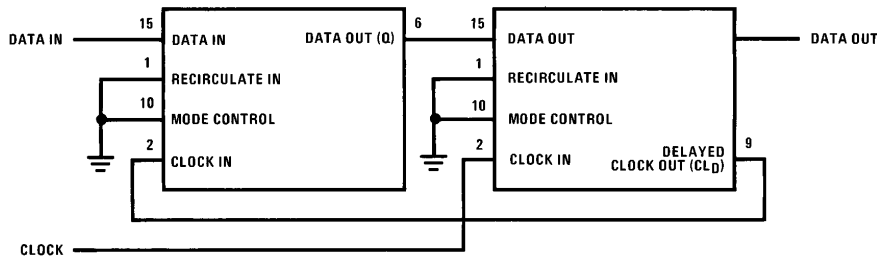
| Symbol                               | Parameter                                                   | Conditions                                                                                  | Min               | Typ               | Max               | Units                                           |
|--------------------------------------|-------------------------------------------------------------|---------------------------------------------------------------------------------------------|-------------------|-------------------|-------------------|-------------------------------------------------|
| $t_{\text{PHL}}$ , $t_{\text{PLH}}$  | Propagation Delay Time, Clock to Q and $\bar{Q}$            | $V_{\text{CC}} = 5\text{V}$<br>$V_{\text{CC}} = 10\text{V}$<br>$V_{\text{CC}} = 15\text{V}$ |                   | 300<br>125<br>100 | 600<br>250<br>200 | ns<br>ns<br>ns                                  |
| $t_{\text{PHL}}$ , $t_{\text{PLH}}$  | Propagation Delay Time, Clock to $\text{CL}_D$              | $V_{\text{CC}} = 5\text{V}$<br>$V_{\text{CC}} = 10\text{V}$<br>$V_{\text{CC}} = 15\text{V}$ |                   | 125<br>60<br>50   | 250<br>125<br>100 | ns<br>ns<br>ns                                  |
| $t_{\text{THL}}$ , $t_{\text{TLH}}$  | Output Transition Time, All Outputs                         | $V_{\text{CC}} = 5\text{V}$<br>$V_{\text{CC}} = 10\text{V}$<br>$V_{\text{CC}} = 15\text{V}$ |                   | 100<br>50<br>40   | 200<br>100<br>80  | ns<br>ns<br>ns                                  |
| $t_{\text{SU}0}$<br>$t_{\text{SU}1}$ | Minimum Data Setup Time, DATA IN or RECIRCULATE IN to Clock | $V_{\text{CC}} = 5\text{V}$<br>$V_{\text{CC}} = 10\text{V}$<br>$V_{\text{CC}} = 15\text{V}$ |                   | 100<br>50<br>40   | 200<br>100<br>80  | ns<br>ns<br>ns                                  |
| $t_{\text{H}0}$<br>$t_{\text{H}1}$   | Minimum Data Hold Time, Clock to DATA IN or RECIRCULATE IN  | $V_{\text{CC}} = 5\text{V}$<br>$V_{\text{CC}} = 10\text{V}$<br>$V_{\text{CC}} = 15\text{V}$ |                   | 100<br>50<br>40   | 200<br>100<br>80  | ns<br>ns<br>ns                                  |
| $t_{\text{WL}}$ , $t_{\text{WH}}$    | Minimum Clock Pulse Width                                   | $V_{\text{CC}} = 5\text{V}$<br>$V_{\text{CC}} = 10\text{V}$<br>$V_{\text{CC}} = 15\text{V}$ |                   | 150<br>60<br>50   | 30<br>125<br>100  | ns<br>ns<br>ns                                  |
| $f_{\text{CL}}$                      | Maximum Clock Frequency                                     | $V_{\text{CC}} = 5\text{V}$<br>$V_{\text{CC}} = 10\text{V}$<br>$V_{\text{CC}} = 15\text{V}$ | 1.6<br>4.0<br>5.0 | 3.2<br>8.0<br>10  |                   | MHz<br>MHz<br>MHz                               |
| $t_{\text{RCL}}$ , $t_{\text{FCL}}$  | Maximum Clock Input Rise and Fall Times (Note 4)            | $V_{\text{CC}} = 5\text{V}$<br>$V_{\text{CC}} = 10\text{V}$<br>$V_{\text{CC}} = 15\text{V}$ | 15<br>10<br>5     |                   |                   | $\mu\text{s}$<br>$\mu\text{s}$<br>$\mu\text{s}$ |
| $C_{\text{IN}}$                      | Input Capacitance                                           | Any Input                                                                                   |                   | 5                 | 7.5               | pF                                              |

\*AC Parameters are guaranteed by DC correlated testing.

**Note 4:** When clocking cascaded packages in parallel, one should insure that:  $t_{\text{r CL}} \leq 2(t_{\text{PD}} - t_{\text{H}})$  where:  $t_{\text{PD}}$  = the propagation delay of the driving stage and  $t_{\text{H}}$  = the hold time of the driven stage.

## Block Diagram

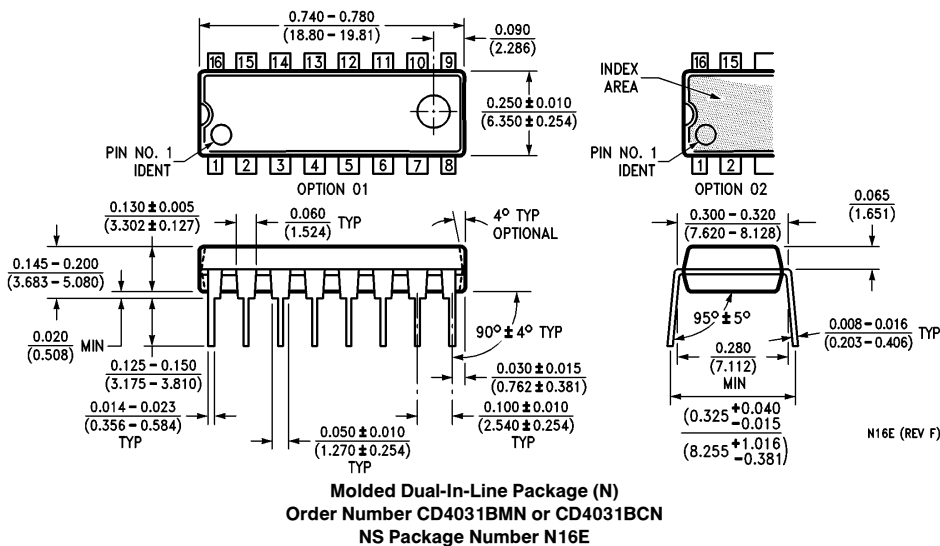
cascading packages using DELAYED CLOCK ( $\text{CL}_D$ ) output



TL/F/5962-4

J16A (REV L)

## Physical Dimensions inches (millimeters) (Continued)



### LIFE SUPPORT POLICY

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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