National Semiconductor

LH0032
Ultra Fast FET-Input Operational Amplifier

General Description

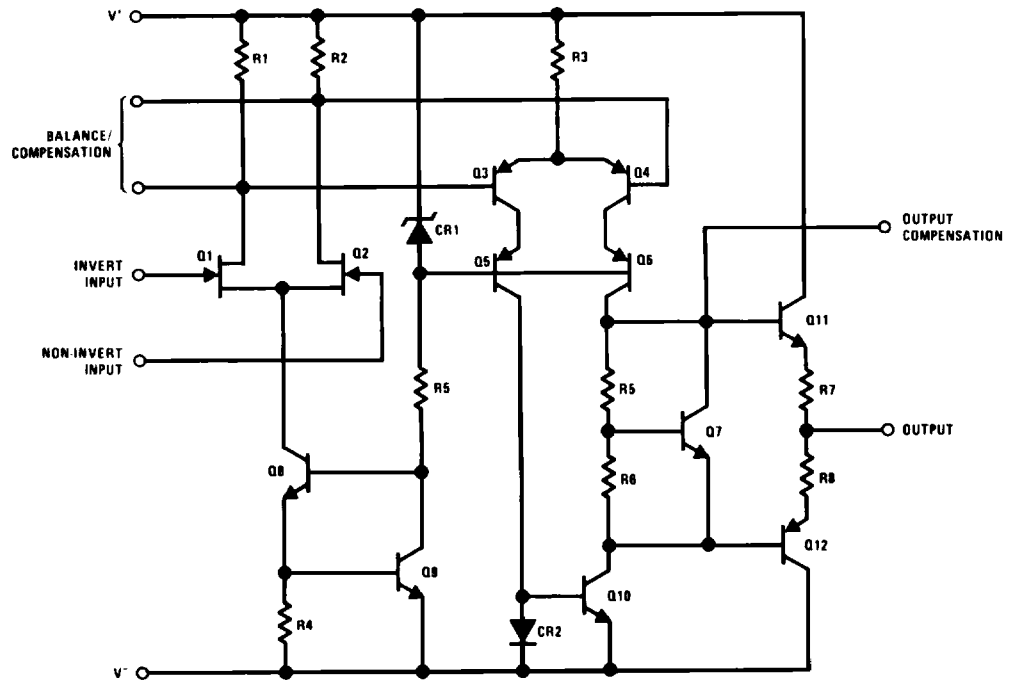
The LH0032 is a high slew rate, high input impedance differential operational amplifier suitable for diverse applications in fast signal handling. The high allowable differential input voltage, ease of output clamping, and high output drive capability particularly suit it for comparator applications. It may be used in applications normally reserved for video amplifiers allowing the use of operational gain setting and frequency response shaping into the megahertz region.

The LH0032's wide bandwidth, high input impedance and high output capacity make it an ideal choice for applications such as summing amplifiers in high speed D to A converters, buffers in data acquisition systems and sample and hold circuits. Additional applications include high speed integrators and video amplifiers. The LH0032 is guaranteed for operation over the temperature range −55°C to +125°C, the LH0032C is guaranteed for −25°C to +85°C.

Features

- 500 V/μs slew rate
- 70 MHz bandwidth
- $10^{12}\Omega$ input impedance
- As low as 2 mV max input offset voltage
- FET input
- Peak output current to 100 mA

Schematic



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Absolute Maximum Ratings (Note 9)

Supply Voltage, V_S	±18V
Input Voltage, V_{IN}	$\pm V_S$
Differential Input Voltage	±30V or $\pm 2V_S$
Power Dissipation, P_D	(Note 10)
Steady State Output Current	±100 mA
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	300°C

Operating Ratings

Temperature Range, T_A	
LH0032G	−55°C to +125°C
LH0032CG	−25°C to +85°C
Junction Temperature, T_J	
LH0032G	+175°C
Thermal Resistance (Note 8)	
θ_{JA} G Package	100°C/W
θ_{JC} G Package	70°C/W

DC Electrical Characteristics $V_S = \pm 15V$, $T_{MIN} \le T_A \le T_{MAX}$ unless otherwise noted (Note 2) ($T_A = T_J$)

Symbol	Parameter	Test Conditions		LH0032			LH0032C			Units
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$V_{IN} = 0$	$T_A = T_J = 25°C$ (Note 3)		2	5 10		2	15 20	mV
$\Delta V_{OS}/\Delta T$	Average Offset Voltage Drift		(Note 4)		15	50		15	50	µV/°C
I_{OS}	Input Offset Current		$T_J = 25°C$ (Note 3) $T_A = 25°C$ (Note 5)			25 250 25			50 500 5	pA pA nA
I_B	Input Bias Current		$T_J = 25°C$ (Note 3) $T_A = 25°C$ (Note 5)			100 1 50			500 5 15	pA nA nA
*V_{INCM}	Input Voltage Range			±10	±12		±10	±12		V
CMRR	Common Mode Rejection Ratio	$\Delta V_{IN} = \pm 10V$		50	60		50	60		dB
A_{VOL}	Open-Loop Voltage Gain	$V_O = \pm 10V$, f = 1 kHz, R_L = 1 kΩ (Note 6)	$T_J = 25°C$	60	70		60	70		dB
				57			57			
V_O	Output Voltage Swing	R_L = 1 kΩ		±10	±13.5		±10	±13		V
I_S	Power Supply Current	$T_A = 25°C$, $I_O = 0$ (Note 5)			18	20		20	22	mA
PSRR	Power Supply Rejection Ratio	$\Delta V_S = 10V$ (±5 to ±15V)		50	60		50	60		dB

*Guaranteed by CMRR test condition.

AC Electrical Characteristics $V_S = \pm 15V$, $R_L = 1k\Omega$, $T_J = 25°C$ (Note 7)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
S_R	Slew Rate	$A_V = +1$	$\Delta V_{IN} = 20V$	350	500		V/μs
t_s	Settling Time to 1% of Final Value	$A_V = -1$,			100		ns
t_s	Settling Time to 0.1% of Final Value				300		ns
t_R	Small Signal Rise Time	$A_V = +1$, $\Delta V_{IN} = 1V$			8	20	
t_D	Small Signal Delay Time				10	25	

Note 1: In order to limit maximum junction temperature to +175°C, it may be necessary to operate with VS < ±15V when T_A or T_C exceeds specific values depending on the P_D within the device package. Total P_D is the sum of quiescent and load-related dissipation. See applications notes AN-277, "Applications of Wide-Band Buffer Amplifiers" and AN-253, "High-Speed Operational-Amplifier Applications" for a discussion of load-related power dissipation.

Note 2: LH0032G is 100% production tested as specified at 25°C, 125°C, and −55°C. LH0032CG is 100% production tested at 25°C only. Specifications at temperature extremes are verified by sample testing, but these limits are not used to calculate outgoing quality level.

Note 3: Specification is at 25°C junction temperature due to requirements of high-speed automatic testing. Actual values at operating temperature will exceed the value at $T_J = 25$ C. When supply voltages are ± 15V, no-load operating junction temperature may rise 40–60°C above ambient, and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_B and I_{OS} will change significantly during warm-up. Refer to I_B and I_{OS} vs. temperature graph for expected values.

Note 4: LH0032G is 100% production tested for this parameter. LH0032CG is sample tested only. Limits are not used to calculate outgoing quality levels. $\Delta V_{OS}/\Delta T$ is the average value calculated from measurements at 25°C and T_{MAX}.

Note 5: Measured in still air 7 minutes after application of power. Guaranteed thru correlated automatic pulse testing.

Note 6: Guaranteed thru correlated automatic pulse testing at $T_J = 25°C$.

Note 7: Not 100% production tested; verified by sample testing only. Limits are not used to calculate outgoing quality level.

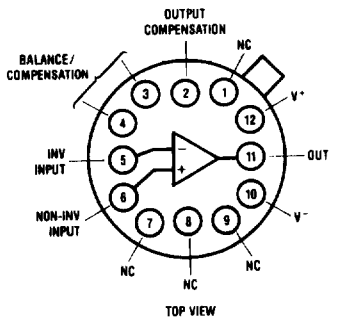
Note 8: For operating at elevated temperatures, the device must be derated based on the thermal resistance θ_{JA} and T_J max. $T_J = T_A + P_D\theta_{JA}$.

Note 9: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 10: The maximum power dissipation is a function of maximum junction temperature T_J max, total thermal resistance θ_{JA}, and ambient temperature T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_J \text{ max} - T_A)/\theta_{JA}$.

Note 11: See RETS0032X for LH0032G military specifications.

Connection Diagram



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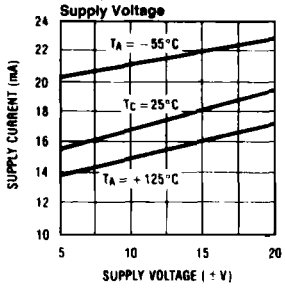
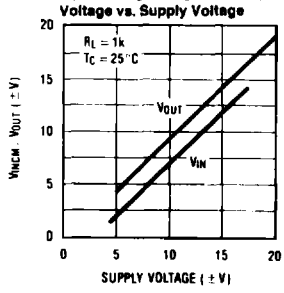
Order Number LH0032G, LH0032G/883 or LH0032CG
See NS Package Number G12B

Typical Performance Characteristics

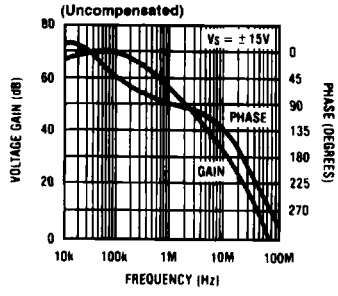
Supply Current vs. Supply Voltage



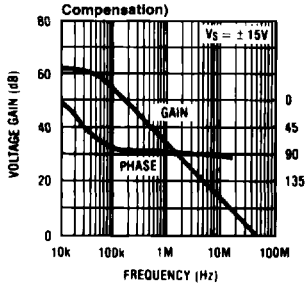
Input Voltage Range and Output Voltage vs. Supply Voltage



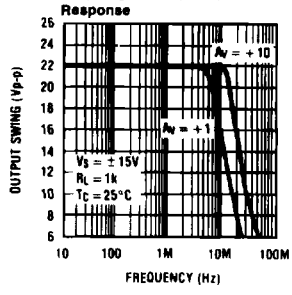
Bode Plot (Uncompensated)



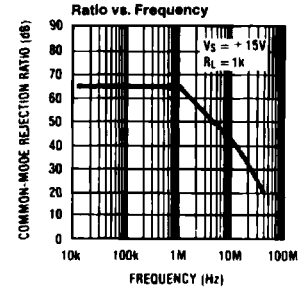
Bode Plot (Unity Gain Compensation)



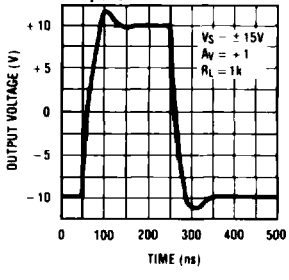
Large Signal Frequency Response



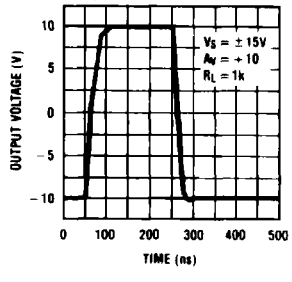
Common Mode Rejection Ratio vs. Frequency



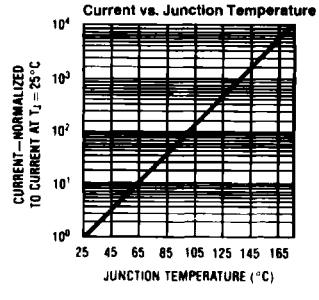
Large Signal Pulse Response



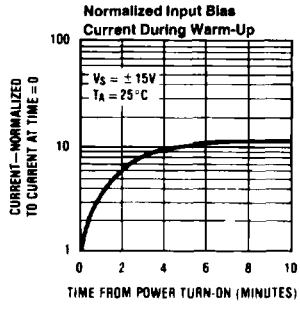
Large Signal Pulse Response



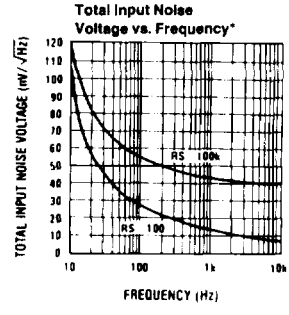
Normalized Input Bias and Offset Current vs. Junction Temperature



Normalized Input Bias Current During Warm-Up



Total Input Noise Voltage vs. Frequency*



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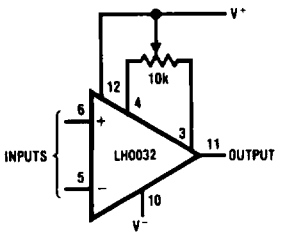
*Noise voltage includes contribution from source resistance.

Auxiliary Circuits

Offset Null



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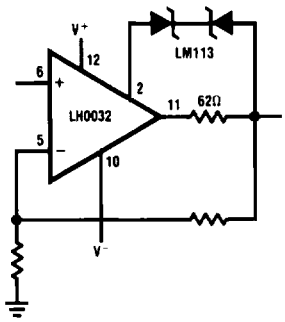
Output Short Circuit Protection



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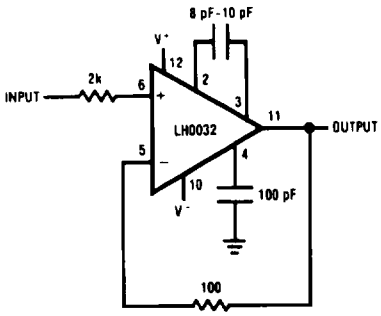
Typical Applications

Unity Gain Amplifier



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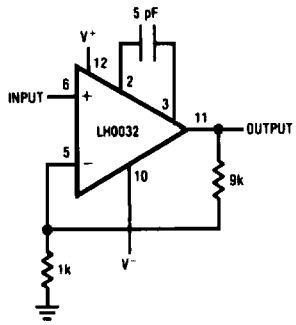
10X Buffer Amplifier



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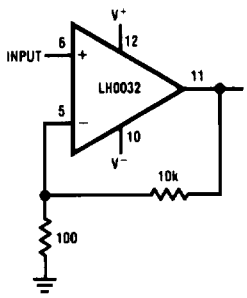
100X Buffer Amplifier



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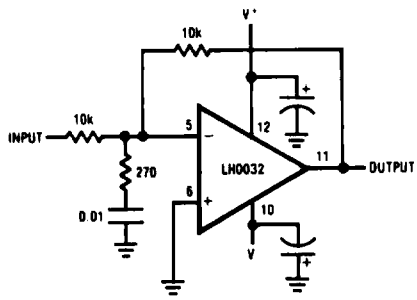
Non-Compensated Unity Gain Inverter



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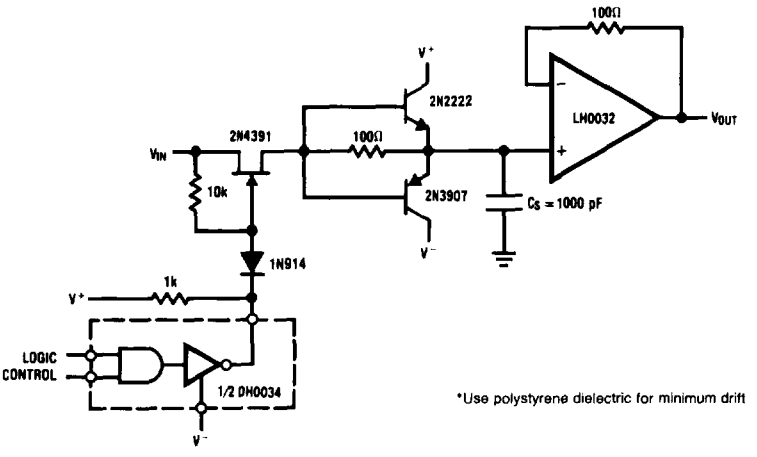
Typical Applications (Continued)

High Speed Sample and Hold



*Use polystyrene dielectric for minimum drift

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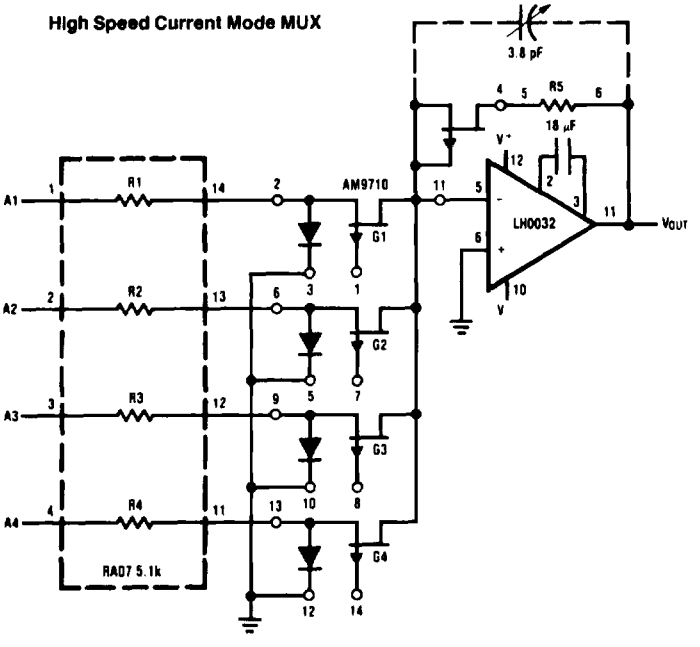
High Speed Current Mode MUX



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Applications Information

POWER SUPPLY DECOUPLING

The LH0032/LH0032A, like most high speed circuits, is sensitive to layout and stray capacitance. Power supplies should be by passed as near to pins 10 and 12 as practicable with low inductance capacitors such as 0.01 µF disc ceramics. Compensation components should also be located close to the appropriate pins to minimize stray reactances.

INPUT CURRENT

Because the input devices are FETs, the input bias current may be expected to double for each 11°C junction temperature rise. This characteristic is plotted in the typical performance characteristics graphs. The device will self-heat due to internal power dissipation after application of power thus raising the FET junction temperature 40–60°C above free-air ambient temperature when supplies are ±15V. The de-

Applications Information (Continued)

vice temperature will stabilize within 5–10 minutes after application of power, and the input bias currents measured at that time will be indicative of normal operating currents. An additional rise would occur as power is delivered to a load due to additional internal power dissipation.

There is an additional effect on input bias current as the input voltage is changed. The effect, common to all FETs, is an avalanche-like increase in gate current as the FET gate-to-drain voltage is increased above a critical value depending on FET geometry and doping levels. This effect will be noted as the input voltage of the LH0032 is taken below ground potential when the supplies are ±15V. All of the effects described here may be minimized by operating the device with $V_S \leq \pm 15V$.

These effects are indicated in the typical performance curves.

INPUT CAPACITANCE

The input capacitance to the LH0032/LH0032C is typically 5pF and thus may form a significant time constant with high value resistors. For optimum performance, the input capacitance to the inverting input should be compensated by a small capacitor across the feedback resistor. The value is strongly dependent on layout and closed loop gain, but will typically be in the neighborhood of several picofarads.

In the non-inverting configuration, it may be advantageous to bootstrap the case and/or a guard conductor to the inverting input. This serves both to divert leakage currents away from the non-inverting input and to reduce the effective input capacitance. A unity gain follower so treated will have an input capacitance under a picofarad.

HEAT SINKING

While the LH0032/LH0032A is specified for operation without any explicit heat sink, internal power dissipation does cause a significant temperature rise. Improved bias current performance can thus be obtained by limiting this temperature rise with a small heat sink such as the Thermalloy No. 2241 or equivalent. The case of the device has no internal connection, so it may be electrically connected to the sink if this is advantageous. Be aware, however, that this will affect the stray capacitances to all pins and may thus require adjustment of circuit compensation values.

For additional applications information request Application Note AN-253.

Compensating the LH0032

With the LH0032, two compensation schemes may be used, depending on the designer's specific needs.

The first technique is shown in *Figure 14*. It offers the best 0.1% settling time for a ±10V square wave input. The compensation capacitors C_C and C_A should be selected from *Figure 15* for various closed-loop gains. *Figure 16* shows how the LH0032 frequency response is modified for different value compensation capacitors.

Although this approach offers the shortest settling time, the falling edge exhibits overshoot up to 30% lasting 200 to 300 ns. *Figure 17* shows the typical pulse response.

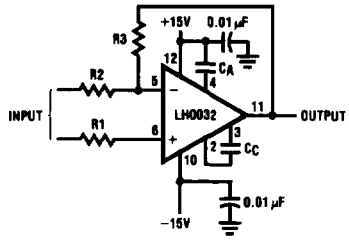

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FIGURE 14. LH0032 Frequency Compensation Circuit

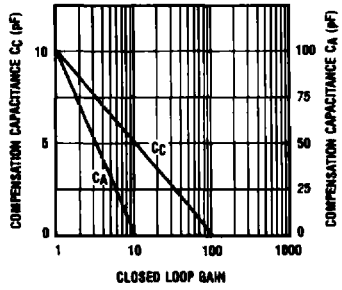

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FIGURE 15. Recommended Value of Compensation Capacitor vs. Closed-Loop Gain for Optimum Settling Time

Applications Information (Continued)

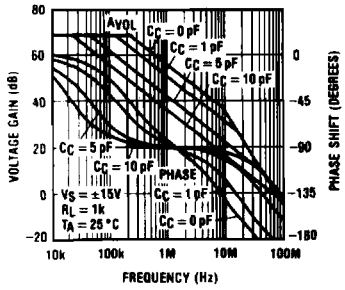

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FIGURE 16. The Effect of Various Compensation Capacitors on LH0032 Open Loop Frequency Response

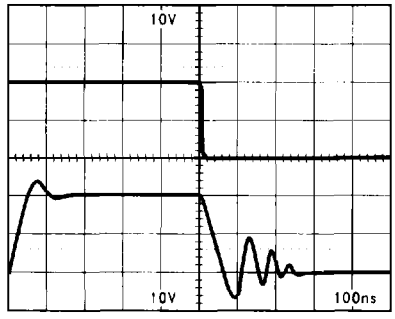

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FIGURE 17. LH0032 Unity Gain Non-Inverting Large Signal Pulse Response: T_A = 25°C, C_C = 10 pF, C_A = 100 pF

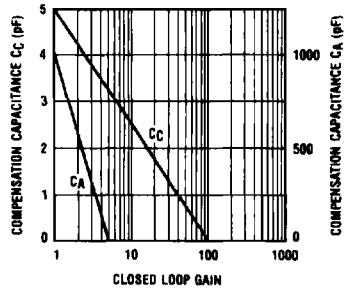

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FIGURE 18. Recommended Value of Compensation Capacitor vs. Closed-Loop Gain for Optimum Slew Rate

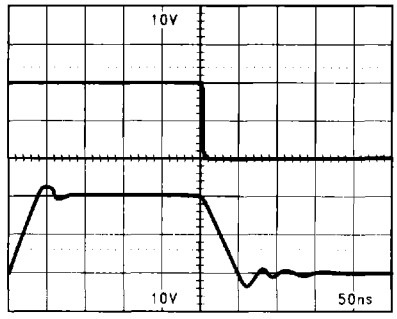

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FIGURE 19. LH0032 Unity Gain Non-Inverting Large Signal Pulse Response: C_C = 5 pF, C_A = 1000 pF

If obtaining minimum ringing at the falling edge is the primary objective, a slight modification to the above is recommended. It is based on the same circuit as that of *Figure 14*.

The values of the unity gain compensation capacitors C_C and C_A should be modified to 5 pF and 1000 pF, respectively. *Figure 18* shows the suitable capacitance to use for various closed-loop gains. The resulting unity gain pulse response waveform is shown in *Figure 19*. The settling time to 1% final value is actually superior to the first method of compensation. However, the LH0032 suffers slow settling thereafter to 0.1% accuracy at the falling edge, and nearly four times as much at the rising edge, compared to the previous scheme. Note, however, that the falling edge ringing is considerably reduced. Furthermore, the slew rate is consistently superior using this compensation because of the smaller value of Miller capacitance C_C required. Typical improvement is as much as 50%. A more detailed discussion of this effect is provided in the Slew Response section of this Application Note.

The second compensation scheme works well with both inverting or non-inverting modes. *Figure 20* shows the circuit schematic, in which a 270Ω resistor and a 0.01 μF capacitor are shunted across the inputs of the device. This lag compensation introduces a zero in the loop modifying the response such that adequate phase margin is preserved at unity gain crossover frequency. Note that the circuit requires no additional compensation.

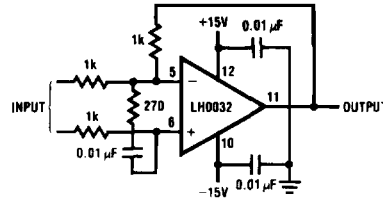

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FIGURE 20. LH0032 Non-Compensated Unity Gain Compensation