National Semiconductor

54LS378/DM74LS378 Parallel D Register with Enable

General Description

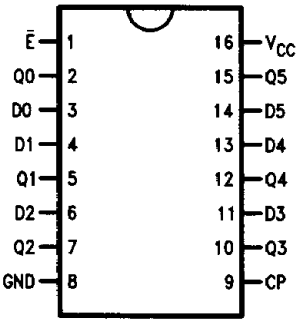
The 'LS378 is a 6-bit register with a buffered common enable. This device is similar to the 'LS174, but with common Enable rather than common Master Reset.

Features

- 6-bit high speed parallel register
- Positive edge-triggered D-type inputs
- Fully buffered common clock and enable inputs
- Input clamp diodes limit high speed termination effects
- Full TTL and CMOS compatible

Connection Diagram

Dual-In-Line Package



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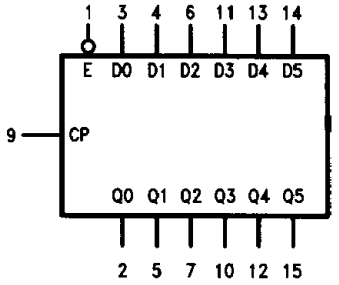
Order Number 54LS378DMQB, 54LS378FMQB, DM74LS378M or DM74LS378N
See NS Package Number J16A, M16A, N16E or W16A

Logic Symbol



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V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
Ē	Enable Input (Active LOW)
D0–D5	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
Q0–Q5	Flip-Flop Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	10V
Operating Free Air Temperature Range	
54LS	−54°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS378			DM74LS378			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s (H)	Setup Time HIGH, D_n to CP	20			20			ns
t_h (H)	Hold Time HIGH, D_n to CP	5.0			5.0			ns
t_s (L)	Setup Time LOW, D_n to CP	20			20			ns
t_h (L)	Hold Time LOW, D_n to CP	5.0			5.0			ns
t_s (H)	Setup Time HIGH, $\overline{E}$ to CP	30			30			ns
t_h (H)	Hold Time HIGH, $\overline{E}$ to CP	5.0			5.0			ns
t_s (L)	Setup Time LOW, $\overline{E}$ to CP	30			30			ns
t_h (L)	Hold Time LOW, $\overline{E}$ to CP	5.0			5.0			ns
t_w (H)	CP Pulse Width HIGH	20			20			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = − 18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.5			V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20.0	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max D_n; $\overline{E}$ = GND, CP = ⌐				22	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	2 kΩ, C_L = 15 pF		Units
		Min	Max	
f_{max}	Maximum Clock Frequency	30		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		27 27	ns

Functional Description

The 'LS378 consists of eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable ($\overline{E}$) inputs are common to all flip-flops.

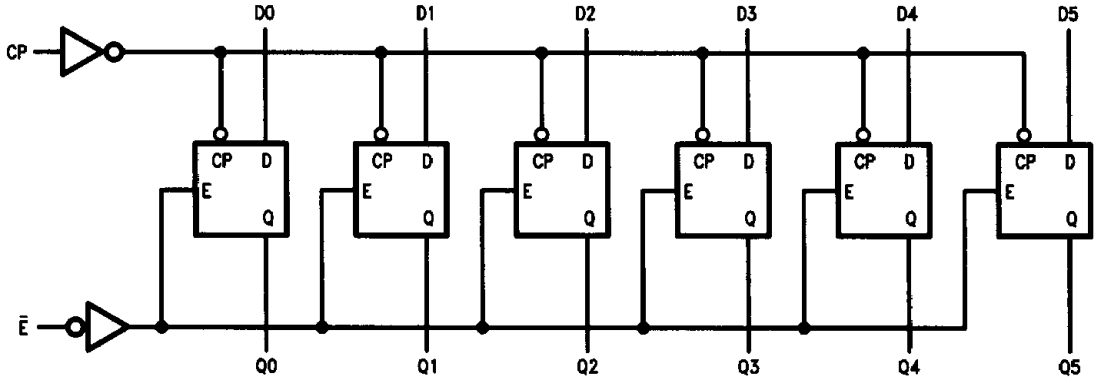
When the $\overline{E}$ input is LOW, new data is entered into the register on the LOW-to-HIGH transition of the CP input. When the $\overline{E}$ input is HIGH the register will retain the present data independent of the CP input.

Truth Table

Inputs			Output
$\overline{E}$	CP	D_n	Q_n
H	⌐	X	No change
L	⌐	H	H
L	⌐	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



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