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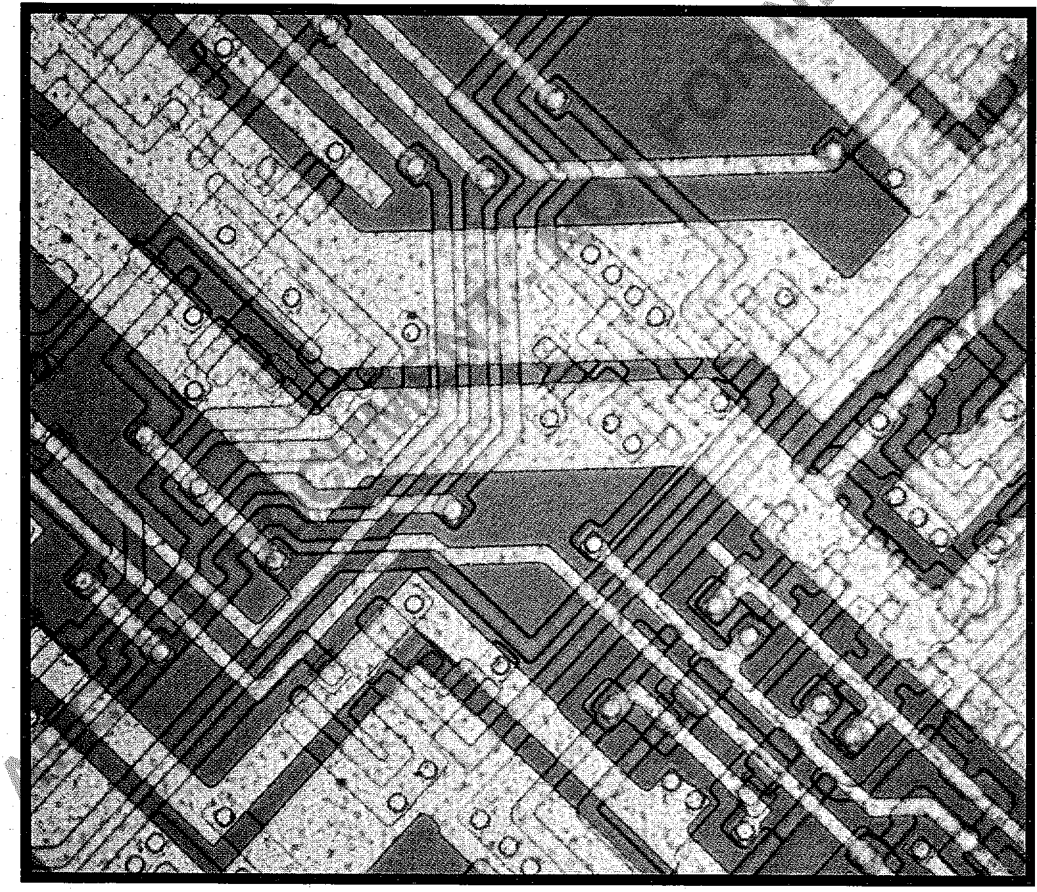
MC68901

Advance Information

Multi-Function Peripheral



This document contains information on a new product. Specifications and information herein are subject to change without notice.

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ADI984R1

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SECTION 1
INTRODUCTION

The MC68901 multi-function peripheral (MFP) is a member of the M68000 Family of peripherals. The MFP directly interfaces with the MC68000 microprocessor via the asynchronous bus structure. Both vectored and polled interrupt schemes are supported with the MFP providing unique vector number generation for each of its 16 interrupt sources. Additionally, handshake lines are provided to facilitate DMAC interfacing. Refer to Figure 1-1 for a block diagram of the MC68901.

The MC68901 performs many of the functions common to most microprocessor-based systems. The resources available to the user include:

- Eight Individually Programmable I/O Pins with Interrupt Capability
- 16-Source Interrupt Controller with Individual Source Enable and Masking
- Four Timers, Two of which are Multi-Mode Timers
- Single-Channel Full-Duplex Universal Synchronous/Asynchronous Receiver-Transmitter (USART) that Supports Asynchronous and with the Addition of a Polynomial Generator Checker that Supports Byte Synchronous Formats

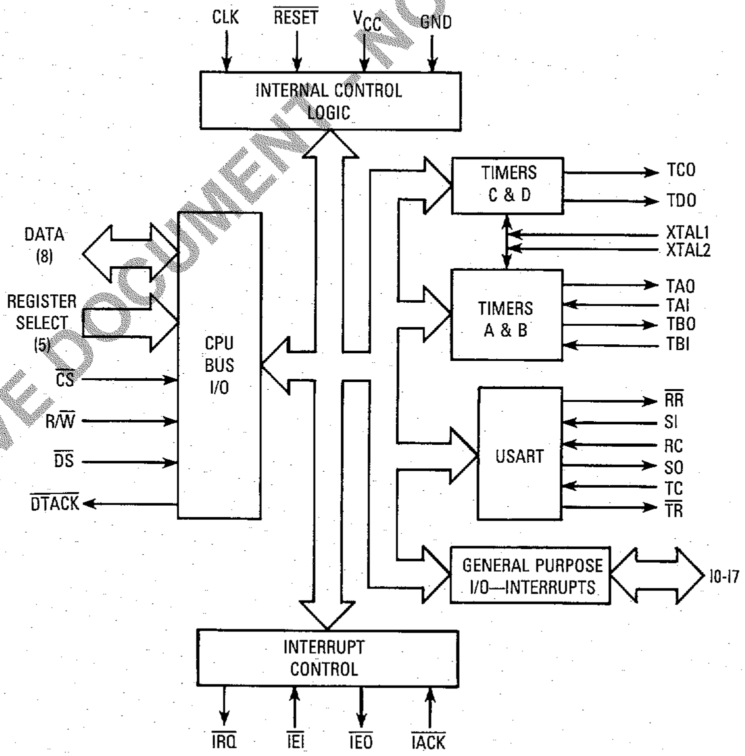


Figure 1-1. MFP Block Diagram

By incorporating multiple functions within the MFP, the system designer retains flexibility while minimizing device count.

From a programmer's point of view, the versatility of the MFP may be attributed to its register set. The registers are well organized and allow the MFP to be easily tailored to a variety of applications. All of the 24 registers are also directly addressable which simplifies programming. The register map is shown in Table 1-1.

Table 1-1. MFP Register Map

Address						Abbreviation	Register Name
Hex	Binary						
	RS5	RS4	RS3	RS2	RS1		
01	0	0	0	0	0	GPDR	General Purpose I/O Data Register
03	0	0	0	0	1	AER	Active Edge Register
05	0	0	0	1	0	DDR	Data Direction Register
07	0	0	0	1	1	IERA	Interrupt Enable Register A
09	0	0	1	0	0	IERB	Interrupt Enable Register B
0B	0	0	1	0	1	IPRA	Interrupt Pending Register A
0D	0	0	1	1	0	IPRB	Interrupt Pending Register B
0F	0	0	1	1	1	ISRA	Interrupt In-Service Register A
11	0	1	0	0	0	ISRB	Interrupt In-Service Register B
13	0	1	0	0	1	IMRA	Interrupt Mask Register A
15	0	1	0	1	0	IMRB	Interrupt Mask Register B
17	0	1	0	1	1	VR	Vector Register
19	0	1	1	0	0	TACR	Timer A Control Register
1B	0	1	1	0	1	TBCR	Timer B Control Register
1D	0	1	1	1	0	TCDCR	Timers C and D Control Register
1F	0	1	1	1	1	TADR	Timer A Data Register
21	1	0	0	0	0	TBDR	Timer B Data Register
23	1	0	0	0	1	TCDR	Timer C Data Register
25	1	0	0	1	0	TDDR	Timer D Data Register
27	1	0	0	1	1	SCR	Synchronous Character Register
29	1	0	1	0	0	UCR	USART Control Register
2B	1	0	1	0	1	RSR	Receiver Status Register
2D	1	0	1	1	0	TSR	Transmitter Status Register
2F	1	0	1	1	1	UDR	USART Data Register

NOTE: Hex addresses assume that RS1 connects with A1, RS2 connects with A2, etc. and that $\overline{DS}$ is connected to $\overline{LDS}$ on the MC68000 or $\overline{DS}$ is connected to $\overline{DS}$ on the MC68008.

SECTION 2
SIGNAL AND BUS OPERATION DESCRIPTION

This section contains a brief description of the input and output signals. A discussion of bus operation during the various operations is also presented.

NOTE

> The terms assertion and negation will be used extensively. This is done to avoid confusion when dealing with a mixture of "active low" and "active high" signals. The term "assert" or "assertion" is used to indicate that a signal is active or true, independent of whether that level is represented by a high or low voltage. The term "negate" or "negation" is used to indicate that a signal is inactive or false.

2.1 SIGNAL DESCRIPTION

The input and output signals can be functionally organized into groups as shown in Figure 2-1. The following paragraphs provide a brief description of the signal and a reference (if applicable) to other sections that contain more detail about its function.

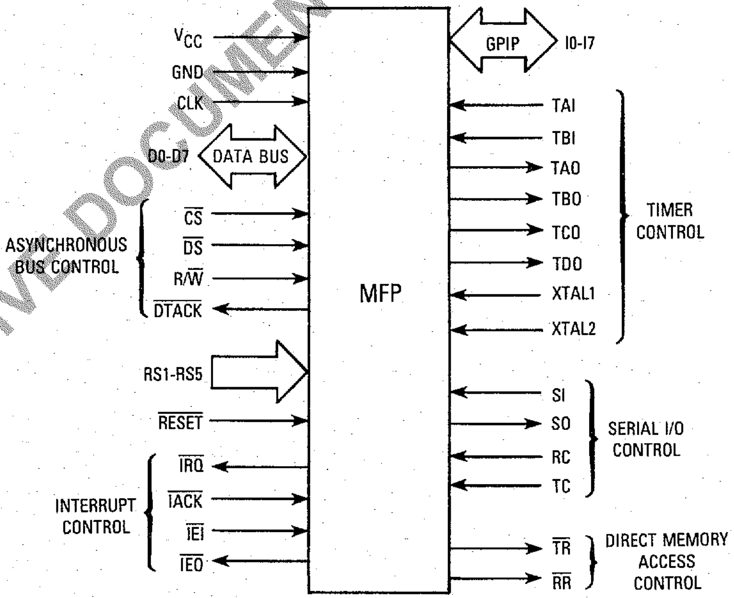


Figure 2-1. Input and Output Signals

2.1.1 V_{CC} and GND

These inputs supply power to the MFP. The V_{CC} is powered at +5 volts, and GND is the ground connection.

2.1.2 Clock (CLK)

The clock input is a single-phase TTL-compatible signal used for internal timing. This input should not be gated off at any time and must conform to minimum and maximum pulse width times. The clock is not necessarily the system clock in frequency or phase.

2.1.3 Data Bus (D0 through D7)

This three-state bidirectional bus is used to transmit data to or receive data from the MFP's internal registers during a processor read or write cycle, respectively. During an interrupt acknowledge cycle, the data bus is used to pass a vector number to the processor. The MFP must be located on data bus lines D0-D7 when used with an MC68000, MC68008, or MC68010 and on data lines D24-D31 when used with an MC68020, if vectored interrupts are to be used.

2.1.4 Asynchronous Bus Control

Asynchronous data transfers are controlled by chip select, data strobe, read/write, and data transfer acknowledge. The register select lines, RS5-RS1, select an internal MFP register for a read or write operation. The reset line initializes the MFP registers and the internal control signals.

2.1.4.1 CHIP SELECT ($\overline{CS}$). This active low input activates the MFP for internal register access. $\overline{CS}$ and $\overline{IACK}$ must not be asserted at the same time.

2.1.4.2 DATA STROBE ($\overline{DS}$). This active low input is part of the internal chip select and interrupt acknowledge functions.

2.1.4.3 READ/WRITE (R/$\overline{W}$). This input defines the current bus cycle as a read (high) or a write (low) cycle.

2.1.4.4 DATA TRANSFER ACKNOWLEDGE ($\overline{DTACK}$). This active low, three-state output signals the completion of the operation phase of a bus cycle to the processor. If the bus cycle is a processor read, the MFP asserts $\overline{DTACK}$ to indicate that the information on the data bus is valid. If the bus cycle is a processor write to the MFP, $\overline{DTACK}$ acknowledges the acceptance of the data by the MFP. $\overline{DTACK}$ will be asserted only by an MFP that has $\overline{CS}$ or $\overline{IACK}$ (and $\overline{IEI}$) asserted.

2.1.5 Register Select Bus (RS1 through RS5)

The register select bus selects an internal MFP register during a read or write operation.

2.1.6 Reset ($\overline{\text{RESET}}$)

This active low input will initialize the MFP during powerup or in response to a total system reset. Refer to **2.2.3 Reset Operation** for further information.

2.1.7 Interrupt Control

The interrupt request and interrupt acknowledge signals are handshake lines for a vectored interrupt scheme. Interrupt enable in and interrupt enable out implement a daisy-chained interrupt structure.

2.1.7.1 INTERRUPT REQUEST ($\overline{\text{IRQ}}$). This active low, open-drain output signals to the processor that an interrupt is pending from the MFP. There are 16 interrupt channels that can generate an interrupt request. Clearing the interrupt pending registers (IPRA and IPRB) or clearing the interrupt mask registers (IMRA and IMRB) will cause the $\overline{\text{IRQ}}$ to be negated. $\overline{\text{IRQ}}$ will also be negated as the result of an interrupt acknowledge cycle, unless additional interrupts are pending in the MFP. Refer to **SECTION 3 INTERRUPT STRUCTURE** for further information.

2.1.7.2 INTERRUPT ACKNOWLEDGE ($\overline{\text{IACK}}$). If both $\overline{\text{IRQ}}$ and $\overline{\text{IEI}}$ are asserted, the MFP will begin an interrupt acknowledge cycle when $\overline{\text{IACK}}$ and $\overline{\text{DS}}$ are asserted. The MFP will supply a unique vector number to the processor which corresponds to the particular channel requesting interrupt service. In a daisy-chained interrupt structure, all devices in the chain must have a common $\overline{\text{IACK}}$. Refer to **2.2.2 Interrupt Acknowledge Operation** and **3.1.2 Interrupt Vector Number Format** for additional information. $\overline{\text{CS}}$ and $\overline{\text{IACK}}$ must not be asserted at the same time.

2.1.7.3 INTERRUPT ENABLE IN ($\overline{\text{IEI}}$). This active low input, together with the $\overline{\text{IEO}}$ signal, provides a daisy-chained interrupt structure for a vectored interrupt scheme. $\overline{\text{IEI}}$ indicates that no higher priority device is requesting interrupt service. So, the highest priority MFP in the chain should have its $\overline{\text{IEI}}$ pin tied low. During an interrupt acknowledge cycle, an MFP with a pending interrupt is not allowed to pass a vector number to the processor until its $\overline{\text{IEI}}$ pin is asserted. When the daisy-chain option is not implemented, all MFPs should have their $\overline{\text{IEI}}$ pin tied low. Refer to **3.2 DAISY-CHAINING MFPs** for additional information.

2.1.7.4 INTERRUPT ENABLE OUT ($\overline{\text{IEO}}$). This active low output, together with the $\overline{\text{IEI}}$ signal, provides a daisy-chained interrupt structure for a vectored interrupt scheme. The $\overline{\text{IEO}}$ of a particular MFP signals lower priority devices that neither it nor any other higher priority device is requesting interrupt service. When a daisy-chain is implemented, $\overline{\text{IEO}}$ is tied to the next lower priority MFP's $\overline{\text{IEI}}$ input. The lowest priority MFP's $\overline{\text{IEO}}$ is not connected. When the daisy-chain option is not implemented, $\overline{\text{IEO}}$ is not connected. Refer to **3.2 DAISY-CHAINING MFPs** for additional information.

2.1.8 General Purpose I/O Interrupt Lines (I0 through I7)

These lines constitute an 8-bit pin-programmable I/O port with interrupt capability. The data direction register (DDR) individually defines each line as either a high-impedance input or a TTL-compatible output. As an input, each line can generate an interrupt on the user selected transition of the input signal. Refer to **SECTION 4 GENERAL PURPOSE INPUT/OUTPUT PORT** for further information.

2.1.9 Timer Control

These lines provide internal timing and auxiliary timer control inputs required for certain operating modes. Additionally, the timer outputs are included in this group.

2.1.9.1 TIMER INPUTS (TAI AND TBI). These inputs are control signals for timers A and B in the pulse width measurement mode and the event count mode. These signals generate interrupts at the same priority level as the general purpose I/O interrupt lines I4 and I3, respectively, when in the pulse width measurement mode. While I4 and I3 do not have interrupt capability when the timers are operated in this mode, they may still be used for I/O. Refer to **5.1.2 Pulse Width Mode Operation** and **5.1.3 Event Count Mode Operation** for further information.

2.1.9.2 TIMER OUTPUTS (TAO, TBO, TCO, AND TDO). Each timer has an associated output which toggles when its main counter counts through 01 (hexadecimal) regardless of which operational mode is selected. When in the delay mode, the timer output will be a square wave with a period equal to two timer cycles. This output may be used to supply the universal synchronous/asynchronous receiver-transmitter (USART) baud rate clocks.

2.1.9.3 TIMER CLOCK (XTAL1 AND XTAL2). This input provides the timing signal for the four timers. A crystal can be connected between the timer clock inputs, XTAL1 and XTAL2, or XTAL1 can be driven with a TTL-level clock while XTAL2 is not connected. The following crystal parameters are suggested:

a) Parallel resonance, fundamental mode AT-cut, HC6 or HC33 holder
b) Frequency tolerance measured with 18 picofarads load (0.1% accuracy) — drive level 10 microwatts
c) Shunt capacitance equals 7 picofarads
d) Series resistance:
    $2.0 < f < 2.7$ MHz; Rs $\leq$ 300 ohms
    $2.8 < f < 4.0$ MHz; Rs $\leq$ 150 ohms

2.1.10 Serial I/O

The full duplex serial channel is implemented by a serial input line. The independent receive and transmit sections may be clocked by separate timing signals on the receive clock input and the transmitter clock input.

2.1.10.1 SERIAL INPUT (SI). This input line is the USART receiver data input. This input is not used in the USART loopback mode. Refer to **6.3.2 Transmitter Status Register** for additional information.

2.1.10.2 SERIAL OUTPUT (SO). This output line is the USART transmitter data output. This output is in a high-impedance state after a device reset.

2.1.10.3 RECEIVER CLOCK (RC). This input controls the serial bit rate of the receiver. The signal may be supplied by the timer output lines or by an external TTL-level clock which meets the minimum and maximum cycle times. This clock is not used in the USART loopback mode. Refer to **6.3.2 Transmitter Status Register** for additional information.

2.1.10.4 TRANSMITTER CLOCK (TC). This input controls the serial bit rate of the transmitter. This signal may be supplied by the timer output lines or by an external TTL-level clock which meets the minimum and maximum cycle times.

2.1.11 Direct Memory Access Control

The USART section of the MFP supports direct memory access transfers through its receiver ready and transmitter ready status lines.

2.1.11.1 RECEIVER READY ($\overline{RR}$). This active low output reflects the receiver buffer full status (bit 7 in the Receiver Status Register) for DMA operations.

2.1.11.2 TRANSMITTER READY ($\overline{TR}$). This active low output reflects the transmitter buffer empty (bit 7 in the Transmitter Status Register) for DMA operations.

2.1.12 Signal Summary

Table 2-1 is a summary of all the signals discussed in the previous paragraphs.

2.2 BUS OPERATION

The following paragraphs explain the control signals and bus operation during data transfer operations and reset.

2.2.1 Data Transfer Operations

Transfer of data between devices involves the following pins:

Register Select Bus — RS1 through RS5
Data Bus — D0 through D7
Control Signals

Table 2-1. Signal Summary

Signal Name	Mnemonic	I/O	Active State
Power Input	V_{CC}	Input	High
Ground	GND	Input	Low
Clock	CLK	Input	N/A
Chip Select	$\overline{\text{CS}}$	Input	Low
Data Strobe	$\overline{\text{DS}}$	Input	Low
Read/Write	R/$\overline{\text{W}}$	Input	Read – High, Write – Low
Data Transfer Acknowledge	$\overline{\text{DTACK}}$	Output	Low
Register Select Bus	RS1–RS5	Input	N/A
Data Bus	D0-D7	I/O	N/A
Reset	$\overline{\text{RESET}}$	Input	Low
Interrupt Request	$\overline{\text{IRQ}}$	Output	Low
Interrupt Acknowledge	$\overline{\text{IACK}}$	Input	Low
Interrupt Enable In	$\overline{\text{IEI}}$	Input	Low
Interrupt Enable Out	$\overline{\text{IEO}}$	Output	Low
General Purpose I/O	I0–I7	I/O	N/A
Timer Clock	XTAL1, XTAL2	Input	N/A
Timer Inputs	TAI, TBI	Input	N/A
Timer Outputs	TAO, TBO, TCO, TDO	Output	N/A
Serial Input	SI	Input	N/A
Serial Output	SO	Output	N/A
Receiver Clock	RC	Input	N/A
Transmitter Clock	TC	Input	N/A
Receiver Ready	$\overline{\text{RR}}$	Output	Low
Transmitter Ready	$\overline{\text{TR}}$	Output	Low

The address and data buses are separate parallel buses used to transfer data using an asynchronous bus structure. In all cases, the bus master assumes responsibility for deskewing all signals it issues at both the start and end of a cycle. Additionally, the bus master is responsible for deskewing the acknowledge and data signals from the peripheral devices.

2.2.1.1 READ CYCLE. To read an MFP register, $\overline{\text{CS}}$ and $\overline{\text{DS}}$ must be asserted, and R/$\overline{\text{W}}$ must be high. The MFP will place the contents of the register which is selected by the register select bus (RS1 through RS5) on the data bus (D0 through D7) and then assert $\overline{\text{DTACK}}$. The register addresses are shown in Table 1-1.

After the processor has latched the data, it negates $\overline{\text{DS}}$. The negation of either $\overline{\text{CS}}$ or $\overline{\text{DS}}$ will terminate the read operation. The MFP will drive $\overline{\text{DTACK}}$ high and place it and the data bus in the high-impedance state. The timing for a read cycle is shown in Figure 2-2. Refer to **7.7 AC ELECTRICAL CHARACTERISTICS** for actual timing numbers.

2.2.1.2 WRITE CYCLE. To write a register, $\overline{\text{CS}}$ and $\overline{\text{DS}}$ must be asserted, and R/$\overline{\text{W}}$ must be low. The MFP will decode the address bus to determine which register is selected. Then the register will be loaded with the contents of the data bus, and $\overline{\text{DTACK}}$ will be asserted. When the processor recognizes $\overline{\text{DTACK}}$, it will negate $\overline{\text{DS}}$. The write cycle is terminated when either $\overline{\text{CS}}$ or $\overline{\text{DS}}$ is negated. The MFP will drive $\overline{\text{DTACK}}$ high and place it in the high-impedance state. The timing for a write cycle is shown in Figure 2-3. Refer to **7.7 AC ELECTRICAL CHARACTERISTICS** for actual numbers.

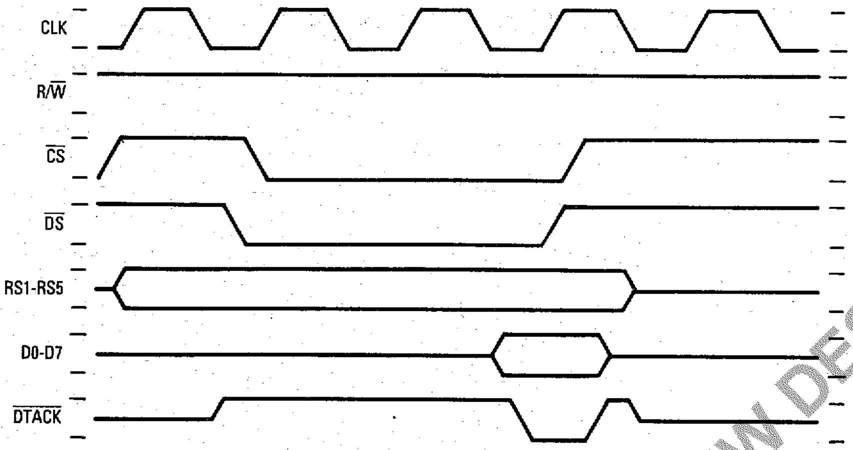


Figure 2-2. Read Cycle Timing

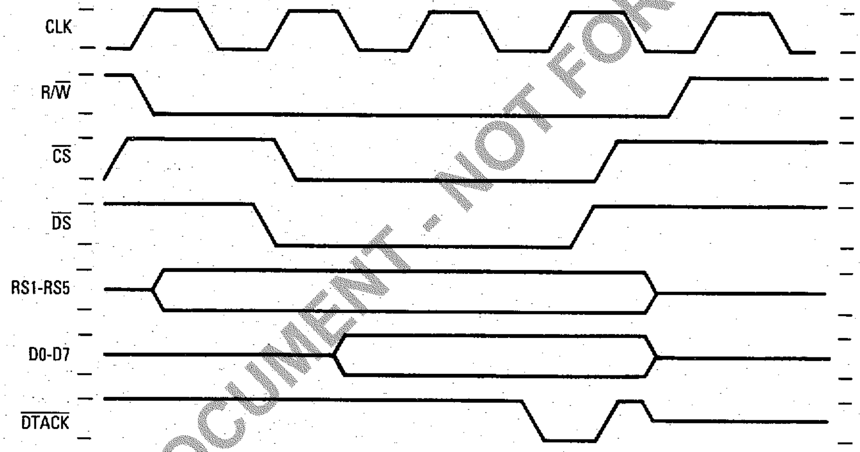


Figure 2-3. Write Cycle Timing

2.2.2 Interrupt Acknowledge Operation

The MFP has 16 interrupt sources: eight internal and eight external. When an interrupt request is pending, the MFP will assert $\overline{IRQ}$. In a vectored interrupt scheme, the processor will acknowledge the interrupt request by performing an interrupt acknowledge cycle. $\overline{IACK}$ and $\overline{DS}$ will be asserted. The MFP responds to the $\overline{IACK}$ signal by placing a vector number on the data bus. This vector number corresponds to the particular interrupt channel requesting service. The format of this vector number is given in Figure 3-1.

When the MFP asserts $\overline{DTACK}$ to indicate that valid data is on the bus, the processor will latch the data and terminate the bus cycle by negating $\overline{DS}$. When either $\overline{DS}$ or $\overline{IACK}$ is negated, the MFP will terminate the interrupt acknowledge operation by driving $\overline{DTACK}$ high and placing it in the high-impedance state. $\overline{IRQ}$ will be negated as a result of the $\overline{IACK}$ cycle unless additional interrupts are pending.

The MFP can be part of a daisy-chain interrupt structure which allows multiple MFPs to be placed at the same interrupt level by sharing a common $\overline{\text{IACK}}$ signal. A daisy-chain priority scheme is implemented with signals $\overline{\text{IEI}}$ and $\overline{\text{IEO}}$. $\overline{\text{IEI}}$ indicates that no higher priority device is requesting interrupt service. $\overline{\text{IEO}}$ signals lower priority devices that neither this device nor any higher priority MFP is requesting service. To daisy-chain MFPs, the highest priority MFP has its $\overline{\text{IEI}}$ tied low and successive MFPs have their $\overline{\text{IEI}}$ connected to the next higher priority MFP's $\overline{\text{IEO}}$. Note that when the daisy-chain interrupt structure is not implemented, the $\overline{\text{IEI}}$s of all MFPs must be tied low and the $\overline{\text{IEO}}$s left unconnected. Refer to **3.2 DAISY-CHAINING MFPs** for additional information.

When the processor initiates an interrupt acknowledge cycle by driving $\overline{\text{IACK}}$ and $\overline{\text{DS}}$, the MFP, whose $\overline{\text{IEI}}$ is low, may respond with a vector number if an interrupt is pending. If this device does not have a pending interrupt, $\overline{\text{IEO}}$ is asserted which allows the next lower priority device to respond to the interrupt acknowledge. When an MFP propagates $\overline{\text{IEO}}$, it will not drive the data bus nor $\overline{\text{DTACK}}$ during the interrupt acknowledge cycle. The timing for an $\overline{\text{IACK}}$ cycle is shown in Figure 2-4. Refer to **7.7 AC ELECTRICAL CHARACTERISTICS** and Figures 7-7 and 7-8 for further information.

2.2.3 Reset Operation

The reset operation will initiate the MFP to a known state. The reset operation requires that the $\overline{\text{RESET}}$ input be asserted for a minimum of two microseconds. During a device reset condition, all internal MFP registers are cleared except for the timer data registers (TADR, TBDR, TCDR, and TDDR), the USART data register (UDR), and the transmitter status register (TSR). All timers are stopped, the USART receiver and transmitter are disabled, and the serial output (SO) line is placed in high impedance. The interrupt channels are also disabled and any pending interrupts are cleared. In addition, the general purpose interrupt I/O lines are placed in the high-impedance input mode, and the timer outputs are driven low. External MFP signals are negated. Since the vector register (VR) is initialized to a $00, an uninitialized MFP may not respond to an interrupt acknowledge cycle with the uninitialized interrupt vector, $0F. See **3.1.2 Interrupt Vector Number Format** for more information.

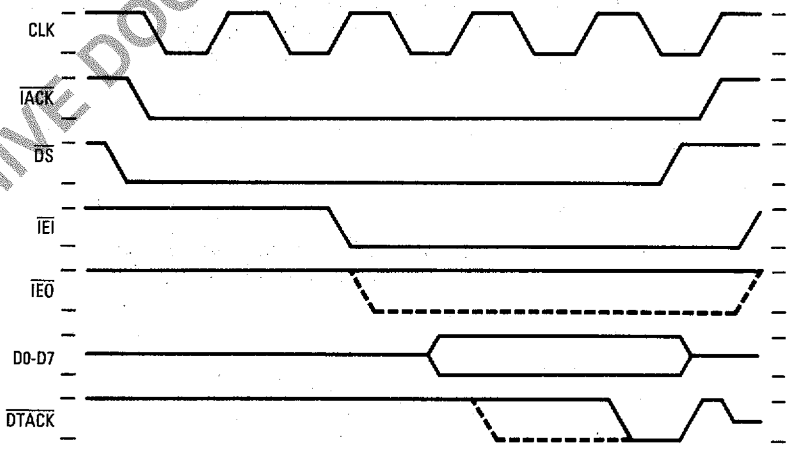


Figure 2-4. $\overline{\text{IACK}}$ Cycle Timing

SECTION 3
INTERRUPT STRUCTURE

In an M68000 system, the MFP will be assigned to one of the seven possible interrupt levels. All interrupt service requests from the MFP's 16 interrupt channels will be presented at this level. As an interrupt controller, the MFP will internally prioritize its 16 interrupt sources. Additional interrupt sources may be placed at the same interrupt level by daisy-chaining multiple MFPs. The MFPs will be prioritized by their position in the chain.

3.1 INTERRUPT PROCESSING

Each MFP provides individual interrupt capability for its various functions. When an interrupt is received on one of the external interrupt channels or from one of the eight internal sources, the MFP will request interrupt service. The 16 interrupt channels are assigned a fixed priority so that multiple pending interrupts are serviced according to their relative importance. Since the MFP can internally generate 16 vector numbers, the unique vector number which corresponds to the highest priority channel that has a pending interrupt is presented to the processor during an interrupt acknowledge cycle. This unique vector number allows the processor to immediately begin execution of the interrupt handler for the interrupting source, decreasing interrupt latency.

3.1.1 Interrupt Channel Prioritization

The 16 interrupt channels are prioritized from highest to lowest, with General Purpose Interrupt 7 (I7) being the highest and I0 the lowest. The priority of the interrupt is determined by the least-significant four bits in the interrupt vector number which are internally generated by the MC68901. Pending interrupts are presented to the processor in order of priority unless they have been masked. By selectively masking interrupts, the channels are in effect re-prioritized.

3.1.2 Interrupt Vector Number

During an interrupt acknowledge cycle, a unique 8-bit interrupt vector number is presented to the system which corresponds to the specific interrupt source that is requesting service.

7	6	5	4	3	2	1	0
V7	V6	V5	V4	IV3	IV2	IV1	IV0

V7-V4 — Copied from the vector register.

IV3-IV0 — Determine highest priority channel requesting interrupt.

IV3	IV2	IV1	IV0	Description
1	1	1	1	General Purpose Interrupt 7 (I7)
1	1	1	0	General Purpose Interrupt 6 (I6)
1	1	0	1	Timer A
1	1	0	0	Receiver Buffer Full
1	0	1	1	Receive Error
1	0	1	0	Transmit Buffer Empty
1	0	0	1	Transmit Error
1	0	0	0	Timer B
0	1	1	1	General Purpose Interrupt 5 (I5)
0	1	1	0	General Purpose Interrupt 4 (I4)
0	1	0	1	Timer C
0	1	0	0	Timer D
0	0	1	1	General Purpose Interrupt 3 (I3)
0	0	1	0	General Purpose Interrupt 2 (I2)
0	0	0	1	General Purpose Interrupt 1 (I1)
0	0	0	0	General Purpose Interrupt 0 (I0)

3.1.3 Vector Register (VR)

This 8-bit register determines the four most-significant bits in the interrupt vector format and which end-of-interrupt mode is used in a vectored interrupt scheme. The vector register should be written to before writing to the interrupt mask or enable registers to ensure that the MC68901 responds to an interrupt acknowledge cycle with a vector number not in the range of allowable user vectors. For information refer to **3.4.1 Selecting the End-Of-Interrupt Mode.**

	7	6	5	4	3	2	1	0	
$17	V7	V6	V5	V4	S	*	*	*	VR
Reset:	0	0	0	0	0	U	U	U	

V7-V4 — Written by user to set the most-significant four bits of the interrupt vector number.
S — In-Service Register Enable
1 = Software end-of-interrupt mode and in-service register bits enabled.
0 = Automatic end-of-interrupt mode and in-service register bits forced low.
2–0 — Not Used

3.2 DAISY-CHAINING MFPs

As an interrupt controller, the MC68901 MFP will support eight external interrupt sources in addition to its eight internal interrupt sources. When a system requires more than eight external interrupt sources to be placed at the same interrupt level, sources may be added to the prioritized structure by daisy-chaining MFPs. Interrupt sources are prioritized internally within each MFP, and the MFPs are prioritized by their position in the chain. Unique vector numbers are provided for each interrupt source.

The IEI and IEO signals implement the daisy-chained structure. The IEI of the highest priority MFP is tied low and the IEO output of this device is tied to the next highest priority MFP's IEI. The IEI and IEO signals are daisy-chained in this manner for all the MFPs in the chain with the lowest priority MFP's IEO left unconnected. Figure 3-1 shows a diagram of the interrupt daisy-chain. Daisy-chaining requires that all parts in the chain have a common IACK. When the common IACK is asserted during an interrupt acknowledge cycle, all parts will prioritize interrupts in parallel. When the IEI signal to an MFP is asserted, the part may respond to the IACK cycle if it requires interrupt service. Otherwise, the part will assert IEO to the next lower priority device. Thus, priority is passed down the chain via IEI and IEO until a part which has a pending interrupt is reached. The part with the pending interrupt passes a vector number to the processor and does not propagate IEO.

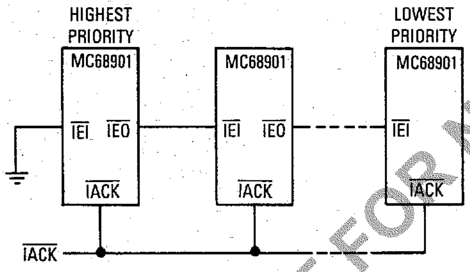


Figure 3-1. Daisy-Chained Interrupt Structure

3.3 INTERRUPT CONTROL REGISTERS

MFP interrupt processing is managed by the enable registers A and B, interrupt pending registers A and B, and interrupt mask registers A and B. These registers allow the programmer to enable or disable individual interrupt channels, mask individual interrupt channels, and access pending interrupt status information. In-service registers A and B allow interrupts to be nested as described in **3.4 NESTING MFP INTERRUPTS**. The interrupt control registers are shown in the following paragraphs.

3.3.1 Interrupt Enable Registers (IREA, IERB)

The interrupt channels are individually enabled or disabled by writing a one or a zero, respectively, to the appropriate bit of interrupt enable register A or B (IERA or IERB). The processor may read these registers at any time.

When a channel is enabled, interrupts received on the channel will be recognized by the MFP, and IRQ will be asserted to the processor indicating that interrupt service is required. On the other hand, a disabled channel is completely inactive; interrupts received on the channel are ignored by the MFP.

Writing a zero to a bit of interrupt enable register A or B will cause the corresponding bit of the interrupt pending register to be cleared. This will terminate all interrupt service requests for the channel and also negate IRQ unless interrupts are pending from other sources. Disabling a channel, however, does not affect the corresponding bit in interrupt in-service registers A or B. So, if the MFP is in the software end-of-interrupt mode (see **3.4.3 Software End-Of-Interrupt**) and an interrupt is in service when a channel is disabled, the in-service bit of that channel will remain set until cleared by software.

	7	6	5	4	3	2	1	0	
$07	GPIP7	GPIP6	Timer A	RCV Buffer Full	RCV Error	XMIT Buffer Empty	XMIT Error	Timer B	IERA
	7	6	5	4	3	2	1	0	
$09	GPIP5	GPIP4	Timer C	Timer D	GPIP3	GPIP2	GPIP1	GPIP0	IERB
Reset:	0	0	0	0	0	0	0	0	

3.3.2 Interrupt Pending Registers (IPRA, IPRB)

When an interrupt is received on an enabled channel, the corresponding interrupt pending bit is set in interrupt pending register A or B (IPRA or IPRB). In a vectored interrupt scheme, this bit will be cleared when the processor acknowledges the interrupting channel and the MFP responds with a vector number. In a polled interrupt system, the interrupt pending registers must be read to determine the interrupting channel, and then the interrupt pending bit is cleared by the interrupt handling routine without performing an interrupt acknowledge sequence.

	7	6	5	4	3	2	1	0	
$0B	GPIP7	GPIP6	Timer A	RCV Buffer Full	RCV Error	XMIT Buffer Empty	XMIT Error	Timer B	IPRA
	7	6	5	4	3	2	1	0	
$0D	GPIP5	GPIP4	Timer C	Timer D	GPIP3	GPIP2	GPIP1	GPIP0	IPRB
Reset:	0	0	0	0	0	0	0	0	

3.3.3 Interrupt Mask Registers (IMRA, IMRB)

Interrupts are masked for a channel by clearing the appropriate bit in interrupt mask register A or B (IMRA or IMRB). Even though an enabled channel is masked, the channel will recognize subsequent interrupts and set its interrupt pending bit. However, the channel is prevented from requesting interrupt service ($\overline{IRQ}$ to the processor) as long as the mask bit for that channel is cleared. If a channel is requesting interrupt service at the time that its corresponding bit in IMRA or IMRB is cleared, the request will cease, and $\overline{IRQ}$ will be negated unless another channel is requesting interrupt service. Later, when the mask bit is set, any pending interrupt on the channel will be processed according to the channel's assigned priority. IMRA and IMRB may be read at any time. Figure 3-2 shows a conceptual circuit of an MC68901 interrupt channel.

	7	6	5	4	3	2	1	0	
$13	GPIP7	GPIP6	Timer A	RCV Buffer Full	RCV Error	XMIT Buffer Empty	XMIT Error	Timer B	IMRA
	7	6	5	4	3	2	1	0	
$15	GPIP5	GPIP4	Timer C	Timer D	GPIP3	GPIP2	GPIP1	GPIP0	IMRB
Reset:	0	0	0	0	0	0	0	0	

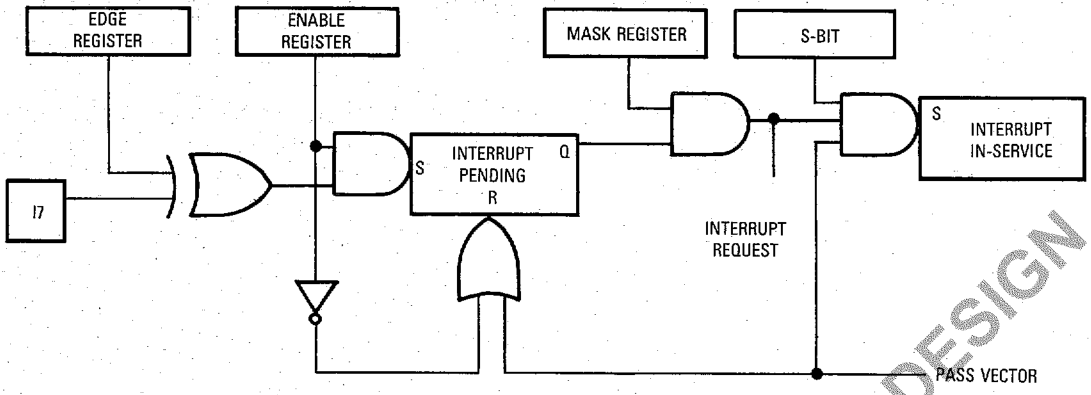


Figure 3-2. Conceptual Circuits of an Interrupt Channel

3.3.4 Interrupt In-Service Registers (ISRA, ISRB)

These registers indicate whether interrupt processing is in progress for a certain channel. A bit is set whenever an interrupt vector number is passed for a interrupt channel during an IACK cycle and the S bit of the vector register is a one. The bit is cleared whenever interrupt service is complete for an associated interrupt channel, the S bit of the vector register is cleared, or the processor writes a zero to the bit.

	7	6	5	4	3	2	1	0	
$0F	GPIP7	GPIP6	Timer A	RCV Buffer Full	RCV Error	XMIT Buffer Empty	XMIT Error	Timer B	ISRA

	7	6	5	4	3	2	1	0	
$11	GPIP5	GPIP4	Timer C	Timer D	GPIP3	GPIP2	GPIP1	GPIP0	ISRB
Reset:	0	0	0	0	0	0	0	0	

3.4 NESTING MFP INTERRUPTS

In an M68000 vectored interrupt system, the MFP is assigned to one of seven possible interrupt levels. When an interrupt is received from the MFP, an interrupt acknowledge for that level is initiated. Once an interrupt is recognized at a particular level, interrupts at the same level or below are masked by the processor. As long as the processor's interrupt mask is unchanged, the M68000 interrupt structure will prohibit nesting the interrupts at the same interrupt level. However, additional interrupt requests from the MFP can be recognized before a previous channel's interrupt service routine is finished by lowering the processor's interrupt mask to the next lower interrupt level within the interrupt handler.

When nesting MFP interrupts, it may be desirable to permit interrupts on any MFP channel regardless of its priority, to preempt or delay interrupt processing of an earlier channel's interrupt service request. Or, it may be desirable to only allow subsequent higher priority channel interrupt requests to supercede previously recognized lower priority interrupt requests. The MFP interrupt structure provides the flexibility by offering two end-of-interrupt options for vectored interrupt schemes. Note that the end-of-interrupt modes are not active in a polled interrupt scheme.

3.4.1 Selecting The End-Of-Interrupt Mode

In a vectored interrupt scheme, the MFP may be programmed to operate in either the automatic end-of-interrupt mode or the software end-of-interrupt mode. The mode is selected by writing the S bit of the vector register. When the S bit is programmed to a one, the MFP is placed in the software end-of-interrupt mode, and when the S bit is a zero, all channels operate in the automatic end-of-interrupt mode.

3.4.2 Automatic End-Of-Interrupt Mode

When an interrupt vector is passed to the processor during an interrupt acknowledge cycle, the corresponding channel's interrupt pending bit is cleared. In the automatic end-of-interrupt mode, no further history of the interrupt remains in the MFP. The in-service bits of the interrupt in-service registers (ISRA and ISRB) are forced low. Subsequent interrupts, which are received on any MFP channel will generate an interrupt request to the processor even if the current interrupt's service routine has not been completed.

3.4.3 Software End-Of-Interrupt Mode

In the software end-of-interrupt mode, the channel's associated interrupt pending bit is cleared. In addition, the channel's in-service bit of in-service register A or B is set when its vector number is passed to the processor during the interrupt acknowledge cycle. A higher priority channel may subsequently request interrupt service and be acknowledged, but as long as the channel's in-service bit is set, no lower priority channel may request interrupt service nor pass its vector during an interrupt acknowledge sequence.

While only higher priority channels may request interrupt service, any channel can receive an interrupt and set its interrupt pending bit. Even the channel with its in-service bit is set can receive a second interrupt. However, no interrupt service request is made until its in-service bit is cleared.

The in-service bit for a particular channel can be cleared by writing a zero to its corresponding bit in ISRA or ISRB and ones to all other bit positions. Since bits in the in-service registers can only be cleared in software and not set, writing ones to the registers does not alter their contents. ISRA and ISRB may be read at any time.

SECTION 4
GENERAL PURPOSE INPUT/OUTPUT PORT

The general purpose input/output (I/O) port (GPIP) provides eight I/O lines (I0 through I7) that may be operated as either inputs or outputs under software control. In addition, these lines may optionally generate an interrupt on either a positive transition or a negative transition of the input signal. The flexibility of the GPIP allows it to be configured as an 8-bit I/O port or for bit I/O. Since interrupts are enabled on a bit-by-bit basis, a subset of the GPIP could be programmed as handshake lines or the port could be connected to as many as eight external interrupt sources, which would be prioritized by the MFP interrupt controller for the interrupt service.

4.1 M6800 INTERRUPT CONTROLLER

The MFP interrupt controller is particularly useful in a system which has many M6800-type devices. Typically, in a vectored M68000 system, M6800 peripherals use the autovector which corresponds to their assigned interrupt level since they can not provide a vector number in response to an interrupt acknowledge cycle. The autovector interrupt handler must then poll all M6800 devices at that interrupt level to determine which device is requesting service. However, by tying the $\overline{\text{IRQ}}$ output from an M6800 peripheral to the general purpose I/O port (GPIP) of an MFP, a unique vector number will be provided to the processor during an interrupt acknowledge cycle. This interrupt structure will significantly reduce interrupt latency for M6800 devices and other peripherals which do not support vectored interrupts.

4.2 GPIP CONTROL REGISTERS

The GPIP is programmed via three control registers. These registers control the data direction, provide user access to the port, and specify the active edge for each bit of the GPIP which will produce an interrupt. These registers are described in detail in the following paragraphs.

4.2.1 General Purpose I/O Data Register (GPDR)

The general purpose I/O data register is used to input data from or output data to the port. When data is written to the GPDR, those pins which are defined as inputs will remain in the high-impedance state. Pins which are defined as outputs will assume the state (high or low) of their corresponding bit in the data register. When the GPDR is read, data will be passed directly from the bits of the data register for pins which are defined as outputs. Data from pins defined as inputs will come from the input buffers.

	7	6	5	4	3	2	1	0	
$01	GPIP7	GPIP6	GPIP5	GPIP4	GPIP3	GPIP2	GPIP1	GPIP0	GPDR
Reset:	0	0	0	0	0	0	0	0	

4.2.2 Active Edge Register (AER)

The active edge register (AER) allows each of the GPIP lines to produce an interrupt on either a one-to-zero or a zero-to-one transition. Writing a zero to the appropriate edge bit of the active edge register will cause the associated input to generate an interrupt on the one-to-zero transition. Writing a one to the edge bit will produce an interrupt on the zero-to-one transition of the corresponding line. When the processor sets a bit, interrupts will be generated on the rising edge of the associated input signal. When the processor clears a bit, interrupts will be generated on the falling edge of the associated input signal.

	7	6	5	4	3	2	1	0	
$03	GPIP7	GPIP6	GPIP5	GPIP4	GPIP3	GPIP2	GPIP1	GPIP0	AER
Reset:	0	0	0	0	0	0	0	0	

NOTE

The inputs to the exclusive-OR of the transition detector are the edge bit and the input buffer. As a result, writing the AER may cause an interrupt-producing transition, depending upon the state of the input. So, the AER should be configured before enabling interrupts via the interrupt enable registers (IERA and IERB). Also, changing the edge bit while interrupts are enabled may cause an interrupt on the corresponding channel.

4.2.3 Data Direction Register (DDR)

The data direction register (DDR) allows the programmer to define I0 through I7 as inputs or outputs by writing the corresponding bit. When a bit of the data direction register is written as a zero, the corresponding interrupt I/O pin will be a high-impedance input. Writing a one to any bit of the data direction register will cause the corresponding pin to be configured as a push-pull output.

	7	6	5	4	3	2	1	0	
$05	GPIP7	GPIP6	GPIP5	GPIP4	GPIP3	GPIP2	GPIP1	GPIP0	DDR
Reset:	0	0	0	0	0	0	0	0	

SECTION 5
TIMERS

The MFP contains four 8-bit timers which provide many functions typically required in microprocessor systems. The timers can supply the baud rate clocks for the on-chip serial I/O channel, generate periodic interrupts, measure elapsed time, and count signal transitions. In addition, two timers have waveform generation capability.

All timers are prescaler/counter timers with a common independent clock input (XTAL1 and XTAL2) and are not required to be operated from the system clock. Each timer's output signal toggles when the timer's main counter times out. Additionally, timers A and B have auxiliary control signals which are used in two of the operation modes. An interrupt channel is assigned to each timer, and when the auxiliary control signals are used in the pulse width measurement mode, a separate interrupt channel will respond to transitions on these inputs.

5.1 OPERATION MODES

Timers A and B are full function timers which, in addition to the delay mode, operate in the pulse width measurements mode and the event count mode. Timers C and D are delay timers only. A brief discussion of each of the timer modes follows.

5.1.1 Delay Mode Operation

All timers may operate in the delay mode. In this mode, the prescaler is always active. The prescaler specifies the number of timer clock cycles which must elapse before a count pulse is applied to the main counter. A count pulse causes the main counter to decrement by one. When the timer has decremented down to 01 (hexadecimal), the next count pulse will cause the main counter to be reloaded from the timer data register and a time out pulse will be produced. This time out pulse is coupled to the timer's interrupt channel and, if the channel is enabled, an interrupt will occur. The time out pulse also causes the timer output pin to toggle. The output will remain in this new state until the next time out pulse occurs.

For example, if delay mode with a divide-by-10 prescaler is selected and the timer data register is loaded with 100 (decimal), the main counter will decrement once every 10 timer clock cycles. After 1000 timer clocks, a time out pulse will be produced. This time out pulse will generate an interrupt if the channel is enabled (IERA, IERB), and in addition, the timer's output line will toggle. The output line will complete one full period every 2000 cycles of the timer clock.

If the prescaler value is changed while the timer is enabled, the first time out pulse will occur at an indeterminate time no less than one nor more than 200 timer clock cycles. Subsequent time out pulses will then occur at the correct interval.

If the main counter is loaded with 01 (hexadecimal), a time out pulse will occur every time the prescaler presents a count pulse to the main counter. If the main counter is loaded with 00, a time out pulse will occur every 256 count pulses.

5.1.2 Pulse Width Measurement Operation

Besides the delay mode, timers A and B may be programmed to operate in the pulse width measurement mode. In this mode, an auxiliary control input is required; timers A and B auxiliary input lines are TAI and TBI. Also, in the pulse width measurement mode, interrupt channels normally associated with I4 and I3 will instead respond to transitions on TAI and TBI, respectively. General purpose lines I3 and I4 may still be used for I/O, but may not be used as interrupt generating inputs. A conceptual circuit of the selection of the interrupt source is shown in Figure 5-1.

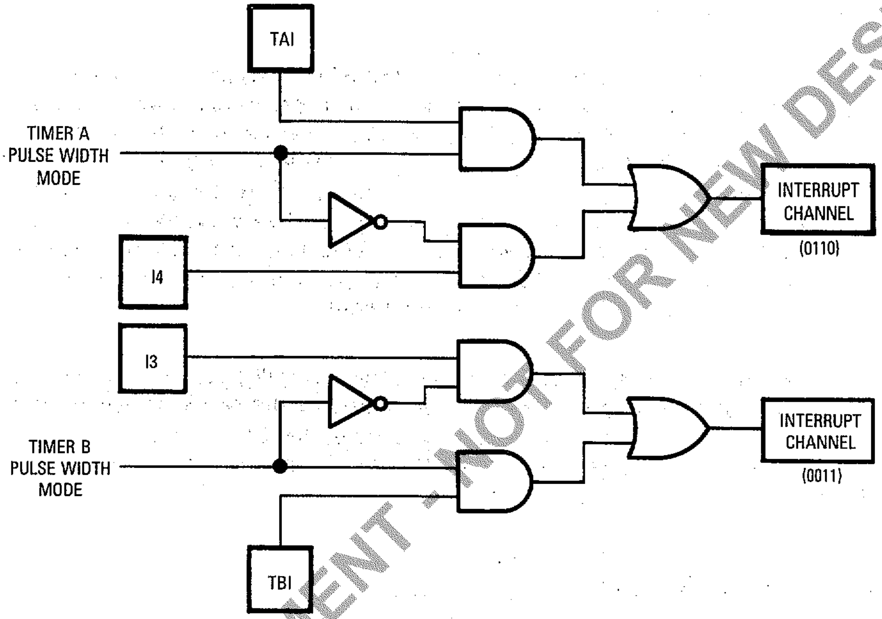


Figure 5-1. Conceptual Circuit of Interrupt Source Selection

The pulse width measurement mode functions similarly to the delay mode, with the auxiliary control signal acting as an enable to the timer. When the control signal is active, the prescaler and main counter are allowed to operate. When the control signal is negated, the timer is stopped. So, the width of the active pulse on TAI or TBI is measured by the number of timer counts which occur while the timer is allowed to operate.

The active state of the auxiliary input line is defined by the associated interrupt channel's edge bit in the active edge register (AER). GPIP4 of the AER is the edge bit associated with TAI, and GPIP3 is associated with TBI. When the edge bit is a one, the auxiliary input will be active high, enabling the timer while the input signal is at a high level. If the edge bit is zero, the auxiliary input will be active low and the timer will operate while the input signal is at a low level.

The state of the active edge bit also specifies whether a zero-to-one transition or a one-to-zero transition of the auxiliary input pin will produce an interrupt when the interrupt channel is enabled. In normal operation, programming the active edge bit to a one will produce an interrupt on the zero-to-one transition of the associated input signal. Alternately, programming the edge bit to a zero will produce an interrupt on the one-to-zero transition of the input signal. However, in the pulse width measurement mode, the interrupt generated by a transition on TAI or TBI will occur on the opposite transition as that normally defined by the edge bit.

For example, in the pulse width measurement mode, if the edge bit is a one, the timer will be allowed to run while the auxiliary input is high. When the input transitions from high to low, the timer will stop and, if the interrupt channel is enabled, an interrupt will occur. By having the interrupt occur on the one-to-zero transition instead of the zero-to-one transition, the processor will be interrupted when the pulse being measured has been terminated and the width of the pulse from the timer is available.

After reading the contents of the timer, the processor must reinitialize the main counter by writing to the timer data register to allow consecutive pulses to be measured. If the data register is written after the auxiliary input signal becomes active, the timer will count from the previous contents of the timer data register until it counts through 01 (hexadecimal). At that time, the main counter is loaded with the new value from the timer data register, a time out pulse is generated which will toggle the timer output, and an interrupt may be optionally generated on the timer interrupt channel. Note that the pulse width measured includes counts from before the main counter was reloaded. If the timer data register is written while the pulse is transitioning to the active state, an indeterminate value may be written into the main counter .

Once the timer is reprogrammed for another mode, interrupts will again occur as normally defined by the edge bit. Note that an interrupt may be generated as the result of placing the timer into the pulse width measurement mode or by reprogramming the timer for another mode. Also, an interrupt may be generated by changing the state of the edge bit while in the pulse width measurement mode.

5.1.3 Event Count Mode Operation

In addition to the delay mode and the pulse width measurement mode, timers A and B may be programmed to operate in the event count mode. Like the pulse width measurement mode, the event count mode requires an auxiliary input signal, TAI or TBI. General purpose lines I3 and I4 can be used for I/O or as interrupt producing inputs.

In the event count mode, the prescaler is disabled allowing each active transition on TAI and TBI to produce a count pulse. The count pulse causes the main counter to decrement by one. When the timer counts through 01 (hexadecimal), a time out pulse is generated which will cause the output signal to toggle and may optionally produce an interrupt via the associated timer interrupt channel. The timer's main counter is also reloaded from the timer data register. To count transitions reliably, the input signal may only transition once every four timer clock periods. For this reason, the input signal must have a maximum frequency of one-fourth that of the timer clock.

The active edge of the auxiliary input signal is defined by the associated channel's edge bit. GPIP4 of the AER specifies the active edge for TAI, and GPIP3 defines the active edge for TBI. When the edge bit is programmed to a one, a count pulse will be generated on the zero-to-one transition of the auxiliary input signal. When the edge bit is programmed to a zero, a count pulse will be generated on the one-to-zero transition. Also, note that changing the state of the edge bit while the timer is in the event count mode may produce a count pulse.

5.2 TIMER REGISTERS

The four timers are programmed via three control registers and four data registers. The following paragraphs describe the different registers.

5.2.1 Timer Data Registers (TxDR)

The four timer data registers (TDRs) are designed as Timer A data register (TADR), Timer B (TBDR), Timer C (TCDR), and Timer D (TDDR). Each timer's main counter is an 8-bit binary down counter. The timer data registers contain the value of their respective main counter. This value was captured on the last low-to-high transition of the data strobe pin.

The main counter is initialized by writing to the TDR. If the timer is stopped, data is loaded simultaneously into both the TDR and main counter. If the TDR is written to while the timer is enabled, the value is not loaded into the timer until the timer counts through 01 (hexadecimal). If a write is performed while the timer is counting through 01, then an indeterminate value will be loaded into the timer's main counter.

Typical Timer Data Register

	7	6	5	4	3	2	1	0	
$1F, $21, $23, $25	D7	D6	D5	D4	D3	D2	D1	D0	TADR, TBDR, TCDR, TDDR

5.2.2 Timer Control Registers (TxCR)

Timer control register A (TACR) and timer control register B (TBCR) are associated with timers A and B, respectivey. Timers C and D are programmed using one control register—the timer C and D control register (TCDCR). The bits in the control register select the operation mode, prescaler value, and disable the timers. Both control registers have bits which allow the programmer to reset output lines TA0 and TB0.

	7	6	5	4	3	2	1	0	
$19	*	*	*	Reset TA0	AC3	AC2	AC1	AC0	TACR

	7	6	5	4	3	2	1	0	
$1B	*	*	*	Reset TB0	BC3	BC2	BC1	BC0	TBCR
Reset:	0	0	0	0	0	0	0	0	

*Unused bits read as zero.

Reset TA0/TB0 — Reset Timer A and B Output Lines.
TA0 and TB0 may be forced low at any time by writing a one to the reset location in TACR and TBCR. Output is held low during the write operation, and at the end of the bus cycle the output is allowed to toggle in response to a time-out pulse. When resetting TA0 and TB0, the other bits in the TCR must be written with their previous value to avoid altering the operating mode.

AC3-AC0, BC3-BC0 — Select Timer A and B Operation Mode.
When the timer is stopped, counting is inhibited. The contents of the timer's main counter is not affected, although any residual count in the prescaler.

AC3 BC3	AC2 BC2	AC1 BC1	AC0 BC0	Operation Mode
0	0	0	0	Timer Stopped
0	0	0	1	Delay Mode, /4 Prescaler
0	0	1	0	Delay Mode, /10 Prescaler
0	0	1	1	Delay Mode, /16 Prescaler
0	1	0	0	Delay Mode, /50 Prescaler
0	1	0	1	Delay Mode, /64 Prescaler
0	1	1	0	Delay Mode, /100 Prescaler
0	1	1	1	Delay Mode, /200 Prescaler
1	0	0	0	Event Count Mode
1	0	0	1	Pulse Width Mode, /4 Prescaler
1	0	1	0	Pulse Width Mode, /10 Prescaler
1	0	1	1	Pulse Width Mode, /16 Prescaler
1	1	0	0	Pulse Width Mode, /50 Prescaler
1	1	0	1	Pulse Width Mode, /64 Prescaler
1	1	1	0	Pulse Width Mode, /100 Prescaler
1	1	1	1	Pulse Width Mode, /200 Prescaler

	7	6	5	4	3	2	1	0	
$1D	*	CC2	CC1	CC0	*	DC2	DC1	DC0	TCDCR
Reset:	0	0	0	0	0	0	0	0	

*Unused bits read as zero.

CC2-CC0, DC3-DC0 — Select Timer C and D Operation Mode.

When the timer is stopped, counting is inhibited. The contents of the timer's main counter is not affected, although any residual count in the prescaler is lost.

CC2 DC2	CC1 DC1	CC0 DC0	Operation Mode
0	0	0	Timer Stopped
0	0	1	Delay Mode, /4 Prescaler
0	1	0	Delay Mode, /10 Prescaler
0	1	1	Delay Mode, /16 Prescaler
1	0	0	Delay Mode, /50 Prescaler
1	0	1	Delay Mode, /64 Prescaler
1	1	0	Delay Mode, /100 Prescaler
1	1	1	Delay Mode, /200 Prescaler

SECTION 6
UNIVERSAL SYNCHRONOUS/ASYNCHRONOUS RECEIVER-TRANSMITTER

The universal synchronous asynchronous receiver-transmitter (USART) is a single, full-duplex serial channel with a double-buffered receiver and transmitter. There are separate receive and transmit clocks and, also, separate receive and transmit status and data bytes. The receive and transmit sections are also assigned separate interrupt channels. Each section has two interrupt channels: one for normal conditions and the other for error conditions. All interrupt channels are edge-triggered. Generally, it is the output of a flag bit or bits which is coupled to the interrupt channel. Thus, if an interrupt-producing event occurs while the associated interrupt channel is disabled, no interrupt would be produced, even if the channel was subsequently enabled because a transition did not occur while the channel was enabled. That particular event would have to occur again, generating another edge, before an interrupt would be generated. The interrupt channels may be disabled and instead, a DMA device can be used to transfer the data via the control signals receiver ready ($\overline{RR}$) and transmitter ready ($\overline{TR}$). See **6.4 DMA OPERATION** for more information.

6.1 CHARACTER PROTOCOLS

The MFP USART supports asynchronous and, with the help of a polynomial generator checker, byte synchronous character formats. These formats are selected independently of the divide-by-one and divide-by-18 clock modes. It is possible to clock data synchronously into the MC68901 but still use start and stop bits. After a start bit is detected, data will be shifted in and a stop bit will be checked to determine proper framing. In this mode, all normal asynchronous format features apply.

When the divide-by-one clock mode is selected, synchronization must be accomplished externally. The receiver will sample serial data on the rising edge of the receiver clock. In the divide-by-18 clock mode, the data is sampled at mid-bit time to increase transient noise rejection.

Also, when the divide-by-18 clock mode is selected, the USART resynchronization logic is enabled. This logic increases the channels clock skew tolerance. Refer to **6.1.1 Asynchronous Format** for more information on the resynchronization logic.

6.1.1 Asynchronous Format

Variable character length and start/stop bit configurations are available under software control for asynchronous operation. The user can choose a character length from five to eight bits and a stop bit length of one, one and one-half, or two bits. The user can also select odd, even, or no parity.

In the asynchronous format, start bit detection is always enabled. New data is not shifted into the receive shift register until a zero bit is received. When the divide-by-18 clock mode is selected, the false start bit logic is also active. Any transition must be stable for three positive receive clock edges to be considered valid. For a start bit to be good, a valid zero-to-one transition must not occur for eight positive receiver clock transitions after the initial one-to-zero transition. After a valid start bit has been detected, the data is checked continuously for valid transitions. When a valid transition is detected, an internal counter is forced to state zero, and no further transition checking is initiated until state four. At state eight, the "previous state" of the transition checking logic is clocked into the receiver. As a result of this resynchronization logic, it is possible to run with asynchronous clocks without start and stop bits if there are sufficient valid transitions in the data streams.

6.1.2 Synchronous Format

When the synchronous character format is selected, the 8-bit synchronous character loaded into the synchronous character register (SCR) is compared to received serial data until a match is found. Once synchronization is established, incoming data is clocked into the receiver. The synchronous word will be continuously transmitted during an underrun condition. All synchronous characters can be optionally stripped from the receive buffer (i.e. taken out of the data stream and thrown away) by clearing the appropriate bit in the receive status register (RSR).

	7	6	5	4	3	2	1	0	
$27	D7	D6	D5	D4	D3	D2	D1	D0	SCR
Reset:	0	0	0	0	0	0	0	0	

The synchronous character should be written after the character length is selected, since unused bits in the synchronous character register are zeroed out. When parity is enabled, synchronous word length is the character length plus one. The MFP will compute and append the parity bit for the synchronous character when a character length of eight is selected. However, if the character length is less than eight, the user must determine the synchronous word parity and write it into the synchronous character register along with the synchronous character. The parity bit must be the most-significant bit. The MFP will then transmit the extra bit in the synchronous word as a parity bit.

6.1.3 USART Control Register (UCR)

This register selects the clock mode and the character format for the receive and transmit sections.

	7	6	5	4	3	2	1	0	
$29	CLK	CL1	CL0	ST1	ST0	PE	E/O	*	UCR
Reset:	0	0	0	0	0	0	0	U	

*Unused bits read as zero.

CLK — Clock Mode

1 = Data clocked into and out of receiver and transmitter at one sixteenth the frequency of their respective clocks.

0 = Data clocked into and out of receiver and transmitter at the frequency of their respective clocks.

CL1,CL0 — Character Length

These bits specify the length of the character exclusive of start bits, and parity.

CL1	CL0	Character Length
0	0	8 Bits
0	1	7 Bits
1	0	6 Bits
1	1	5 Bits

ST0-ST1 — Start/Stop Bit and Format Control

These bits select the number of start and stop bits and specify the character format.

ST1	ST0	Start Bits	Stop Bits	Format
0	0	0	0	Synchronous
0	1	1	1	Asynchronous
1	0	1	1-1/2	Asynchronous*
1	1	1	2	Asynchronous

*Used with Divide-by-16 mode only.

PE — Parity Enable

Parity is not automatically appended to the synchronous character for character lengths of less than eight bits. Therefore, parity should be written into the SCR along with the synchronous character.

1 = Parity checked by receiver and parity calculated and inserted during data transmission.
0 = No parity check and no parity bit computed for transmission.

E/O — Even/Odd Parity

1 = Even parity is selected.
0 = Odd parity is selected.

Bit 0 — Not used

6.2 RECEIVER

As data is received on the serial input line (SI), it is clocked into an internal 8-bit shift register until the specified number of data bits have been assembled. The character will then be transferred to the receive buffer, assuming that the last word in the receive buffer has been read. This transfer will set the buffer full bit in the Receiver Status Register (RSR) and produce a buffer full interrupt to the processor, assuming this interrupt has been enabled.

Reading the receive buffer satisfies the buffer full condition and allows a new data word to be transferred to the receive buffer when it is assembled. The receive buffer is accessed by reading the USART data register (UDR). The UDR is simply an 8-bit data register used when transferring data between the MFP and the CPU.

Each time a word is transferred to the receive buffer, its status information is latched into the receiver status register (RSR). The RSR is not updated again until the data word in the receive buffer has been read. When a buffer full condition exists, the RSR should always be read before the receive buffer (UDR) to maintain the correct correspondence between data and flags. Otherwise, it is possible that after reading the UDR and prior to reading the RSR, a new word could be received and transferred to the receive buffer. Its associated flags would be latched into the RSR, writing over the flags for the previous data word. Thus, when the RSR was read to access the status information for the first data word, the flags for the new word would be retrieved.

6.2.1 Receiver Interrupt Channels

The USART receiver section is assigned two interrupt channels. One indicates the buffer full condition while the other channel indicates an error condition. Error conditions include overrun, parity error, frame error, synchronous found, and break. These interrupting conditions correspond to the OE, PE, FE, and F/S or B bits of the receiver status register. These flags will function as described in **6.2.2 Receiver Status Register** whether the receiver interrupt channels are enabled or disabled.

While only one interrupt is generated per character received, two dedicated interrupt channels allow separate vector numbers to be assigned for normal and abnormal receiver conditions. When a received word has an error associated with it and the error interrupt channel is enabled, an interrupt will be generated on the error channel only. However, if the error channel is disabled, an interrupt for an error condition will be generated on the buffer full interrupt channel along with interrupts produced by the buffer full condition. The receiver status register must always be read to determine which error condition produced the interrupt.

6.2.2 Receiver Status Register (RSR)

The RSR contains the receiver buffer full flag, the synchronous strip enable, the various status information associated with the data word in the receive buffer. The RSR is latched each time a data word is transferred to the receive buffer. RSR flags cannot change again until the new data word has been read. However, the M/CIP bit is allowed to change.

	7	6	5	4	3	2	1	0	
$2B	BF	OE	PE	FE	F/S or B	M/CIP	SS	RE	RSR
Reset:	0	0	0	0	0	0	0	0	

BF — Buffer Full

Receiver word is transferred to the receive buffer.
Receiver buffer is read by accessing the USART data register.

OE — Overrun Error

Overrun error occurs when a received word is to be transferred to the receive buffer, but the buffer is full. Neither the receiver buffer nor the RSR is overwritten.

1 = Receiver buffer full.
0 = Read by RSR or MFP reset.

PE — Parity Error

1 = Parity error detected on character transfer to receiver buffer.
0 = No parity error detected on character transfer to receiver buffer.

FE — Frame Error

A frame error exists when a non-zero data character is not followed by a stop bit in the asynchronous character format.

1 = Frame error detected on character transfer to receiver buffer.
0 = No frame error detected on character transfer to receiver buffer.

F/S or B — Found/Search or Break Detect

The F/S bit is used in the synchronous character format. When set to zero, the USART receiver is placed in the search mode. F/S is cleared when the incoming character does not match the synchronous character.

1 = Match found. Character length counter enabled.
0 = Incoming data compared to SCR. Character length counter disabled.

The B bit is used in the asynchronous character format. This flag indicates a break condition which continues until a non-zero data bit is received.

1 = Character transferred to the receive buffer is a break condition.
0 = Non-zero data bit received and break condition was acknowledged by reading the RSR at least once.

M or CIP — Match/Character in Progress

The M bit is used in the synchronous character format and indicates a synchronous character has been received.

1 = Character transferred to the receive buffer matches the synchronous character.
0 = Character transferred to the receive buffer does not match the synchronous character.

The CIP bit is used in the asynchronous character format and indicates that a character is being assembled.

1 = Start bit is detected.
0 = Final stop bit has been received.

SS — Synchronous Strip Enable

1 = Characters that match the synchronous character will not be loaded into the receiver buffer and no buffer full condition will be produced.
0 = Characters that match the synchronous character will be transferred to the receive buffer and a buffer full condition will be produced.

RE — Receiver Enable

This bit should not be set until the receiver clock is active. When the transmitter is disabled in auto-turnaround mode this bit is set.

1 = Receiver operation is enabled.
0 = Receiver is disabled.

6.2.3 Special Receive Conditions

Certain receive conditions relating to the overrun error flag and the break detect flag require further explanation. Consider the following examples:

1) A break is received while the receive buffer is full. This does not produce an overrun condition. Only the B flag will be set after the receiver buffer is read.
2) A new word is received, and the receive buffer is full. A break is received before the receive buffer is read.

Both the B and OE flags will be set when the buffer full condition is satisfied.

6.3 TRANSMITTER

The transmit buffer is loaded by writing to the USART data register (UDR). The data character will be transferred to an internal 8-bit shift register when the last character in the shift register has been transmitted. This transfer will produce a buffer empty condition. If the transmitter completes the transmission of the character in the shift register before a new character is written to the transmit buffer, an underrun error will occur. In the asynchronous character format, the transmitter will send a mark until the transmit buffer is written. In the synchronous character format, the transmitter will continuously send the synchronous character until the transmit buffer is written.

The transmit buffer can be loaded prior to enabling the transmitter. After the transmitter is enabled, there is a delay before the first bit is output. The serial output line (SO) should be programmed to be high, low, or high impedance (by setting the appropriate bits in the Transmitter Status Register (TSR)) before the transmitter is enabled forcing the output line to the desired state until the first bit of the first character is shifted out. The state of the H and L bits in the TSR determine the state of the first transmitted bit after the transmitter is enabled. If the high impedance mode is selected prior to the transmitter being enabled, the first bit transmitted is indeterminate. Note that the SO line will always be driven high for one bit time prior to the character in the transmit shift register being transmitted when the transmitter is first enabled.

When the transmitter is disabled, any character currently being transmitted will continue to completion. However, any character in the transmit buffer will not be transmitted and will remain in the buffer. Thus, no buffer empty condition will occur. If the buffer is empty when the transmitter is disabled, the buffer empty condition will remain, but no underrun condition will be generated when the character in transmission is completed. If no character is being transmitted when the transmitter is disabled, the transmitter will stop at the next rising edge of the internal shift clock.

In the asynchronous character format, the transmitter can be programmed to send a break. The break will be transmitted once the word currently in the shift register has been sent. If the shift register is empty, the break command will be effective immediately. A transmit error interrupt will be generated at every normal character boundary to aid in timing the break transmission. The contents of the TSR are not affected, however. The break will continue until the break bit is cleared. The underrun error (UE) must be cleared from the TSR. Also, the interrupt pending register must be cleared of pending transmitter errors at the beginning of the break transmission, or no interrupts will be generated at the character boundary time. The break (B) bit cannot be set until the transmitter has been enabled and has had sufficient time (one transmitter clock cycle) to perform internal reset and initialization functions.

Any character in the transmit buffer at the start of a break will be transmitted when the break is terminated, assuming the transmitter is still enabled. If the transmit buffer is empty at the start of a break, it may be written at any time during the break. If the buffer is still empty at the end of the break, an underrun condition will exist.

Disabling the transmitter during a break condition causes the transmitter to cease transmission of the break character at the end of the current character. No end-of-break stop bit will be transmitted. Even if the transmit buffer is empty, no buffer empty condition will occur nor will an underrun condition occur. Also, any word in the transmit buffer will remain.

6.3.1 Transmitter Interrupt Channels

The USART transmit section is assigned two interrupt channels. The normal channel indicates a buffer empty condition, and the error channel indicates an underrun or end condition. These interrupting conditions correspond to the BE, UE, and END flags in the TSR. The flag bits will function as described in **6.3.2 Transmitter Status Register** whether their associated interrupt channel is enabled or disabled.

6.3.2 Transmitter Status Register

The TSR contains various transmitter error flags and transmitter control bits for selecting auto-turnaround and loopback mode.

	7	6	5	4	3	2	1	0	
$2D	BE	UE	AT	END	B	H	L	TE	TSR
Reset:	0	0	0	0	0	0	0	0	

BE — Buffer Empty
1 = Character in the transmit buffer transferred to TSR.
0 = Transmit buffer reloaded by writing to the USR.

U — Underrun Error
One full transmitter clock cycle is required after UE bit is set before it can be cleared. This bit does not require clearing before writing to the UDR.
1 = Character in the TSR was transmitted before a new word was loaded into the transmit buffer.
0 = Transmitter disabled or read performed on TSR.

AT — Auto-Turnaround
When set, the receiver will be enabled automatically after the transmitter has been disabled and the last character being transmitted is complete.

END — End of Transmission
If the transmitter is disabled while a character is being transmitted, this bit is set after transmission is complete. If no character was being transmitted, then this bit is set immediately. Reenabling the transmitter clears this bit.

B — Break
This bit only functions in the asynchronous format. When B is set, BE cannot be set. A break consists of all zeros with no stop bit. This bit cannot be set until transmitter is enabled and internal reset and initialization is complete.
1 = Break transmitted and transmission stops.
0 = Break ceases and normal transmission resumes.

H, L — High and Low
These bits configure the transmitter output (SO) when the transmitter is disabled. Changing these bits after the transmitter is enabled will alter the output state until END is cleared.

H	L	Output State
0	0	High Impedance
0	1	Low
1	0	High
1	1	Loopback Mode

TE — Transmitter Enable
The serial output will be driven according to H and L bits until transmission begins. A one bit is transmitted before character transmission in the TSR begins.
1 = Transmitter enabled.
0 = Transmitter disabled. UE bit cleared and END bit set.

6.4 DMA OPERATION

USART error conditions are valid only for each character boundary. When the USART performs block data transfers by using the DMA handshake lines receiver ready ($\overline{RR}$) and transmitter ready ($\overline{TR}$), errors must be saved and checked at the end of a block. This is accomplished by enabling the error channel for the receiver or transmitter and by masking interrupts for this channel. Once the transfer is complete, interrupt pending register A is read. Any pending receiver or transmitter error indicates an error in the data transfer.

$\overline{RR}$ is asserted when the buffer full bit is set in the RSR unless a parity error or frame error is detected by the receiver. $\overline{TR}$ is asserted when the buffer empty bit is set in the TSR unless a break is currently being transmitted.

SECTION 7
ELECTRICAL CHARACTERISTICS

This section contains the electrical specifications and associated timing information for the MC68901 multi-function peripheral.

7.1 MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to 7.0	V
Input Voltage	V_{in}	−0.3 to 7.0	V
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	−65 to 150	°C
Power Dissipation	P_D	1.5	W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{CC} or GND).

7.2 THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Symbole	Value	Rating
Thermal Resistance	θ_{JA}		θ_{JC}		°C/W
Ceramic		40		15*	
Plastic		40		20*	

*Estimated

7.3 POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA} \qquad (1)$$

where:

T_A = Ambient Temperature, °C
θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W
P_D = $P_{INT} + P_{I/O}$
P_{INT} = $I_{CC} \times V_{CC}$, Watts — Chip Internal Power
$P_{I/O}$ = Power Dissipation on Input and Output Pins, Watts — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An appropriate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \qquad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \cdot (T_A + 273°C) + \theta_{JA} \cdot P_D^2 \qquad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case) surface (θ_{JC}) and from the case to the outside ambient (θ_{CA}). These terms are related by the equation:

$$\theta_{JA}=\theta_{JC}+\theta_{CA}$$

θ_{JC} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals θ_{JC}. Substitution of θ_{JC} for θ_{JA} in equation (1) will result in a lower semiconductor junction temperature.

Values for thermal resistance presented in this document, unless estimated, were derived using the procedure described in Motorola Reliability Report 7843, "Thermal Resistance Measurement Method for MC68XX Microcomponent Devices," and are provided for design purposes only. Thermal measurements are complex and dependent on procedure and setup. User derived values for thermal resistance may differ.

7.4 DC ELECTRICAL CHARACTERISTICS ($T_A=0°C$ to $70°C$, $V_{CC}=-5\ V\pm5\%$, unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	2.0	$V_{CC}+0.3$	V
Input Low Voltage	V_{IL}	−0.3	0.8	V
Output High Voltage, Except $\overline{\text{DTACK}}$ ($I_{OH}=-120\ \mu A$)	V_{OH}	2.4	—	V
Output Low Voltage, Except $\overline{\text{DTACK}}$ ($I_{OL}=2.0\ mA$)	V_{OL}	—	0.5	V
Power Supply Current (Outputs Open)	I_{LL}	—	180	mA
Input Leakage Current ($V_{in}=0$ to V_{CC})	I_{LI}	—	10	µA
Hi-Z Output Leakage Current in Float ($V_{out}=2.4$ to V_{CC})	I_{LOH}	—	10	µA
Hi-Z Output Leakage Current in Float ($V_{out}=0.5\ V$)	I_{LOL}	—	−10	µA
$\overline{\text{DTACK}}$ Output Source Current ($V_{out}=2.4\ V$)	I_{OH}	—	−400	µA
$\overline{\text{DTACK}}$ Output Sink Current ($V_{out}=0.5\ V$)	I_{OL}	—	5.3	mA

7.5 CAPACITANCE ($T_A=25°C$, f=1 MHz, unmeasured pins returned to ground)

Characteristic	Symbol	Min	Max	Unit
Input Capacitance	C_{in}	—	10	pF
Hi-Z Output Capacitance	C_{out}	—	10	pF
Load Capacitance $\overline{\text{IRQ}}$, $\overline{\text{DTACK}}$ All Other Outputs	C	— —	100 130	pF

7.6 CLOCK TIMING (see Figure 7-1)

Characteristic	Symbol	Min	Max	Unit
Frequency of Operation	f	1.0	4.0	MHz
Cycle Time	t_{cyc}	250	1000	ns
Clock Pulse Width	t_{CL}, t_{CH}	110	250	ns
Rise and Fall Times	t_{Cr}, t_{Cf}	—	15	ns

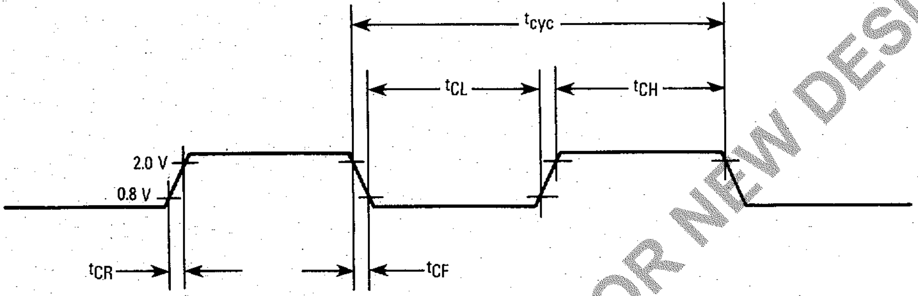
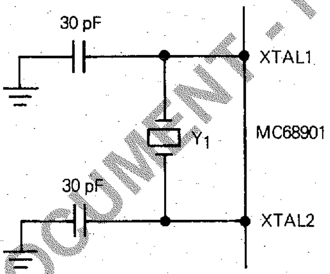


Figure 7-1. Clock Input Timing Diagram



Crystal Parameters
Parallel resonance fundame
$R_S \leq 150\ \Omega$ (f = 2.8 – 4.0 MHz
$R_S \leq 300\ \Omega$ (f = 2.0 – 2.7 MHz
$C_L = 18$ pF, $C_M = 0.02$ pF, C
f (typical) = 2.4576 MHz

Figure 7-2. MFP External Oscillator Components

7.7 AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0 Vdc ± 5%, GND = 0°C to 70°C unless otherwise noted; see Figures 7-3 through 7-12.

Num	Characteristic	Min	Max	Unit
1[4]	$\overline{\text{CS}}$, $\overline{\text{DS}}$ Width High	50	—	ns
2	R/$\overline{\text{W}}$, RS1-RS5 Valid to Falling $\overline{\text{CS}}$ Setup Time	0	—	ns
3	Data Valid Prior to Falling CLK Setup Time (Write Cycle Only)	0	—	ns
4[1]	$\overline{\text{CS}}$, $\overline{\text{IACK}}$ Valid to Falling CLK Setup Time	50	—	ns
5	CLK Low to $\overline{\text{DTACK}}$ Low	—	220	ns
6	$\overline{\text{CS}}$ or $\overline{\text{DS}}$ or $\overline{\text{IACK}}$ High to $\overline{\text{DTACK}}$ High	—	60	ns
7	$\overline{\text{CS}}$ or $\overline{\text{DS}}$ or $\overline{\text{IACK}}$ High to $\overline{\text{DTACK}}$ High Impedance	—	100	ns
8	$\overline{\text{DTACK}}$ Low to Data Invalid Hold Time (Write)	0	—	ns
9	$\overline{\text{CS}}$ or $\overline{\text{DS}}$ or $\overline{\text{IACK}}$ High to Data High Impedance (Read)	—	50	ns
10	$\overline{\text{CS}}$ or $\overline{\text{DS}}$ High to RS1-RS5, R/$\overline{\text{W}}$ Invalid Hold Time	0	—	ns
11[5]	Data Valid from $\overline{\text{CS}}$ Low (Read)	—	310	ns
12	Data Valid to $\overline{\text{DTACK}}$ Low Setup Time (Read)	50	—	ns
13	$\overline{\text{DTACK}}$ Low to $\overline{\text{DS}}$ or $\overline{\text{CS}}$ or $\overline{\text{IACK}}$ High Hold Time	0	—	ns
14	$\overline{\text{IEI}}$ Low to Falling CLK Setup Time	50	—	ns
15	$\overline{\text{IEO}}$ Valid from CLK Low Delay Time	—	180	ns
16	Data Valid from CLK Low Delay Time	—	300	ns
17	$\overline{\text{IEO}}$ Invalid from $\overline{\text{IACK}}$ High Delay Time	—	150	ns
18	$\overline{\text{DTACK}}$ Low from CLK High Delay Time	—	180	ns
19	$\overline{\text{IEO}}$ Valid from $\overline{\text{IEI}}$ Low Delay Time	—	100	ns
20	Data Valid from $\overline{\text{IEI}}$ Low Delay Time	—	220	ns
21	CLK Cycle Time	250	1000	ns
22	CLK Width Low	110	—	ns
23	CLK Width High	110	—	ns
24[2,4]	$\overline{\text{CS}}$, $\overline{\text{IACK}}$ Inactive to Rising CLK Setup Time	100	—	ns
25	I/O Minimum Active Pulse Width	100	—	ns
26[3]	$\overline{\text{IACK}}$ Width High	2	—	t_{cyc}
27	I/O Data Valid from Rising $\overline{\text{CS}}$ or $\overline{\text{DS}}$ (Write)	—	450	ns
28	Receiver Ready ($\overline{\text{RR}}$) Delay from Rising RC	—	600	ns
29	Transmitter Ready ($\overline{\text{TR}}$) Delay from Rising TC	—	600	ns
30	TxO (A or B) Low from Rising Edge of $\overline{\text{CS}}$ or $\overline{\text{DS}}$ (Reset Time)	—	450	ns
31[3]	Timer Output (TxO) Valid from Falling t_{clk} that Causes Timeout	—	2 t_{clk} +300	ns
32	Timer Clock (t_{clk}) Low Time	110	—	ns
33	Timer Clock (t_{clk}) High Time	110	—	ns
34	Timer Clock (t_{clk}) Cycle Time	250	1000	ns
35	$\overline{\text{RESET}}$ Low Time	2	—	µs
36	Delay to Falling $\overline{\text{IRQ}}$ from Ix Active Transition	—	380	ns
37	Transmitter Interrupt Delay from Falling Edge of TC	550	—	ns
38	Receiver Interrupt Delay from Rising Edge of RC (Buffer Full)	800	—	ns
39	Receiver Interrupt Delay from Falling Edge of RC (Error)	800	—	ns

7.7 AC ELECTRICAL CHARACTERISTICS (Continued)

Num	Characteristic	Min	Max	Unit
40	SI Setup Time from Rising Edge of RC (Divide by 1 Only)	80	—	ns
41	SI Hold Time from Rising Edge of RC (Divide by 1 Only)	350	—	ns
42	SO Data Valid from Falling Edge of TC (Divide by 1 Only)	—	440	ns
43	TC Low Time	500	—	ns
44	TC High Time	500	—	ns
45	TC Cycle Time	1.05	∞	µs
46	RC Low Time	500	—	ns
47	RC High Time	500	—	ns
48	RC Cycle Time	1.05	∞	µs
49[3]	$\overline{CS}$, $\overline{IACK}$, $\overline{DS}$ Width Low	—	80	t_{cyc}
50	SO Data Valid from Falling Edge of TC (Divide by 16 Only)	—	490	ns

NOTES:

1. If the setup time is not met, $\overline{CS}$ will not be recognized until the next falling clock.
2. If this setup time is met (for consecutive cycles), the minimum hold-off time of one clock cycle will be obtained. If not met, the hold-off time will be two clock cycles.
3. t_{cyc} refers to the clock signal applied to the MFP CLK input pin. t_{clk} refers to the timer clock signal, regardless of whether that signal comes from the XTAL1/XTAL2 crystal clock inputs or the TAI or TBI timer inputs
4. $\overline{CS}$ is latched internally, therefore if specifications 1 and 24 are met, then $\overline{CS}$ may be negated before the falling clock and still initiate a bus cycle.
5. Although $\overline{CS}$ and $\overline{DTACK}$ are synchronized with the clock, the data out during a read cycle is asynchronous to the clock, relying only on $\overline{CS}$ for timing.

Timing diagrams (Figures 7-3 through 7-12) are located on foldout pages 1 through 3 at the end of this document.

7.8 TIMER AC CHARACTERISTICS

Definitions:

Error = Indicated time value — actual time value

$t_{psc} = t_{CLK} \times$ Prescale Value

Internal Timer Mode:

Single Interval Error (Free Running) (See Note 2)	$\pm$ 100 ns
Cumulative Internal Error	0
Error Between Two Timer Reads	$\pm (t_{psc} - 4\ t_{CLK})$
Start Timer to Stop Timer Error	$2\ t_{CLK} + 100$ ns to $-(t_{psc} + 6\ t_{CLK} + 100$ ns$)$
Start Timer to Read Timer Error	0 to $-(t_{psc} + 6\ t_{CLK} + 400$ ns$)$
Start Timer to Interrupt Request Error (See Note 3)	$-2\ t_{CLK}$ to $-(4\ t_{CLK} + 800$ ns$)$

Pulse Width Measurement Mode:

Measurement Accuracy (See Note 1)	$2\ t_{CLK}$ to $-(t_{psc} + 4\ t_{CLK})$
Minimum Pulse Width	$4\ t_{CLK}$

Event Counter Mode:

Minimum Active Time of TAI and TBI	$4\ t_{CLK}$
Minimum Inactive Time of AI and TBI	$4\ t_{CLK}$

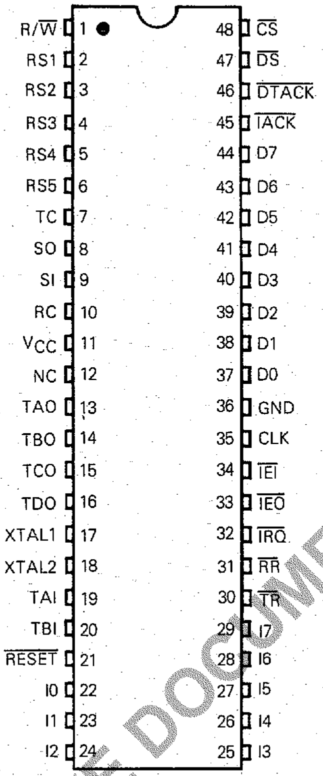
NOTES:

1. Error may be cumulative if repetitively performed.
2. Error with respect to t_{out} or $\overline{IRQ}$ if note 3 is true.
3. Assuming it is possible for the timer to make an interrupt request immediately.

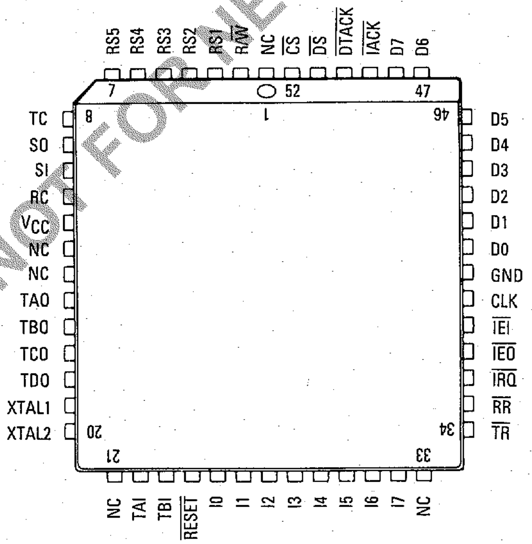
SECTION 8
MECHANICAL DATA AND ORDERING INFORMATION

This section contains the pin assignments, package dimensions, and ordering information for the MC68901.

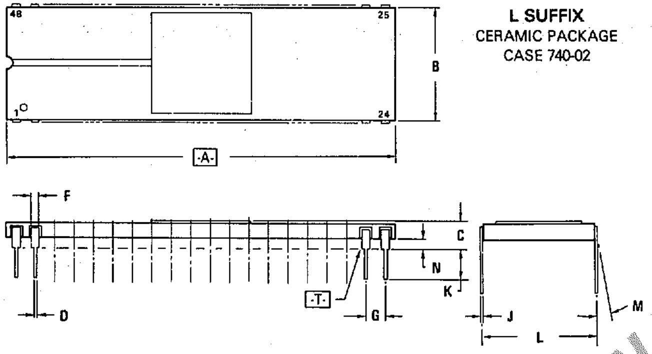
8.1 PIN ASSIGNMENTS



52-Lead Quad MC68901
(Top View)



8.2 PACKAGE DIMENSIONS

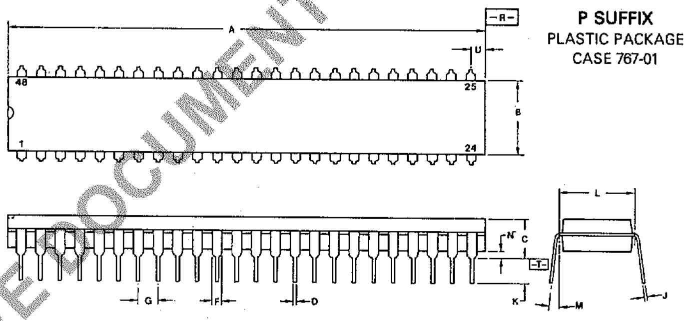


L SUFFIX
CERAMIC PACKAGE
CASE 740-02

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	60.35	61.57	2.376	2.424
B	14.63	15.34	0.576	0.604
C	3.05	4.32	0.120	0.160
D	0.381	0.533	0.015	0.021
F	0.762	1.397	0.030	0.055
G	2.54 BSC		0.100 BSC	
J	0.203	0.330	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.99	15.65	0.590	0.616
M	0°	10°	0°	10°
N	1.016	1.524	0.040	0.060

NOTES:

1. DIMENSION -A- IS DATUM.
2. POSTIONAL TOLERANCE FOR LEADS:
   ⌖ | Ø 0.25 (0.010) Ⓜ | T | A Ⓜ
3. -T- IS SEATING PLANE.
4. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.



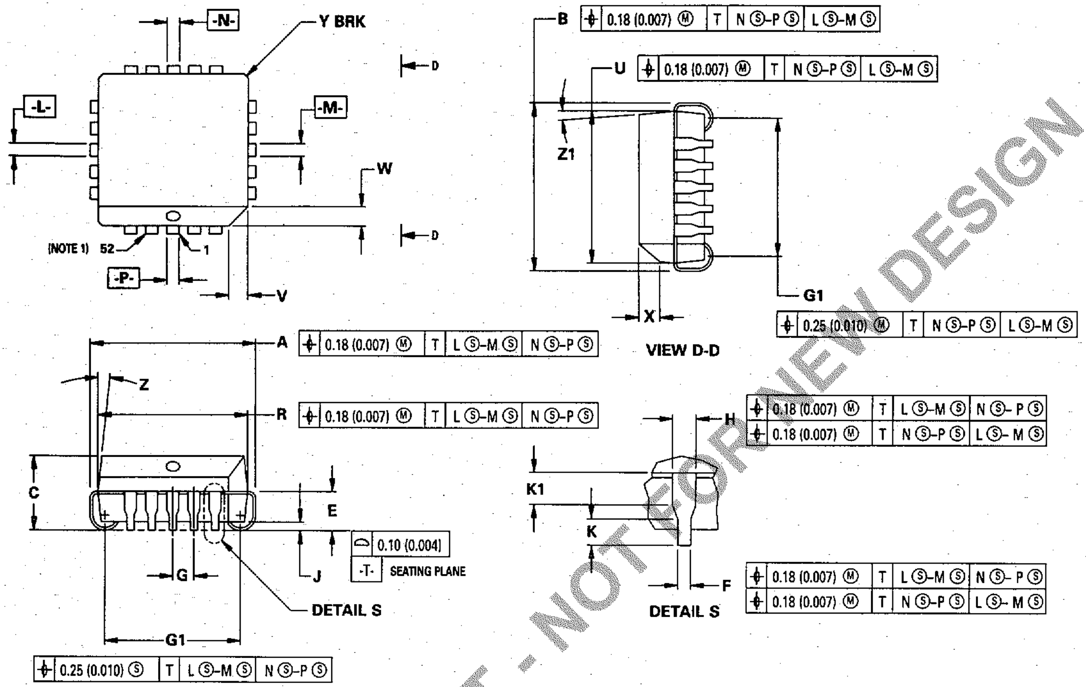
P SUFFIX
PLASTIC PACKAGE
CASE 767-01

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	61.67	61.77	2.428	2.432
B	13.92	14.02	0.548	0.552
C	4.83	5.06	0.190	0.200
D	0.38	0.50	0.015	0.020
F	1.22	1.34	0.048	0.053
G	2.54 BSC		0.100 BSC	
J	0.25	0.30	0.010	0.012
K	3.23	3.37	0.127	0.133
L	15.24 BSC		0.600 BSC	
M	0°	10°	0°	10°
N	0.64	0.88	0.025	0.035
U	1.79 BSC		0.070 BSC	

NOTES:

1. -R- IS END OF PACKAGE DATUM PLANE.
   -T- IS BOTH A DATUM AND SEATING PLANE.
2. POSITIONAL TOLERANCE FOR LEADS 24 & 25:
   ⌖ | 0.35 (0.014) | T | B Ⓜ | R
   POSITIONAL TOLERANCE FOR LEAD PATTERN:
   ⌖ | 0.25 (0.010) | T | B Ⓜ
3. DIM B DOES NOT INCLUDE MOLD FLASH.
4. DIM L IS TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

FN SUFFIX
CASE 778-02
PIN GRID ARRAY



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.94	20.19	0.785	0.795
B	19.94	20.19	0.785	0.795
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	19.05	19.20	0.750	0.756
U	19.05	19.20	0.750	0.756
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	18.04	18.54	0.710	0.730
K1	1.02	—	0.040	—
Z1	2°	10°	2°	10°

NOTES:

1. DUE TO SPACE LIMITATION, CASE 778-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 52 LEADS.
2. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.

8.3 ORDERING INFORMATION

Package Type	Maximum Clock Frequency	Temperature Range	Order Number
Ceramic L Suffix	4.0 MHz	0°C to 70°C	MC68901L
Plastic P Suffix	4.0 MHz	0°C to 70°C	MC68901P
Quad Pack FN Suffix	4.0 MHz	0°C to 70°C	MC68901FN

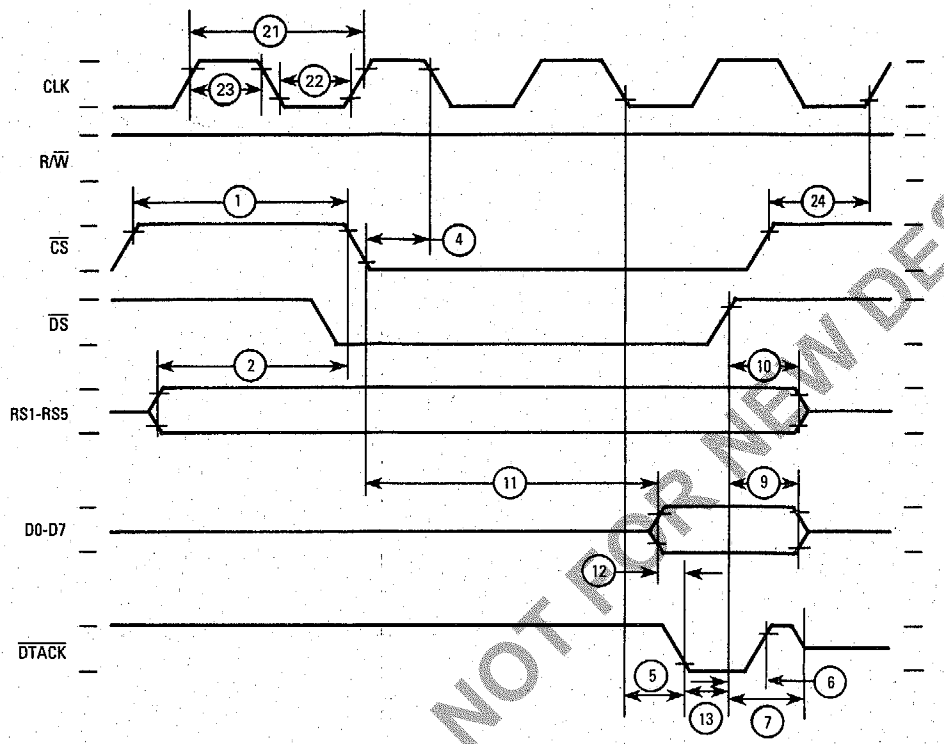


Figure 7-3. Read Cycle Timing

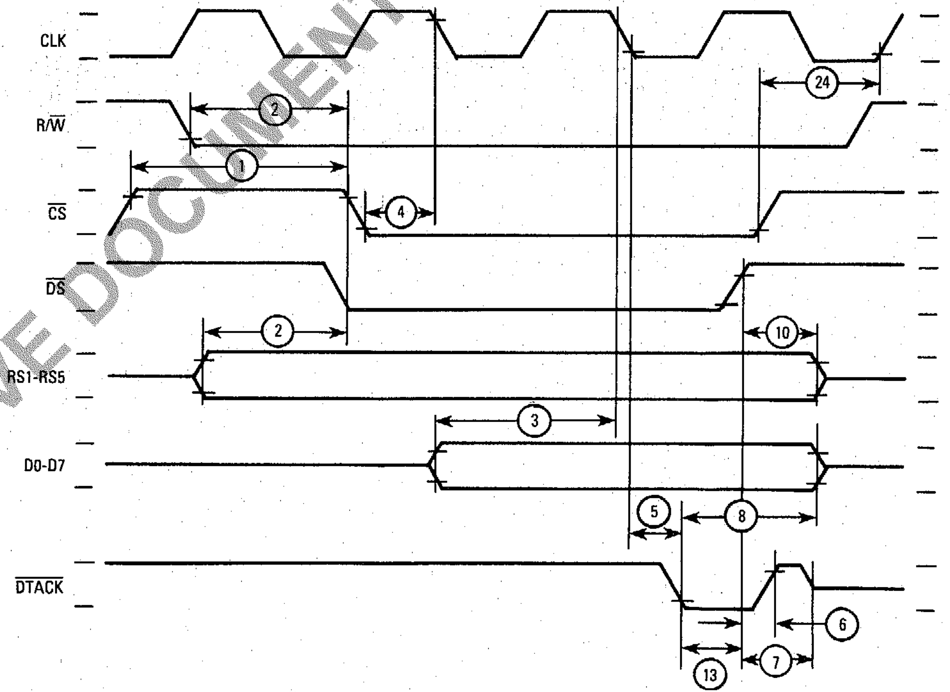
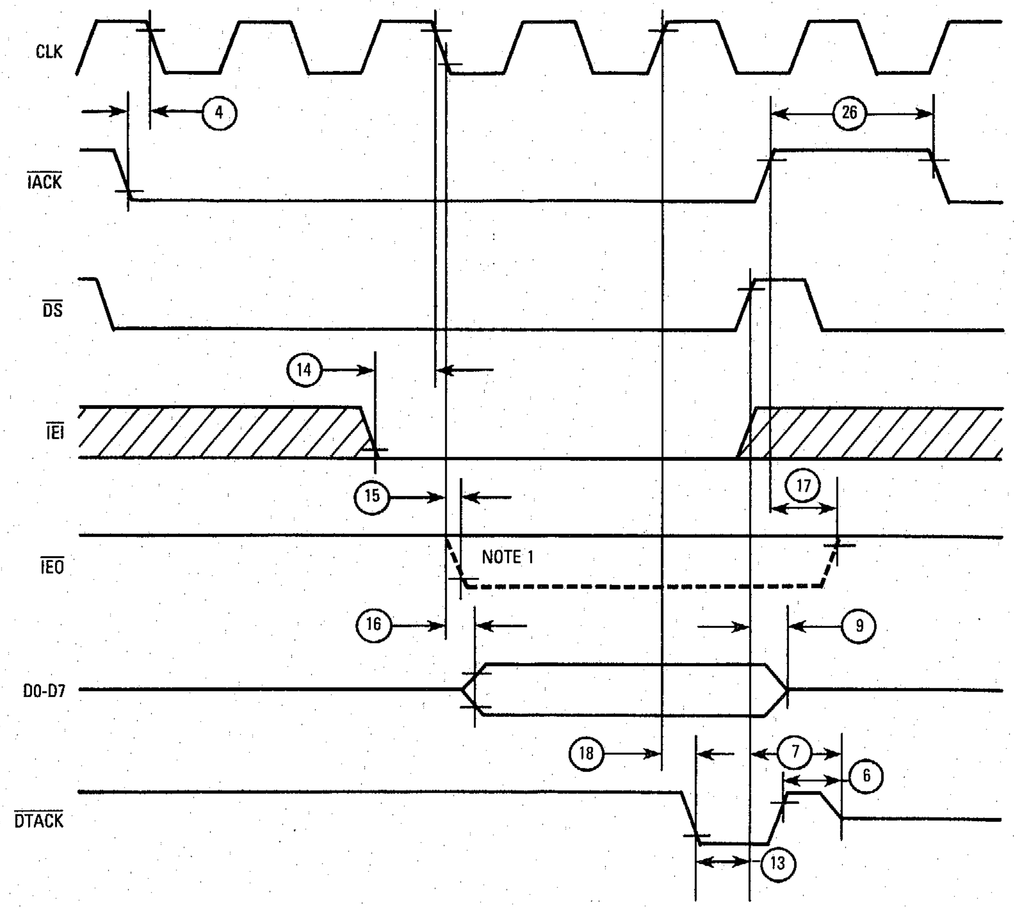
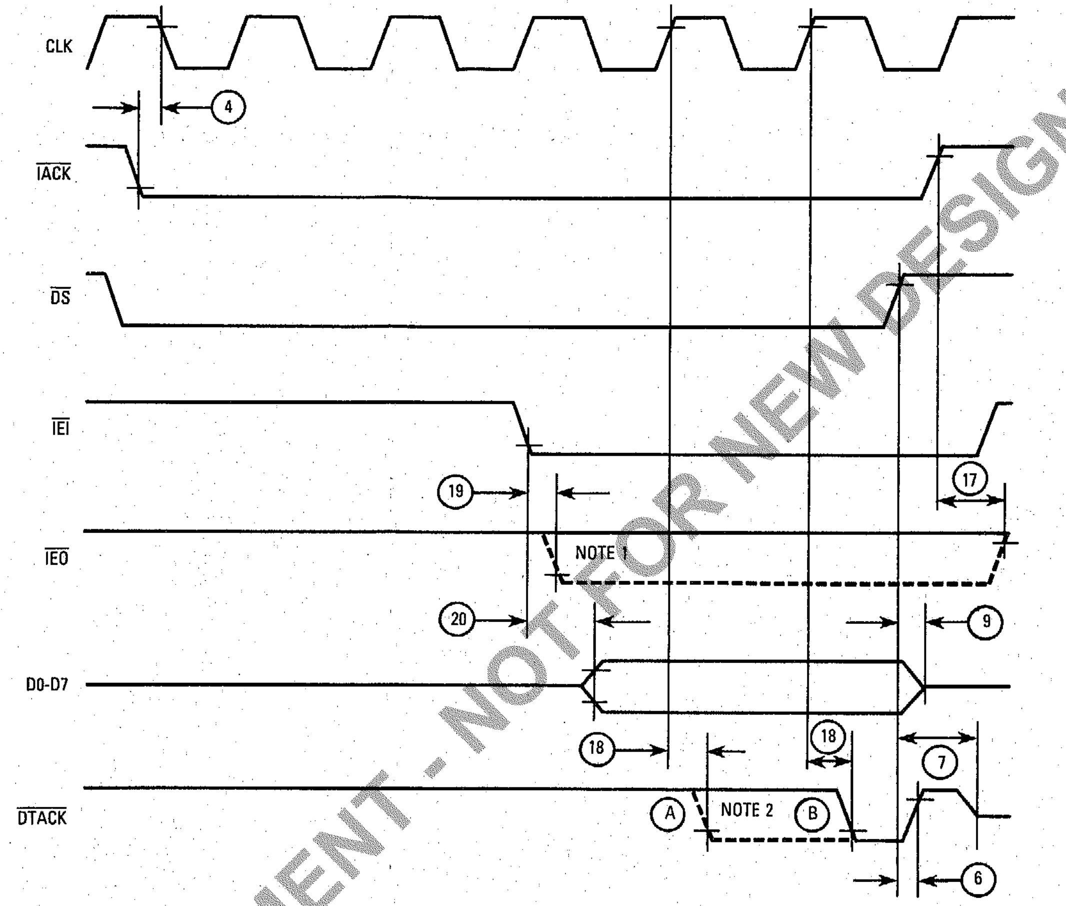


Figure 7-4. Write Cycle Timing



NOTE 1: $\overline{IEO}$ only goes low if no acknowledgable interrupt is pending. If $\overline{IEO}$ goes low, $\overline{DTACK}$ and the data bus remain in the high-impendance state.

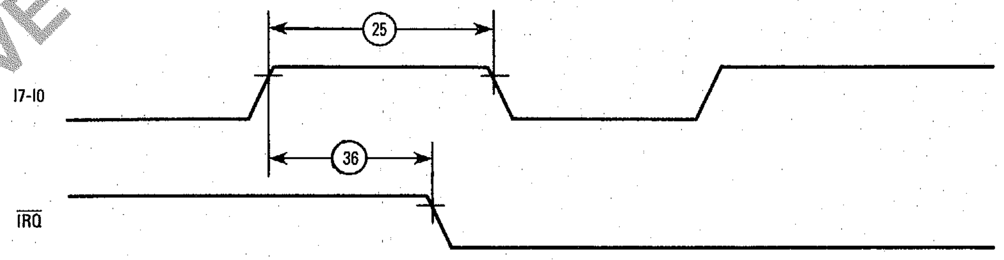
Figure 7-5. Write Cycle Timing



NOTES:

1. $\overline{\text{IEO}}$ only goes low if no acknowledge interrupt is pending. If $\overline{\text{IEO}}$ goes low, $\overline{\text{DTACK}}$ and the data bus remain in the high-impedance state.
2. $\overline{\text{DTACK}}$ will go low at Ⓐ if specification number ⑭ is met. Otherwise, $\overline{\text{DTACK}}$ will go low at Ⓑ.

Figure 7-6. Interrupt Acknowledge Cycle ($\overline{\text{IEI}}$ High)



NOTE: Active Edge is assumed to be the rising edge.

Figure 7-7. Interrupt Timing

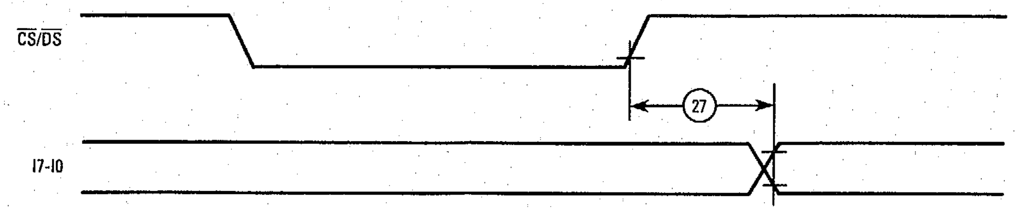


Figure 7-8. Port Timing

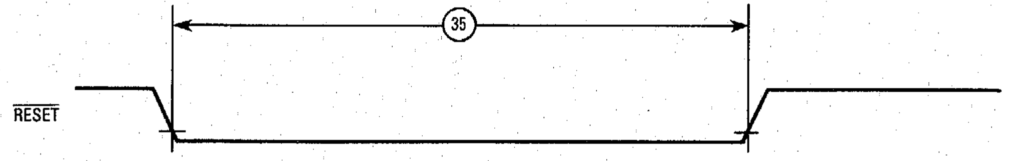


Figure 7-9. Reset Timing

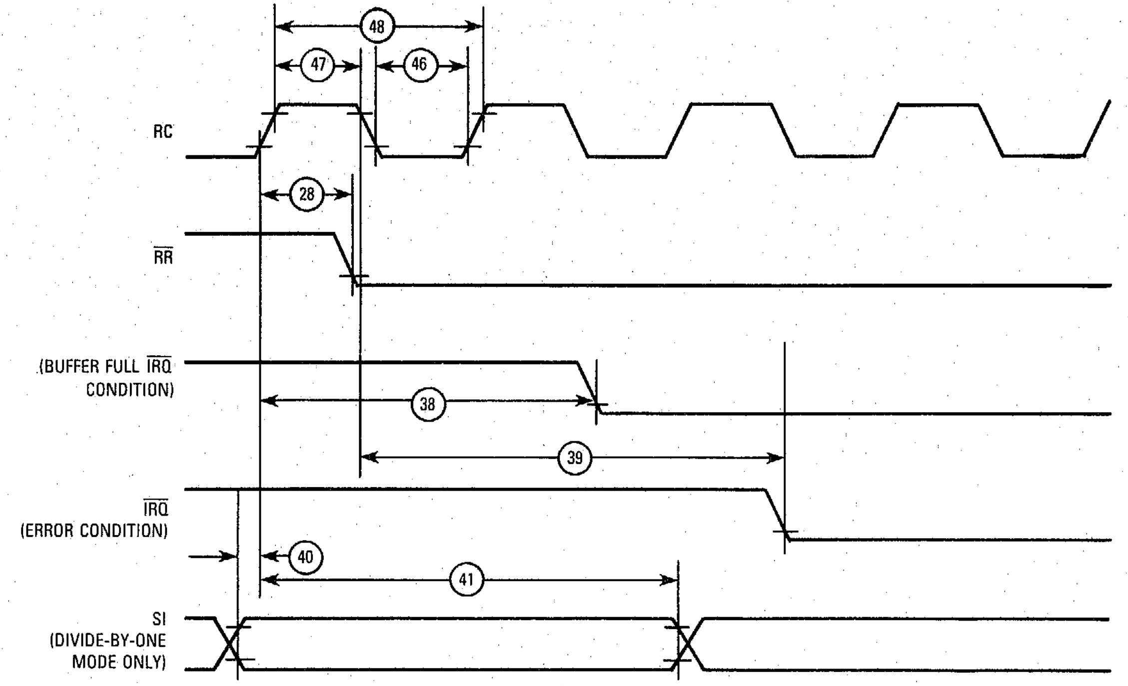


Figure 7-10. Receiver Timing

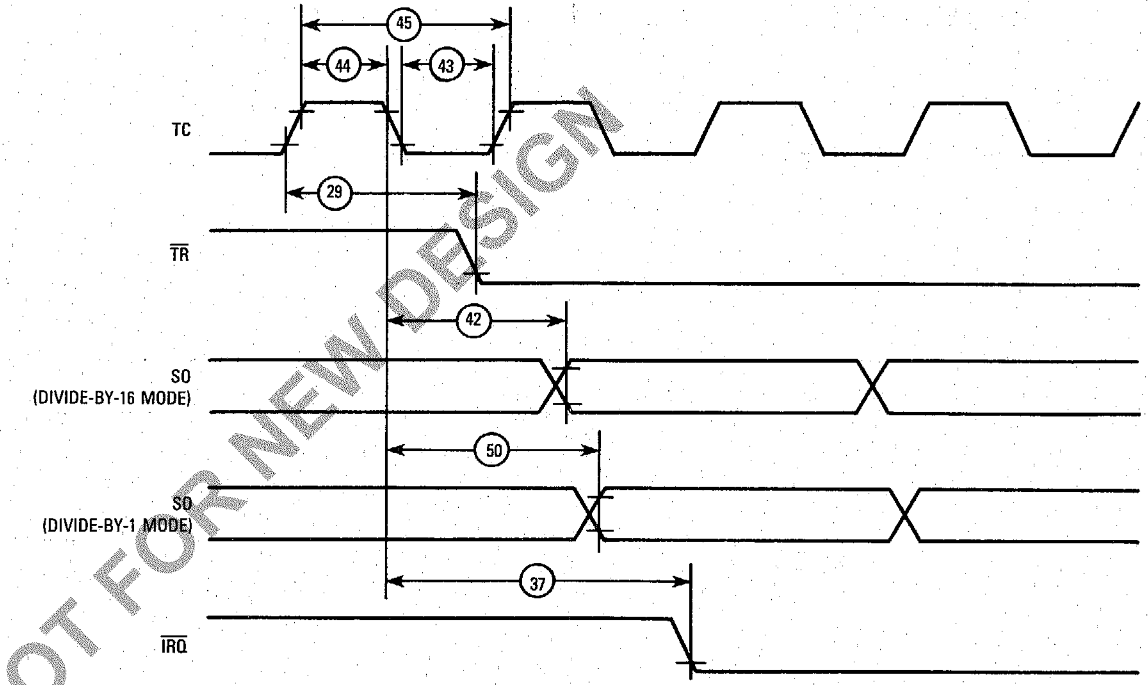
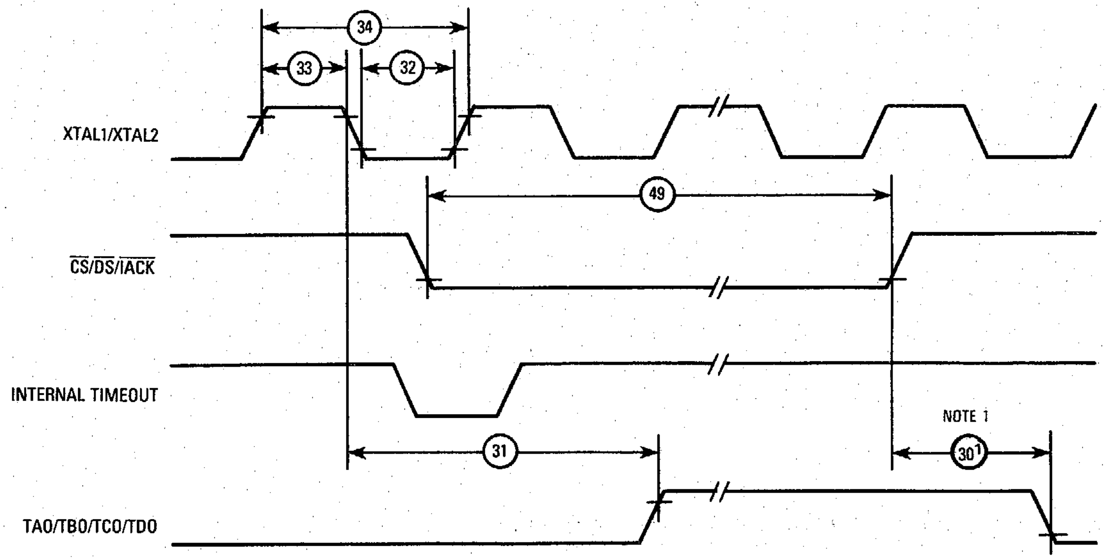


Figure 7-11. Transmitter Timing



NOTE 1: Specification number 30 applies to timer outputs TAO and TBO only.

Figure 7-12. Timer Timing

Literature Distribution Centers:

USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.
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