MOTOROLA
Semiconductor Technical Data

Order Number: MC33888FB/D
Rev. 1.6, 06/2001

Advance Information

Quad High Side and Octal Low Side Switch for Automotive

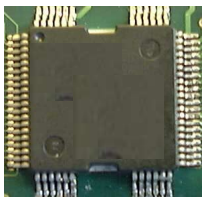
MC33888FB

SOLID STATE RELAY FOR AUTOMOTIVE APPLICATIONS

SEMICONDUCTOR TECHNICAL DATA

MO188 Jedec Package

PACKAGE

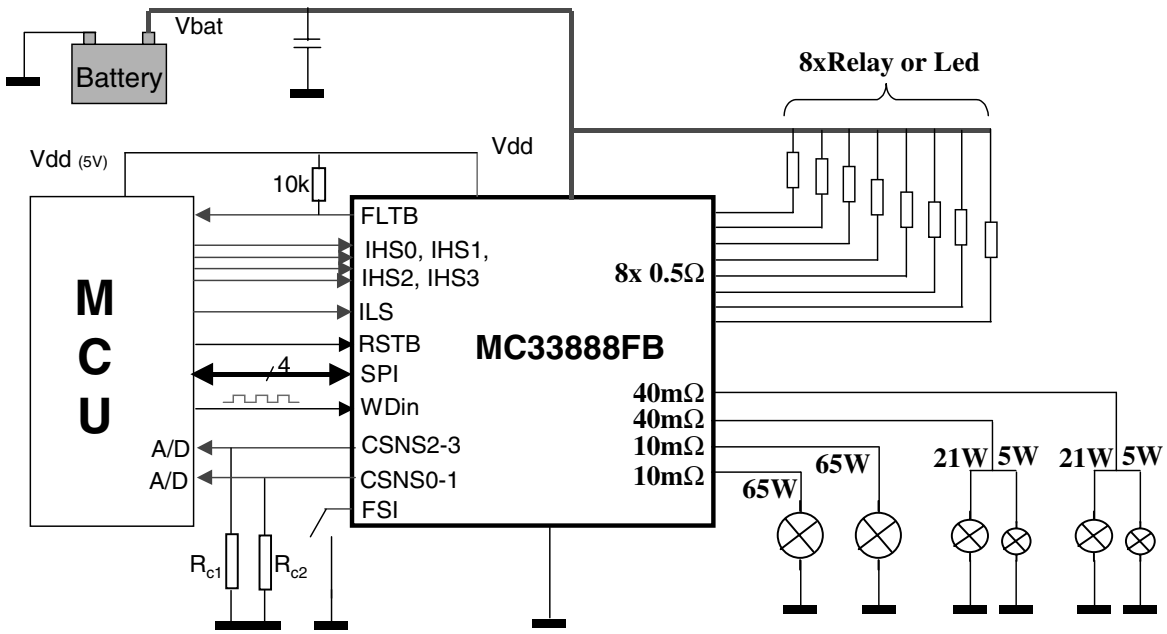


MO188
64 pins
0.65 pitch

This QHSOLSS is a single packaged combination of four discrete high-side FETs and an integrated IC consisting of eight low-side drivers with appropriate control, protection, and diagnostic features. The high-side drivers are useful for both internal and external vehicle lighting applications as well as capable of driving inductive solenoid loads. The low-side drivers are capable of controlling low current on/off type inductive loads, such as relays and solenoids as well as LED indicators and small lamps. The device will be useful in body control, instrumentation, and other high power switching applications and systems.

- Operating Voltage Range from 6V to 27V
- Maximum Breakdown Voltage greater than 41V
- Protected in case of loss of ground, loss of Vbat
- Enhanced -16V Reverse Battery Protection (MOSFETs turned ON)
- Surface Mount Power Package
- Dual 10mΩ High Side, Dual 40mΩ High Side, Octal 500mΩ Low Side
- Configurable SPI and/Or Direct High Side Control
- SPI Low Side Control with Single Configurable Direct Input
- SPI or Direct Fed Watchdog
- SPI Diagnostics
- Individual Overtemperature Protection with Hysteresis
- Configurable Open Load Detection in Off-State
- Short-Circuit Protection to ground and to Vbat.
- Configurable High Side Current Sense
- Configurable High Side Current limitation
- Under and Over Voltage Protection
- Standby Current less than 80µA at V_{bat}<14V and Tj<85°C.

Simplified Application Schematic



This document contains information on a new product. Specifications and information herein are subject to change without notice.

MOTOROLA digital dna™

Figure 1. Internal Block Diagram

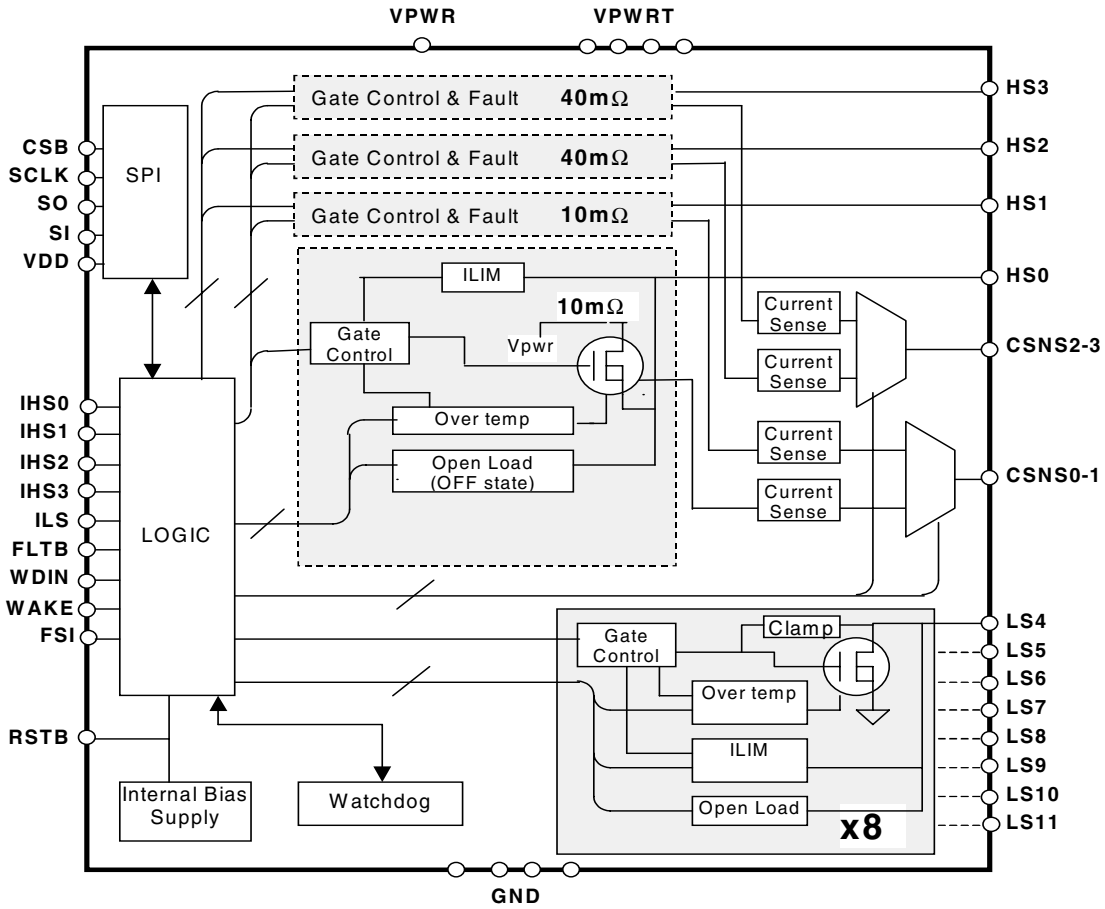
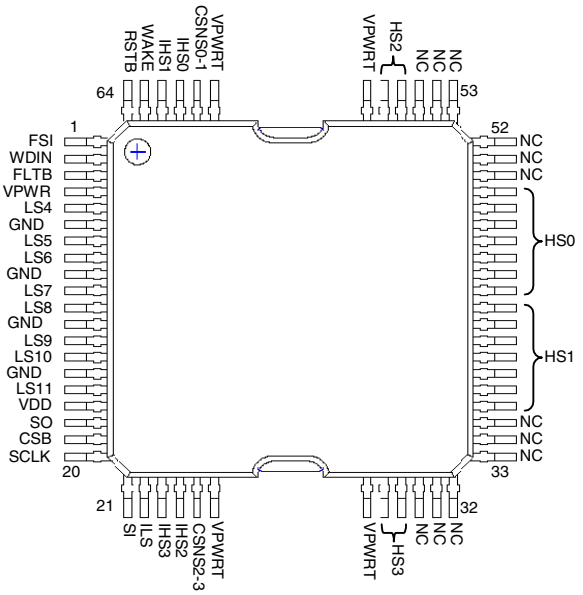


FIGURE 1: QHSOLSS BLOCK DIAGRAM



Pinout Description

PINS FUNCTION DESCRIPTION

Pin Number	pin name	Description
6,9,12,15	GND	Ground. These pins serve as the ground for the source of the low-side output transistors as well as the logic portion of the device.
4	VPWR	Battery Voltage
43-49 36-42	HS0 HS1	Each pin is the source of a 10m Ohm FET, high-side driver, which delivers current through the connected loads. These outputs can be controlled via SPI or using the IHS pins depending on the internal configuration. These outputs are current limited and thermally protected. During failsafe mode, output HS0 will be turned on until the device is reinitialized and then immediately followed by normal operation.
56, 57 28, 29	HS2 HS3	Each pin is the source of a 40m Ohm FET, high-side driver which delivers current through the connected loads. These outputs can be controlled via SPI or using the IHS pins depending on the internal configuration. These outputs are current limited and thermally protected. During failsafe mode, output HS2 will be turned on until the device is reinitialized and then immediately followed by normal operation.
61 62 24 23	IHS0 IHS1 IHS2 IHS3	Each High-Side Input pin is used to directly control only one designated HSO output. These inputs may or may not be activated depending upon the configured state of the internal logic.
60 25	CSNS0-1, CSNS2-3	The Current Sense pins deliver a ratioed amount of the high-side output currents that can be used to generate signal ground referenced output voltages for use by the microcontroller. Each respective CSNS pin can be configured via SPI to deliver current from either of the two assigned outputs, or the currents could be the sum of the two. Current from HS0 and/or HS1 are sensed via CSNS0-1. Current from HS2 and/or HS3 are sensed via CSNS2-3.
5 8 11 14	LS4 LS6 LS8 LS10	Each LS pin is one 0.6 Ohm low-side output FET drain which pulls current through the connected loads. Each of the outputs are actively clamped at 53V. These outputs are current and thermal overload protected. Maximum steady state current through each of these outputs is 500mA.
7 10 13 16	LS5 LS7 LS9 LS11	Each LS pin is one 0.6 Ohm low-side output FET drain which pulls current through the connected loads. Each of the outputs are actively clamped at 53V. These outputs are current and thermal overload protected. Maximum steady state current through each of these outputs is 800mA
22	ILS	The low-side input pin is used to directly control a number of the low-side devices as configured by SPI. This pin may or may not be activated depending upon the configured state of the internal logic.
20	SCLK	The Serial Clock Pin is connected to the SCLK pin of the master device which is a bit (shift) clock for the SPI port. It transitions 1 time per bit transferred at an operating frequency, fSPI and is idle between command transfers. It is 50% duty cycle, and has CMOS logic levels. This signal is used to shift data to and from the device..
21	SI	The Serial Input is connected to the SPI Serial Data Output pin of the master device from which it receives output command data. This input has an internal active pull-down and requires CMOS logic levels. The serial data transmitted on this line is a 16 bit control command sent MSB first, which controls the twelve output channels. Bits D0-D3 control the high-side outputs HS0-HS3, respectively. Bits D4-D11 control the low-side outputs LS4-LS11, respectively. The master will ensure that data is available on the falling edge of SCLK.

PINS FUNCTION DESCRIPTION

18	SO	The Serial Output pin is connected to the SPI Serial Data Input pin of the master device or to the SI pin of the next device in a daisy chain. This output will remain tri-stated unless the device is selected by a low CSB pin. The output signal generated will have CMOS logic levels and the output data will transition on the rising edges of SCLK. The serial output data provides fault information for each output and is returned MSB first when the device is addressed. Fault bit assignments for return data are as follows: OD11 through OD0 are output fault bits for outputs 11 through 0, respectively.
19	CSB	The Chip Select Bar pin is connected to a chip select output of an LSI IC. This IC controls which device is addressed by pulling the CSB pin of the desired device low, enabling the SPI communication with the device, while other devices on the serial link keep their serial outputs tri-stated. This input has an internal active pull-up and requires CMOS logic levels.
64	RSTB	The Reset pin is used to initialize the device configuration and fault registers, as well as place the device in a low current standby mode. This pin also starts the watchdog timeout when transitioned from logic L to logic H. This pin should not be allowed to be at logic H until the VCC is in regulation. This input has an internal passive pull-down.
63	WAKE	This pin is a logic input that starts the device watchdog timeout when brought to a logic H. This pin will have an internal clamp which will protect the pin from high voltages when current is limited with an external resistor.This input has a passive internal pull-down.
2	WDIN	The Watchdog Input pin is a CMOS logic level input that is used to monitor system operation. If the incoming watchdog signal does not transition within the normal watchdog timeout range, then the device will operate in the failsafe mode.This input has an active internal pull-down.
17	VDD	SPI logic power supply.
3	FLTB	The Fault output is an open drain indication that goes active low when a fault mode is detected by the device. Specific device fault indication is given via the SO pin.
1	FSI	The FailSafe Input pin level determines the state of the outputs after a watchdog timeout occurs. This pin has an internal pull-up. If the FSI pin is left to float to a logic H, then HS0 and HS2 will turn on when in the failsafe state. If the FSI pin is tied to GND, then the watchdog circuit and failsafe operation will be disabled, thus allowing operation without a watchdog signal.
30,31,32 33,34,35 50,51,52 53,54,55	NC1 NC2 NC3 NC4	These pins are not connected to the die. Although the NCx pins can be tied to any potential (or left to float), all pins sharing the same NCx designation must be tied to the same potential because they are internally connected together.
26, 27, 58, 59, TAB	VPWRT	These pins are tied to the backside TAB

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Power Supply Voltage Steady State	VPWR(sus)	-16 to 41	V
Input Pin Voltage (Note 1)	VIN	-0.3 to 7.0	V
WAKE Input Pin Clamp Current	WICI	2.5	mA
LS 4,6,8,10 Continuous Per Output Current (Note 2)	IOUTLS4,6,8,10	500	mA
LS 5,7,9,11 Continuous Per Output Current (Note 2)	IOUTLS5,7,9,11	800	mA
HS0,1 Continuous Per Output Current (Note 3)	IOUTHS0,1	10	A
HS2,3 Continuous Per Output Current (Note 3)	IOUTHS2,3	5	A
HS0,1 Output Clamp Energy (Note 4)	EHS0,1	1.5	J
HS2,3 Output Clamp Energy (Note 5)	EHS2,3	1.2	J
LS Output Clamp Energy (Note 6)	ELS	50	mJ
Storage Temperature	Tstg	-55 to 150	Deg C
Operating Junction Temperature	Tjunc	-40 to 150	Deg C
Control Die Thermal Resistance (C/W) One LS on All LS on	theta Cjc	 12 5	 C/W
Power Die Thermal Resistance (C/W) One HS2,3 on All HSx on	theta Pjc	 4 2	 C/W C/W
Ambient Thermal Resistance	theta ja		C/W
ESD Voltage Human Body Model (Note 7) Machine Model (Note 8) Module (Note 9)	 VESD1 VESD2 VESD3	 2000 200 10000	 V V V

NOTES:
1 Exceeding voltage limits on SCLK, SI, CSB, WDin, RSTB, IHS, FSI or ILS pins may cause permanent damage to the device.
2 Low-side output continuous output rating so long as maximum junction temperature is not exceeded. Operation at 125 Deg C ambient temperature will require maximum output current computation using package thermal resistances
3 High-side output continuous output rating so long as maximum junction temperature is not exceeded. Operation at 125 Deg C ambient temperature will require maximum output current computation using package thermal resistances
4 Active HS0,1 clamp energy using the following conditions: single pulse data pending
5 Active HS2,3 clamp energy using the following conditions: single pulse data pending
6 Active LS clamp energy using the following conditions: single non-repetitive pulse, 450mA, Tj=150C
7 ESD1 testing is performed in accordance with the Human Body Model (Czap = 100pF, Rzap = 1500Ohms)
8 ESD2 testing is performed in accordance with the Machine Model (Czap = 100pF, Rzap = 0Ohm)
9 ESD3 testing is performed in accordance with the system module specification and will include at least 0.01uF of capacitance external to the device on each tested output (HS0-3, LS4-11, VPWR)

ELECTRICAL CHARACTERISTICS (VPWR from 6 to 27V, VDD from 4.5V to 5.5V and Tj from -40° to 150°C, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
STATIC CHARACTERISTICS					
Supply Voltage Range Full Operational	VPWR	6.0		27.0	V
VPWR Supply Current	IPWR(on)			20	mA
VPWR Supply Current (all Outputs OFF, Open Load Detect Disabled, WAKE=H, RSTB=H)	IPWR(sby)			5	mA
Sleep State Supply Current (VPWR < 14V, RSTB <0.5V, WAKE<0.5V) Tj=85C Tj=25C	IPWR(ss)			 80 25	 uA uA
Logic Supply Voltage Range	VDD	4.5	5.0	5.5	V
Logic Supply Current	IDD(on)			5	mA
Logic Supply Sleep State Current	IDD(ss)			5	uA
Sleep State LS Output Leakage Current (per LS Output, RSTB = L) Tj=85C Tj=25C	LSLK(ss)			 3 1	 uA uA
Overvoltage Shutdown	VPWROV	28	32	36	V
Overvoltage Shutdown Hysteresis	VPWROV(hyst)	0.2	0.8	1.5	V
Undervoltage Output Shutdown (Note 1)	VPWRUV	5.0	5.5	6.0	V
Undervoltage Power On Reset (Note 2)	UVPOR			5.0	V
Undervoltage Shutdown Hysteresis	VPWRUV(hyst)	0.1		0.5	V
Current Sense Ratio: CSNS0-1/HS0, (CSNS0-1/HS1) (VPWR=9V-16V, CNS <4.5V)	CSR0-1		1/1400		
Current Sense Ratio (CSR0-1) Accuracy HS0,1 Output Current: 1A 2A 5A 6.5A 10A	CSA0-1	 -35 -19 -14 -12 -9		 +35 +19 +14 +12 +9	 %
Current Sense Ratio: CSNS2-3/HS2, (CSNS2-3/HS3) (VPWR=9V-16, CNS <4.5V)	CSR2-3		1/880		
Current Sense Ratio (CSR2-3) Accuracy HS2,3 Output Current: 0.5A 1A 3A 3.7A 5A	CSA2-3	 -30 -19 -13.5 -12 -9		 +30 +19 +13.5 +12 +9	 %
Max Current Sense Voltage Clamp (ICNS=15mA)	SVmax	4.5	6	7	V

HS0,1 POWER OUTPUT CHARACTERISTICS

HS0,1 Drain-to-Source ON Resistance (IOUT=5.5A,TJ=25 Deg C) VPWR = 6.0V VPWR = 9.0V VPWR = 13V	HS01RON25			 0.020 0.01 0.01	 Ohms Ohms Ohms
HS0,1 Drain-to-Source ON Resistance (Iout=5.5A, TJ=150 Deg C) VPWR=6.0V VPWR=9.0V VPWR=13V	HS01RON150			 0.034 0.017 0.017	 Ohms Ohms Ohms
HS0,1 Reverse Battery Source-to-Drain ON Resistance (Iout=-5.5A, TJ=25 Deg C) VPWR=-12V	HS01RONRev			 0.020	 Ohms
Output Self Limiting Peak Current Outputs ON, Vout=0.3V Outputs ON, Vout=4.0V	HS01ilimpk	 1 35	 10 40	 60 60	 A
Output Self Limiting Sustain Current Outputs ON, Vout=0.3V Outputs ON, Vout=4.0V	HS01ilimsus	 1 15	 24	 30 30	 A
Open Load Detect Current (Note 3)	HS01OLDC	30		100	uA
Output Fault Detect Threshold Output Programmed OFF	HS01OLDV	2	3	4	V
Output Negative Clamp Voltage 0.5A<=Iout<=2A, Output OFF	HS01VCL	-20			V
Over-temperature Shutdown (Outputs OFF) (Note 6)	HS01TLIM	160	170	190	Deg C
Over-temperature Shutdown Hysteresis (Note 6)	TLIM(hyst)	10	20	30	Deg C

HS2,3 POWER OUTPUT CHARACTERISTICS

HS2,3 Drain-to-Source ON Resistance (IOUT=4.5A,TJ=25 Deg C) VPWR = 6V VPWR = 9.0V VPWR = 13V	HS23RON25			 0.08 0.04 0.04	 Ohms Ohms Ohms
HS2,3 Drain-to-Source ON Resistance (Iout=4.5A, TJ=150 Deg C) VPWR=6V VPWR=9.0V VPWR=13V	HS23RON150			 0.136 0.068 0.068	 Ohms Ohms Ohms
HS2,3 Reverse Battery Source-to-Drain ON Resistance (Iout=-4.5A, TJ=25 Deg C) VPWR=-12V	HS23RonRev			 0.08	 Ohms
Output Self Limiting Peak Current Outputs ON, Vout=0.3V Outputs ON, Vout=4.0V	HS23ilimpk	 0.5 15	 6 20	 35 35	 A
Output Self Limiting Sustain Current Outputs ON, Vout=0.3V Outputs ON, Vout=4.0V	HS23ilimsus	 0.5 6	 11	 15 15	 A
Open Load Detect Current (Note 3)	HS23OLDC	30		100	uA

Output Fault Detect Threshold (Note 4) Output Programmed OFF	HS23OLDV	2	3	4	V
Output Negative Clamp Voltage 0.5A<=Iout<=2A, Outputs OFF	HS23VCL	-20			V
Over-temperature Shutdown (Outputs OFF) (Note 6)	HS23TLIM	160	170	190	Deg C
Over-temperature Shutdown Hysteresis (Note 6)	TLIM(hyst)	10	20	30	Deg C

LOW-SIDE POWER OUTPUT CHARACTERISTICS

Drain-to-Source ON Resistance (IOUT=0.3A,TJ=25 Deg C) VPWR = 6.0V VPWR = 9.0V VPWR = 13V	LSRon			 1.0 0.7 0.6	 Ohms Ohms Ohms
Drain-to-Source ON Resistance (Iout=0.3A, TJ=150 Deg C) VPWR=6.0V VPWR=9.0V VPWR=13V	LSRon			 1.8 1.1 0.9	 Ohms Ohms Ohms
LS4,6,8,10 Output Self Limiting Current Outputs Programmed ON, Vout=3.0V	LS4,6,8,10 ILIM	0.5	0.9	1.4	A
LS5,7,9,11 Output Self Limiting Current Outputs Programmed ON, Vout=3.0V	LS5,7,9,11 ILIM	0.8	1.3	1.9	A
Output OFF Open Load Detect Current (Note 3) Output Programmed OFF, Vout=3.0V	LSOLDC	30	50	100	uA
Output Fault Detect Threshold (Note 5) Output Programmed OFF	LSOLDV	2.0	3.0	4.0	V
Output Clamp Voltage 2.0mA =< IOUT <= 200mA, Outputs OFF	LSVCLMP	41	53	60	V
LS Body Diode Voltage (I=-300mA, Ta=150 C)	LSBDV	TBD	0.6	TBD	V
Over-temperature Shutdown (Outputs OFF) (Note 6)	LSTLIM	160	170	190	Deg C
Over-temperature Shutdown Hysteresis (Note 6)	TLIM(hyst)	10	20	30	Deg C

NOTES:
1 SPI I/O and internal logic operational. Outputs will recover in instructed state when VPWR voltage level returns to normal as long as the level does not go below UVPOR.
2 VPWR Voltage levels less than UVPOR will result in a reinitialization of all internal logic when the level returns to normal levels.
3 Output OFF Open Load Detect Current is the current required to flow through the load for the purpose of detecting the existence of an open load condition when the specific output is commanded OFF.
4 Output fault detect threshold with outputs programmed OFF.
5 Output fault detect threshold with outputs programmed OFF. For the LS Outputs, fault detect thresholds are the same for output open and battery shorts.
6 Guaranteed by Design; not production tested.

DIGITAL INTERFACE TIMING

Characteristic	Symbol	Min	Typ	Max	Unit
Input Logic High Voltage (Note 1)	VIH	3.5			V
Input Logic Low Voltage (Note 1)	VIL			1.0	V
Input Logic Voltage Hysteresis (SI, CSB, SCLK, IHS, ILS) (Note 2)	Vin(hyst)	100	350	750	mV
Input Logic Pulldown Current (SI, SCLK, IHS, ILS, WDIN)	Idwn	5		20	uA

Input Logic Pulldown Resistor (WAKE, RSTB)	Rdwn	100	200	400	kOhm
Input Logic Pullup Current (CSB, FSI, Vin=3.5V) (Note 5)	Iup	5		20	uA
Wake Input Clamp Voltage (WICI < 2.5mA) (Note 4)	WICV	7		14	V
Wake Input Forward Voltage (WICI = - 2.5mA)	WIFV	-2		-0.3	V
SO High State Output Voltage (IOH=1.0 mA)	VSOH	0.8VDD			V
FLTB, SO Low State Output Voltage (IOL=-1.6mA)	VSOL		0.2	0.4	V
SO Tri-State Leakage Current (CSB ≥ 3.5V)	SOLK	-5	0	5	uA
Input Capacitance (Note 3)	Cin		4	12	pF
SO, FLTB Tri-State Capacitance (Note 2)	CSO			20	pF

NOTES:
1. Upper and lower logic threshold voltage range applies to SI, CSB, SCLK, RSTB, IHS0-3, ILS, WAKE and WDIN input signals.The WAKE, FSI, and RSTB signals are derived from an internal supply
2. Parameter is guaranteed by design but is not production tested.
3. Input capacitance of SI, CSB, SCLK, RSTB, IHS0-3, ILS, WAKE and WDIN. This parameter is guaranteed by process monitor but is not production tested.
4. The current must be limited by a series resistance when using voltages higher than the WICV.
5. The CSB is pulled up to VDD.

POWER OUTPUT TIMING

HS Output Rising Slew Rate (Note 1)	SRr	0.1	0.3	1	V/uS
HS Output Falling Slew Rate (Note 1)	SRf	0.1	0.3	1	V/uS
LS & HS Output Turn ON delay Time (Note 2)	Tdly(on)	1.0		200	uS
LS & HS Output Turn OFF delay Time (Note 3)	Tdly(off)	1.0		200	uS
Direct Input Switching Frequecy	PWMf			125	Hz
LS Output Fault Delay Timer (Note 4)	Tdly(flt)	70	150	250	uS
Watchdog timeout (Note 5)	wdto	340	524	707	mS
LS Output Rise Time (Note 6)	LSrt	1		10	uS
LS Output Fall Time (Note 6)	LSft	1		10	uS
Peak Current Limit Timer (Note 7)	Tpct	40	70	100	mS

Notes
1. For HS Output Rise and Fall time respectively, measured across a 5 Ohm resistive load at 10% to 90% voltage points. These parameters are guaranteed by process monitor.
2. For LS Outputs, turn ON delay time measured from rising edge of CSB to 90% of output OFF Vout with RL=27 Ohm resistive load. For HS Outputs, turn ON delay time measured from rising edge of CSB to 90% of output OFF Vout with RL=5 Ohm resistive load.
3. For LS Output, turn OFF delay time measured from rising edge of CSB to 10% of output OFF Vout voltage with RL=27 Ohm resistive load. For HS Output, turn OFF delay time measured from rising edge of CSB to 10% of output OFF Vout voltage with RL=5 Ohm resistive load.
4. Propagation time of Short Fault Disable Report Delay measured from rising edge of CSB to Output disabled, LS=5.0V, and device configured for LS output over current latchoff using CLOCCR.
5. Wdto delay measured from the rising edge of WAKE or RSTB from the sleep state, to the HS0,1 turn-on with the outputs driven OFF and the FSI floating. The accuracy of wdto is maintained for all configured watchdog timeouts.
6. For LS Output Rise and Fall time respectively, measured across a 27 Ohm resistive load at 30% to 70% and 70% to 30% voltage points.
7. Tpct measured from the rising edge of CSB to 90% of HSxxilimpk when the peak current limit is enabled.

SPI INTERFACE TIMING(TJ FROM -40° TO 150°C, AND SYMMETRICAL 50% DUTY CYCLE SCLK CLOCK PERIOD OF 333 NS)

Recommended Frequency of SPI Operation	f_{SPI}			3	MHz
Required Low State Duration for RSTB (Note 1)	TwRSTB	-	50	167	nS
Falling edge of CSB to Rising Edge of SCLK (Required Setup Time) (Note 2)	Tlead	-	50	167	nS
Falling edge of SCLK to Rising Edge of CSB (Required Setup Time) (Note 2)	Tlag	-	50	167	nS
SI to Falling Edge of SCLK (Required Setup Time) (Note 2)	TSIsu	-	25	83	nS
Falling Edge of SCLK to SI (Required Hold Time) (Note 2)	TSI(hold)	-	25	83	nS
SO Rise Time (CL=200pF)	TrSO	-	25	50	nS
SO Fall Time (CL=200pF)	TfSO	-	25	50	nS
SI, CSB, SCLK, Incoming Signal Rise Time (Note 3)	TrSI	-	-	50	nS
SI, CSB, SCLK, Incoming Signal Fall Time (Note 3)	TfSI	-	-	50	nS
Time from Falling Edge of CSB to SO Low Impedance (Note 4)	TSO(en)	-	-	145	nS
Time from Rising Edge of CSB to SO High Impedance (Note 5)	TSO(dis)	-	65	145	nS
Time from Rising Edge of SCLK to SO Data Valid (Note 6) 0.2VDD<=SO>=0.8VDD, CL = 200 pF	Tvalid	-	65	105	nS

Notes :
1. RSTB low duration measured with outputs enabled and going to OFF or disabled condition.
2. Maximum setup time required for the QHSOLSS is the minimum guaranteed time needed from the micro.
3. Rise and Fall time of incoming SI, CSB, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
4. Time required for output status data to be available for use at SO. 1 K Ohm pullup on CSB
5. Time required for output status data to be terminated at SO. 1 K Ohm pullup on CSB
6. Time required to obtain valid data out from SO following the rise of SCLK.

SPI Interface and Protocol Description

The SPI interface has full duplex, three wire synchronous data transfer and has four I/O lines associated with it: (SI, SO, SCLK, and CSB). The SI/SO pins of the QHSOLSS follow a first in / first out (D15 / D0) protocol with both input and output words transferring the most significant bit first. All inputs are compatible with 5.0 V CMOS logic levels. During SPI output control, a logic L in a message word will result in the designated output being turned off. Similarly, a logic H will turn on a corresponding output. All specific pin functions are specified as follows:

SCLK – Clocks the internal shift registers of the QHSOLSS. The Serial Input (SI) pin accepts data into the input shift register on the falling edge of the SCLK signal while the serial output pin (SO) shifts data information out of the SO Line Driver on the rising edge of the SCLK signal. It is important that the SCLK pin be in a logic low state whenever the Chip Select Bar (CSB) makes any transition. For this reason, it is recommended that the SCLK pin be kept in a logic L as long as the device is not accessed (CSB in logic H state). SCLK has an internal pull-down “Idwn” . When CSB is logic H, signals at the SCLK and SI pins are ignored and SO is tri-stated (high impedance). See the Data Transfer Timing diagram in Figure 2.

SI – This pin is the input of Serial Instruction data. SI information is read in on the falling edge of SCLK. A sixteen bit stream of serial data is required on the SI pin, starting with D15, D14, etc, to D0. The twelve outputs of the QHSOLSS are configured and controlled using the 3 bit addressing scheme and the twelve assigned data bits designed into the QHSLOSS. SI has an internal pulldown “Idwn” .

SO – The Serial Output data pin is a tri-stateable output from the shift register. The SO pin remains in a high impedance state until the CSB pin is put into a logic L state. The SO data report the status of the outputs as well as provide the capability to reflect the state of the direct inputs. The SO pin changes states on the rising edge of SCLK and reads out on the falling edge of SCLK. When an output is on or off and not faulted, the corresponding SO bit, OD0 – OD11, are a logic L. If the output is faulted, the corresponding SO state is a logic H. SO OD12-OD14 reflect the state of six various inputs (three at a time) depending upon the reported state of the previously written watchdog bit OD15.

CSB – The Chip Select (Bar) pin enables communication with the Master device. When this pin is in a logic L state, the QHSOLSS is capable of transferring information to and receiving information from the Master. The QHSOLSS latches in data from the input shift registers to the addressed registers on the rising edge of CSB. The QHSOLSS transfers status information from the power outputs to the shift registers on the falling edge of CSB. The output driver on the SO pin is enabled when CSB is logic L. CSB is only transitioned from a logic H state to a logic L state when SCLK is a logic L. CSB has an internal pullup “Iup” .

The QHSOLSS is capable of interfacing directly with a microcontroller, via the 16 bit SPI protocol described and specified below

Figure 2. Data Transfer Timing

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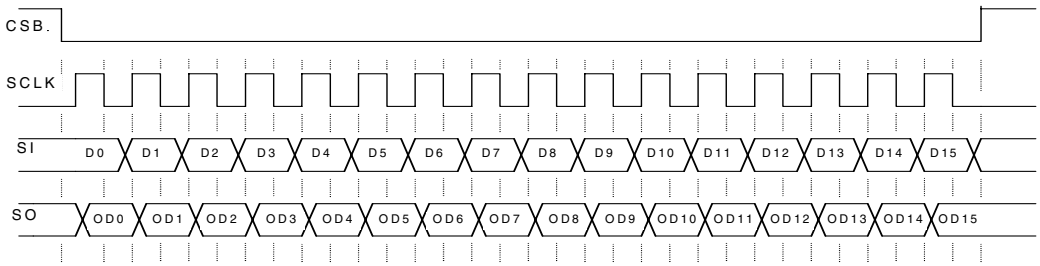
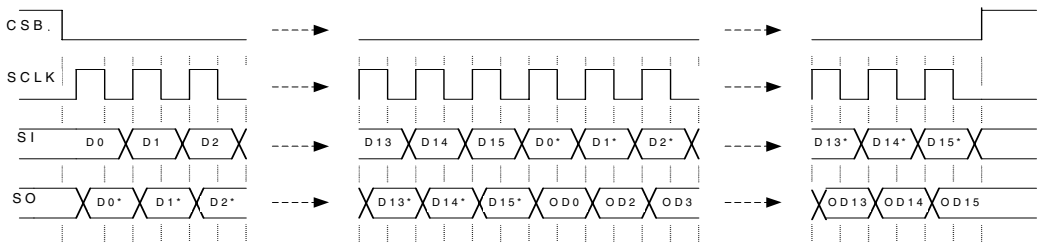


NOTES: 1. RSTB is in a logic H state during the above operation.
2. DO, D1, D2, ... , and D15 relate to the most recent ordered entry of program data into the QHSLOSS
3. OD0, OD1, OD2, ..., and OD15 relate to the first 16 bits of ordered fault and status data out of the QHSLOSS

FIGURE 2a. SINGLE 16bit WORD SPI COMMUNICATION



NOTES: 1. RSTB is in a logic H state during the above operation.
2. DO, D1, D2, ... , and D15 relate to the most recent ordered entry of program data into the QHSLOSS
3. D0*, D1*, D2*, ..., and D15* relate to the first 16 bits of ordered entry data into the QHSLOSS
4. OD0, OD1, OD2, ..., and OD15 relate to the first 16 bits of ordered fault and status data out of the QHSLOSS

FIGURE 2b. MULTIPLE 16bit WORD SPI COMMUNICATION

SI COMMUNICATION

SPI communication will be accomplished via 16bit messages. A message is transmitted by the master starting with the MSB D15 and ending with the LSB D0. Each incoming command message on the SI pin can be interpreted using the following bit assignment: the first twelve LSBs, D0-11, control each of the twelve outputs, the next three bits, D12-D14, determine the command mode, and the MSB, D15, is the watchdog bit (see TABLE 1). Multiple messages can be transmitted in succession to accommodate those applications where daisy chaining is desirable, or to confirm transmitted data, as long as the messages are all multiples of 16bits. If an attempt is made to latch in a message that is not 16bits, then it is ignored.

The QHSOLSS has 6 registers which are used to configure the device and control the state of the four high-side and eight low-side outputs. The registers are addressed via D12-D14 of the incoming SPI word (see TABLE 1).

Table 1 • SI MESSAGE BIT ASSIGNMENT

BIT SIG	SI MESSAGE BIT	MESSAGE BIT DESCRIPTION
MSB	D15	Watchdog in: toggled to satisfy watchdog requirements
	D14	Register Address Bit:
	D13	Register Address Bit
	D12	Register Address Bit
	D11	Used to Configure Low-Side Output LS11
	D10	Used to Configure Low-Side Output LS10
	D9	Used to Configure Low-Side Output LS9
	D8	Used to Configure Low-Side Output LS8
	D7	Used to Configure Low-Side Output LS7
	D6	Used to Configure Low-Side Output LS6
	D5	Used to Configure Low-Side Output LS5 (Watchdog timeout MSB during WDCSCR configuration)
	D4	Used to Configure Low-Side Output LS4 (Watchdog timeout LSB during WDCSCR configuration)
	D3	Used to Configure High-Side Output HS3
	D2	Used to Configure High-Side Output HS2
	D1	Used to Configure High-Side Output HS1
LSB	D0	Used to Configure High-Side Output HS0

The eight possible addresses (D12,D13,D14) and a description of their impact on the device operation is as follows (see TABLE 2):

- Address LLL (SPI Output Control Register (SOCR)) – This register allows the master to control the outputs via the SPI. Incoming message bits D0-3 reflect the desired states of the high-side outputs HS0-HS3. Message bits D4-D11 reflect the desired state of the low-side outputs LS4-LS11 respectively.

- Address LLH (Direct Input Control Register (DICR)) -This register is used by the master to enable direct input control of the outputs. For the outputs, a logic L on bits D0-D11 will enable the corresponding output for direct control. A logic H on a D0-D11 bit will disable the output from direct control.

- Address LHL (Logic Function Control Register (LFCR)) – This register is used by the master to configure the relationship between the SOCR bits D0 – D11 and the Direct Inputs IHSx and ILS. While addressing this register (if the Direct Inputs were enabled for direct control with the DICR), a logic H on any or all of the D0-D3 bits will result in a Boolean AND of the

IHSx pin(s) with its (their) corresponding D0-D3 message bit(s) when addressing the SOCR. A logic H on any or all of the D4-D11 bits will result in a Boolean AND of the ILS and the corresponding D4-D11 message bits when addressing the SOCR. Similarly, a logic L on the D0-D3 pins will result in a Boolean OR of the IHSx pin(s) to their corresponding message bits when addressing the SOCR, and the ILS will be Boolean ORed with message bits D4 – D11 when addressing the SOCR (if ILS enabled).

- Address LHH (Watchdog and Current Sense Configuration Register (WDCSCR)) – This register is used by the master to configure the Watchdog Timeout and the CSNS01 and CSNS23 pins. The Watchdog timeout is configured using bits D4 and D5. The state of D4 and D5 determine the divided value of the wdto. For example, if D4 and D5 are logic LL, respectively, then the wdto will be in the default state as specified in Table 10. A D4D5 of HL will result in a watchdog timeout of wdto ÷ 2. Similarly, a D4D5 of LH results in a watchdog timeout of wdto ÷ 4, and a D4D5 of HH results in a watchdog timeout of wdto ÷ 8. Note that when D4D5 bits are programmed for the desired watchdog timeout period, the WDSPI bit should be toggled as well to insure that the new timeout period is programmed at the beginning of a new count sequence. CSNS01 is the current sense output for the HS0 and HS1 outputs. Similarly, the CSNS23 pin is the current sense output for the HS2 and HS3 outputs respectively. In this mode, a logic H on any or all of the message bits that control the HS outputs will result in the sensed current from the corresponding output to be directed out of the appropriate CSNS output. For example, if D0 and D1 are both logic H, then the sensed current from HS0 and HS1 will be summed into the CSNS01. If D2 is logic H and D3 is logic L, then only the sensed current from HS2 will be directed out of CSNS23.

- Address HLL (Open Load Configuration Register (OLCR)) – This register allows the master to configure each of the outputs for Open Load Fault detection. While in this mode, a logic H on any of the D0-D3 message bits will disable the corresponding outputs' circuitry that allows the device to detect open load faults while the output is off. For the Low side drivers, a logic H on any of the D4-D11 bits will enable the open load detection circuitry. This feature allows the master to minimize load current in some applications, and may be useful to diagnose output shorts to battery (for HS).

- Address HLH (Current Limit Over Current Configuration Register (CLOCCR)) - This register allows the master to individually override the peak current limit levels for each of the High Side outputs. A logic H on any or all of the D0-D3 bit(s) results in the corresponding HSx to current limit at the sustain current limit level. This register also allows the master to enable or disable the over current shutdown of the Low Side outputs. A logic H on any or all ot the D4-D11 message bit(s) will result in the corresponding LSxx to latch off if the current exceeds ILIM after a timeout of tdly(flt).

- Address HHL – Not presently used
- Address HHH – This register is reserved for test and is not accessible via SPI during normal operation.

Table 2 • ADDRESS AND CONFIGURATION BIT MAP

HIGH-SIDE				LOW-SIDE								ADDRESS			WD	REG NAME
D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D 12	D 13	D 14	D 15	
HS 0	HS 1	HS 2	HS 3	LS 4	LS 5	LS 6	LS 7	LS 8	LS 9	LS 10	LS 11	L	L	L	X	SOCR
PW B0	PW B1	PW B2	PW B3	PW B4	PW B5	PW B6	PW B7	PW B8	PW B9	PW B10	PW B11	L	L	H	X	DICR
A/ OB 0	A/ OB 1	A/ OB 2	A/ OB 3	A/ OB4	A/ OB 5	A/ OB 6	A/ OB 7	A/ OB8	A/ OB 9	A/ OB1 0	A/ OB1 1	L	H	L	X	LFCR
CS 0	CS 1	CS 2	CS 3	WD L	WD H	NA	NA	NA	NA	NA	NA	L	H	H	X	WDCSCR
OLB 0	OLB 1	OLB 2	OLB 3	OL 4	OL 5	OL 6	OL 7	OL 8	OL 9	OL 10	OL 11	H	L	L	X	OLCR
ILIM 0	ILIM 1	ILIM 2	ILIM 3	OC 4	OC 5	OC 6	OC 7	OC 8	OC 9	OC 10	OC 11	H	L	H	X	CLOCCR
-	-	-	-	-	-	-	-	-	-	-	-	H	H	L	X	NOT USED
OT	ILIM	WD	ILIM PK									H	H	H	X	TEST

X : don't care
NA Not Applicable

SO Communication (see TABLE 3)

When the CSB pin is pulled low, the output status register for each output is loaded into the output register and the fault data is clocked out MSB (OD15) first, as the new message data is clocked into the SI pin.
OD15 reflects the state of the watchdog bit (D15) that was addressed during the prior SOCR communication. If the OD15 is logic L, then the following three MSBs (OD14, OD13, OD12) will reflect the logic states of the IHS0, IHS1 and FSI pins respectively. If the OD15 bit is logic H, then the following three bits will reflect the logic states of the IHS2, IHS3 and WAKE pins respectively. The next twelve bits clocked out of SO following a low transition of the CSB pin will reflect the state of each output, with a logic H in any of the bits indicating that the respective output experienced a fault condition prior to the CSB transition. Any bits clocked out of the SO pin after the first sixteen will be representative of the initial message bits that were clocked into the SI pin since the CSB pin first transitioned to a logic L; this feature is useful for daisy chaining devices as well as message verification.

Following a CSB transition L to H, the device determines if the message was of a valid length (a valid message length is one that is a multiple of 16 bits) and if so, latches the data into the appropriate registers. At this time, the SO pin is tri-stated and the fault status register is now able to accept new fault status information.

Table 3 • SO OUTPUT BIT ASSIGNMENT

BIT SIG	SO MESSAGE BIT	MESSAGE DISCRIPTION
MSB	OD15	Reflects the state of the Watchdog bit from the previously clocked in message.
	OD14	If OD15 is logic L, then this bit will reflect the state of the direct input IHS0. If OD15 is logic H, then this bit will reflect the state of IHS2.
	OD13	If OD15 is logic L, then this bit will reflect the state of the direct input IHS1. If OD15 is logic H, then this bit will reflect the state of IHS3.
	OD12	If OD15 is logic L, then this bit will reflect the state of the input FSI. If OD15 is logic H, then this bit will reflect the state of the input WAKE.
	OD11	Reports the absence or presence of a fault on LS11
	OD10	Reports the absence or presence of a fault on LS10
	OD9	Reports the absence or presence of a fault on LS9
	OD8	Reports the absence or presence of a fault on LS8
	OD7	Reports the absence or presence of a fault on LS7
	OD6	Reports the absence or presence of a fault on LS6
	OD5	Reports the absence or presence of a fault on LS5
	OD4	Reports the absence or presence of a fault on LS4
	OD3	Reports the absence or presence of a fault on HS3
	OD2	Reports the absence or presence of a fault on HS2
	OD1	Reports the absence or presence of a fault on HS1
LSB	OD0	Reports the absence or presence of a fault on HS0

WATCHDOG AND FAILSAFE OPERATION

The watchdog is enabled and a timeout is started when the WAKE or RSTB transition from logic L to logic H. The WAKE input is capable of being pulled up to VPWR with a series limiting resistance that limits the internal clamp current. The timeout is a multiple of an internal oscillator . As long as the WDIN pin, or D15 of an incoming SPI message, is toggled within the minimum watchdog timeout, wdto (or a divided value configured during a WDCSCR message), then the device will operate normally. If the watchdog timeout occurs before the WD bit or WDIN pin is toggled, then the device will revert to a failsafe mode until the device is reinitialized (if the FSI pin is left disconnected). During failsafe mode, all outputs will be off except for HS0 and HS2, which will be driven on regardless of the state of the various direct inputs and modes. The device can be brought out of failsafe mode by transitioning the WAKE and RSTB pins from logic H to logic L. In the event that the WAKE pin was not transitioned to a logic H during normal operation and the watchdog times out, then the device can be brought out of failsafe by bringing the RSTB to a logic L. If the FSI pin is tied to GND, then the watchdog, and therefore failsafe operation, will be disabled (see TABLE 4).

Table 4 • FAILSAFE OPERATION

WAKE	RSTB	WDTO	HS0	HS2	OTHER LSx, HSx	COMMENTS
L	L	X	OFF	OFF	OFF	Device is in Sleep Mode
H	L	NO	OFF	OFF	OFF	All outputs are OFF, when RSTB transitions to logic H, device is in Default
H	L	YES	ON	ON	OFF	Failsafe. Device reset into Default mode by transitioning WAKE to logic L
L	H	NO	S	S	S	Device in Normal Operating mode
L	H	YES	ON	ON	OFF	Failsafe. Device reset into Default mode by transitioning RSTB to logic L
H	H	NO	S	S	S	Device in Normal Operating Mode
H	H	YES	ON	ON	OFF	Failsafe. Device reset into Default mode by transitioning RSTB & WAKE to logic L

X: don't care

S: state determined by SPI and/or Direct Input configurations.

Assumptions: Normal operating Voltage and Junction Temperatures, FSI pin floating.

DEFAULT MODE

The default mode describes the state of the device after first applying battery or a reset transition from logic L to H prior to SPI communication. In the default mode, all of the outputs will be off (assuming that the direct inputs ILS and IHSx, and the WAKE pins are at logic L). All of the specific pin functions will operate as though all of the addressable configuration register bits were set to logic L. This means, for example, that all of the LS outputs will be controllable by the ILS pin, and that all HS outputs will be controllable via their respective IHS pins. During the Default Mode, all of the HS drivers will default with the open load detection enabled. All of the low side drivers will default with the open load detection disabled. This mode allows limited control of the QHSOLSS with the direct inputs in the absence of a SPI.

FAULT LOGIC REQUIREMENTS

The QHSOLSS indicates all of the following faults as they occur: over-temperature fault, open-load fault, over-current fault and an over-voltage fault. All of these faults, with the exception of the over-voltage, are output specific. The over-voltage fault is a global fault. The over-current fault is only reported for the low side outputs.

The QHSOLSS low-side outputs incorporate an internal fault filter "Tdly(flt)".The fault timer filters noise and switching transients for over-current faults (when the output is on) and open load faults (when the output is off). All faults are latched and indicated

by a logic H for each output in the QHSOLSS status word (TABLE 3).). If the fault is removed, the status bit for the faulted output will be cleared by a rising edge on CSB.

The FLTB pin is driven to a logic L when a fault exists on any of the outputs. FLTB provided real time monitoring of the over-voltage fault. For the high side outputs, FLTB provides real time monitoring of the open-load and over-temp. For the low side outputs, the FLTB is latched to a logic L for open-load, over-temp, and over-current faults. The latch is cleared by toggling the state of the faulted output or by brinding RSTB low.

OVER-TEMPERATURE FAULT REQUIREMENTS

The QHSOLSS incorporates over-temperature detection and shutdown circuitry into each individual output structure. Over-temperature detection occurs when an output is in the on state. When an output is shutdown, due to an over-temperature condition, no other outputs is affected. The output experiencing the fault, is shutdown to protect itself from damage. A fault bit is loaded into the status register if the over-temp condition is removed, the fault bit is cleared upon the rising edge of CSB.
For the LS outputs, the faulted output is latched OFF during an over-temp condition. If the temperature falls below the recovery level, “TLIM(hyst)”, then the output can be turned back ON only after the output has first been commanded OFF either through the SPI or the ILS, depending on the logic configuration.
For the HS output(s), an over-temperature condition will result in the output(s) turning OFF until the temperature falls below the TLIM(hyst). This cycle will continue indefinitely until action is taken by the master to shut the output(s) OFF.

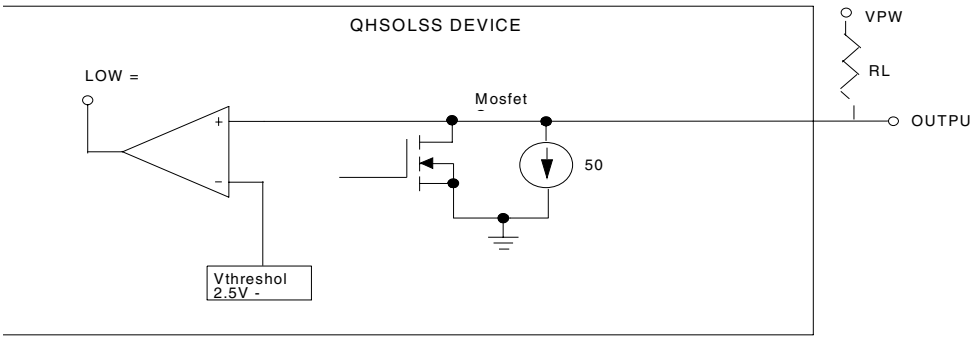
OVER-VOLTAGE FAULT REQUIREMENTS

The QHSOLSS do shutdown all outputs during an over-voltage condition on the VPWR pin. The outputs remain in the off state, until the over-voltage condition is removed. Fault status for all outputs is latched into the status register. Following an over-voltage condition, the next write cycle sent by the SO pin of the QHSOLSS is logic H on OD0-OD11, indicating all outputs have shutdown. If the over-voltage condition is removed, the status register can be cleared by a rising edge on CSB.

OPEN LOAD FAULT

The QHSOLSS incorporates open-load detection circuitry on every output. A HS or LS Output Open Load Fault is detected and reported as a fault condition when the corresponding output is disabled (OFF) if it was configured for open load detection by setting the appropriate bit to logic L (HS0-HS3), or logic H (LS4-LS11) in the OLFCR register.
The HS open load fault is detected and latched into the status register after the internal gate voltage is pulled low enough to turn off the output. If the open load fault is removed or if the faulted output is commanded ON, the status register can be cleared by a rising edge on CSB. Note that the device default state will enable the HS open load detection and disable the LS open load detection circuits, respectively.

Figure 3. LS Output OFF Open Load Detect



OVER-CURRENT FAULT REQUIREMENTS: LS OUTPUT

An over-current condition is defined as any current value greater than ILIM (500mA min value)for LS5, 7, 9, 11 and 800mA min value for LS4, 6, 8, 10). The status of the corresponding bit in the CLOCCR register determines whether a specific output will shutdown, or will continue to operate in an analog current limited mode, until either the over-current condition is removed or the thermal shutdown limit is reached (see Figure3). If the over-current shutdown mode is disabled, the fault reporting is disabled as well.

For the LS output of interest, if a D4-D11 bit was set to a logic H in the OLCR register, the over-current protection shutdown circuitry will be enabled for that output. When a low side output is commanded ON either from the SPI or the ILS pin, the drain of the low side driver will be monitored for a voltage greater than the Fault Detect Threshold (3V typ). If the drain voltage exceeds this threshold, a timer will start and the output will be turned off and a fault latched in the status register after the timeout expires. The faulted output can be retried only by commanding the output OFF and back ON either through the SPI or the ILS pin, depending on the logic configuration. If the fault is gone, the retried output will return to normal operation and the status register

can be cleared on a rising edge of CSB. If the fault remains, the retried output will latch off after the fault timer expires and the fault bit will remain set in the status register.

For the LS output of interest, if a D4-D11 bit was set to a logic L in the OLCR register, the output experiencing an over-current condition is not disabled until an over-temperature fault threshold has been reached. The specific output goes into an analog current limit mode of operation ILIM . The QHSOLSS uses over-temperature shutdown to protect all outputs in this mode of operation. If the over-current condition is removed before the output has reached its over-temperature limit, the output will function as if no fault has occurred.

Note that each pair of Low Side Drivers, LS4-5, LS6-7, LS8-9, and LS10 –11 consist of a 500mA and 800mA output. As shown in the device pinout, each of these pairs of outputs share ground bondwires. The bondwires are not rated to handle both outputs in current limit mode simultaneously.

OVER-CURRENT FAULT REQUIREMENTS: HS OUTPUT

For the HS output of interest, the output current is limited to one of four levels depending upon : the type of HS output, the amount of time that has elapsed since the output was switched on, and the state of the CLOCCR register. Assuming that bits D0-D3 of the CLOCCR register are at logic L, the current limit levels of the outputs will be initially at their peak levels as specified by the HSxxilimpk. After the HS output is switched on, the peak current timer will start. After a period of time Tpct, the current limit level will change to the sustain levels HSxxilimsus.

For the HS output of interest, if a D0-D3 bit of the CLOCCR is at logic H, then the assigned output will only current limit at the sustain level specified by HSxxilimsus.

Current is limited until the over temperature circuitry shuts OFF the device. The device will turn ON automatically when the temperature fails below the TLIM(hyst). This cycle continues indefinitely until action is taken by the master to shut the output(s) OFF.

REVERSE BATTERY REQUIREMENTS

The LS and HS outputs survive the application of reverse battery as low as –16V.

GROUND DISCONNECT PROTECTION

In the event that the QHSOLSS ground is disconnected from load ground, the device protects itself and safely turns off the outputs, regardless of the state of the output at the time of disconnection.

BATTERY DISCONNECT PROTECTION

In the event that the QHSOLSS is disconnected from Vpwr, the device protects itself and safely turn off the outputs, regardless of the state of the output at the time of disconnection.

UNDER-VOLTAGE SHUTDOWN REQUIREMENTS

All outputs turn off at some battery voltage below 6.0V, however, as long as the level stays above 5.0V, the internal logic states within the device are designed to be sustained. This ensures that when the battery level then rises above 6.0V, the device will return to the state that it was in prior to the excursion between 5.0V and 6.0V (assuming that there was no SPI communication or direct input changes during the event). If the battery voltage falls to a level below 5.0V, then the internal logic is reinitialized and the device is then in the Default state upon the return of levels in excess of 6.0V.

OUTPUT VOLTAGE CLAMPING

Each output has an internal clamp to provide protection and dissipate the energy stored in inductive loads. Each clamp independently limits the drain to source voltage to the range specified in the table “Power output characteristics”.

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