

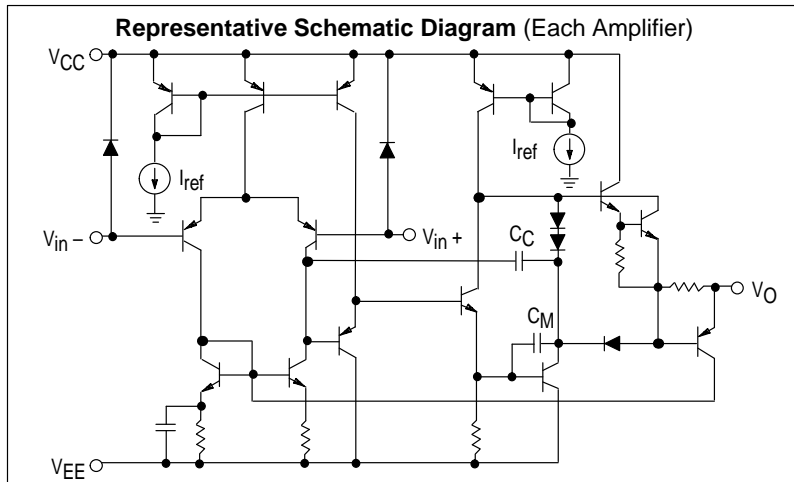


High Output Current Low Power, Low Noise Bipolar Operational Amplifiers

The MC33178/9 series is a family of high quality monolithic amplifiers employing Bipolar technology with innovative high performance concepts for quality audio and data signal processing applications. This device family incorporates the use of high frequency PNP input transistors to produce amplifiers exhibiting low input offset voltage, noise and distortion. In addition, the amplifier provides high output current drive capability while consuming only 420 μ A of drain current per amplifier. The NPN output stage used, exhibits no deadband crossover distortion, large output voltage swing, excellent phase and gain margins, low open-loop high frequency output impedance, symmetrical source and sink AC frequency performance.

The MC33178/9 family offers both dual and quad amplifier versions, tested over the vehicular temperature range, and are available in DIP and SOIC packages.

- 600 Ω Output Drive Capability
- Large Output Voltage Swing
- Low Offset Voltage: 0.15 mV (Mean)
- Low T.C. of Input Offset Voltage: 2.0 μ V/ $^{\circ}$ C
- Low Total Harmonic Distortion: 0.0024% (@ 1.0 kHz w/600 Ω Load)
- High Gain Bandwidth: 5.0 MHz
- High Slew Rate: 2.0 V/ μ s
- Dual Supply Operation: \pm 2.0 V to \pm 18 V
- ESD Clamps on the Inputs Increase Ruggedness without Affecting Device Performance



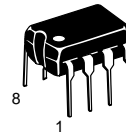
ORDERING INFORMATION

Op Amp Function	Fully Compensated	Operating Temperature Range	Package
Dual	MC33178D MC33178P	$T_A = -40^{\circ}$ to $+85^{\circ}$ C	SO-8 Plastic DIP
Quad	MC33179D MC33179P		SO-14 Plastic DIP

MC33178 MC33179

HIGH OUTPUT CURRENT LOW POWER, LOW NOISE OPERATIONAL AMPLIFIERS

DUAL

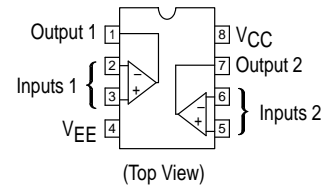


P SUFFIX
PLASTIC PACKAGE
CASE 626

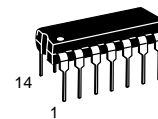


D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

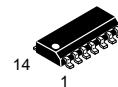
PIN CONNECTIONS



QUAD

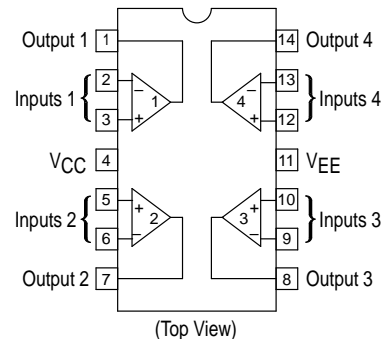


P SUFFIX
PLASTIC PACKAGE
CASE 646



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

PIN CONNECTIONS



MC33178 MC33179

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (V_{CC} to V_{EE})	V_S	+36	V
Input Differential Voltage Range	V_{IDR}	(Note 1)	V
Input Voltage Range	V_{IR}	(Note 1)	V
Output Short Circuit Duration (Note 2)	t_{SC}	Indefinite	sec
Maximum Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	-60 to +150	°C
Maximum Power Dissipation	P_D	(Note 2)	mW

- NOTES:** 1. Either or both input voltages should not exceed V_{CC} or V_{EE} .
 2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded. (See power dissipation performance characteristic, Figure 1.)

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15$ V, $V_{EE} = -15$ V, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Input Offset Voltage ($R_S = 50 \Omega$, $V_{CM} = 0$ V, $V_O = 0$ V) ($V_{CC} = +2.5$ V, $V_{EE} = -2.5$ V to $V_{CC} = +15$ V, $V_{EE} = -15$ V) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ$ to $+85^\circ\text{C}$	2	$ V_{IO} $	— —	0.15 —	3.0 4.0	mV
Average Temperature Coefficient of Input Offset Voltage ($R_S = 50 \Omega$, $V_{CM} = 0$ V, $V_O = 0$ V) $T_A = -40^\circ$ to $+85^\circ\text{C}$	2	$\Delta V_{IO}/\Delta T$	—	2.0	—	$\mu\text{V}/^\circ\text{C}$
Input Bias Current ($V_{CM} = 0$ V, $V_O = 0$ V) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ$ to $+85^\circ\text{C}$	3, 4	I_{IB}	— —	100 —	500 600	nA
Input Offset Current ($V_{CM} = 0$ V, $V_O = 0$ V) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ$ to $+85^\circ\text{C}$		$ I_{IO} $	— —	5.0 —	50 60	nA
Common Mode Input Voltage Range ($\Delta V_{IO} = 5.0$ mV, $V_O = 0$ V)	5	V_{ICR}	-13 —	-14 +14	— +13	V
Large Signal Voltage Gain ($V_O = -10$ V to $+10$ V, $R_L = 600 \Omega$) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ$ to $+85^\circ\text{C}$	6, 7	A_{VOL}	50 k 25 k	200 k —	— —	V/V
Output Voltage Swing ($V_{ID} = \pm 1.0$ V) ($V_{CC} = +15$ V, $V_{EE} = -15$ V) $R_L = 300 \Omega$ $R_L = 300 \Omega$ $R_L = 600 \Omega$ $R_L = 600 \Omega$ $R_L = 2.0$ k Ω $R_L = 2.0$ k Ω ($V_{CC} = +2.5$ V, $V_{EE} = -2.5$ V) $R_L = 600 \Omega$ $R_L = 600 \Omega$	8, 9, 10	V_{O+} V_{O-} V_{O+} V_{O-} V_{O+} V_{O-} V_{O+} V_{O-}	— — +12 — +13 — — —	+12 -12 +13.6 -13 +14 -13.8 1.6 -1.6	— — — -12 — -13 — -1.1	V
Common Mode Rejection ($V_{in} = \pm 13$ V)	11	CMR	80	110	—	dB
Power Supply Rejection $V_{CC}/V_{EE} = +15$ V/ -15 V, $+5.0$ V/ -15 V, $+15$ V/ -5.0 V	12	PSR	80	110	—	dB
Output Short Circuit Current ($V_{ID} = \pm 1.0$ V, Output to Ground) Source ($V_{CC} = 2.5$ V to 15 V) Sink ($V_{EE} = -2.5$ V to -15 V)	13, 14	I_{SC}	+50 -50	+80 -100	— —	mA
Power Supply Current ($V_O = 0$ V) ($V_{CC} = 2.5$ V, $V_{EE} = -2.5$ V to $V_{CC} = +15$ V, $V_{EE} = -15$ V) MC33178 (Dual) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ$ to $+85^\circ\text{C}$ MC33179 (Quad) $T_A = +25^\circ\text{C}$ $T_A = -40^\circ$ to $+85^\circ\text{C}$	15	I_D	— — — —	— — 1.7 —	1.4 1.6 2.4 2.6	mA

MC33178 MC33179

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = +15\text{ V}$, $V_{EE} = -15\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Slew Rate ($V_{in} = -10\text{ V}$ to $+10\text{ V}$, $R_L = 2.0\text{ k}\Omega$, $C_L = 100\text{ pF}$, $A_V = +1.0\text{ V}$)	16, 31	SR	1.2	2.0	—	V/ μs
Gain Bandwidth Product ($f = 100\text{ kHz}$)	17	GBW	2.5	5.0	—	MHz
AC Voltage Gain ($R_L = 600\ \Omega$, $V_O = 0\text{ V}$, $f = 20\text{ kHz}$)	18, 19	A_{VO}	—	50	—	dB
Unity Gain Frequency (Open-Loop) ($R_L = 600\ \Omega$, $C_L = 0\text{ pF}$)		f_U	—	3.0	—	MHz
Gain Margin ($R_L = 600\ \Omega$, $C_L = 0\text{ pF}$)	20, 22, 23	A_m	—	15	—	dB
Phase Margin ($R_L = 600\ \Omega$, $C_L = 0\text{ pF}$)	21, 22, 23	ϕ_m	—	60	—	Degrees
Channel Separation ($f = 100\text{ Hz}$ to 20 kHz)	24	CS	—	-120	—	dB
Power Bandwidth ($V_O = 20\text{ V}_{pp}$, $R_L = 600\ \Omega$, $\text{THD} \leq 1.0\%$)		BW_p	—	32	—	kHz
Distortion ($R_L = 600\ \Omega$, $V_O = 2.0\text{ V}_{pp}$, $A_V = +1.0\text{ V}$) ($f = 1.0\text{ kHz}$) ($f = 10\text{ kHz}$) ($f = 20\text{ kHz}$)	25	THD	—	0.0024 0.014 0.024	—	%
Open Loop Output Impedance ($V_O = 0\text{ V}$, $f = 3.0\text{ MHz}$, $A_V = 10\text{ V}$)	26	$ Z_O $	—	150	—	Ω
Differential Input Resistance ($V_{CM} = 0\text{ V}$)		R_{in}	—	200	—	k Ω
Differential Input Capacitance ($V_{CM} = 0\text{ V}$)		C_{in}	—	10	—	pF
Equivalent Input Noise Voltage ($R_S = 100\ \Omega$) $f = 10\text{ Hz}$ $f = 1.0\text{ kHz}$	27	e_n	—	8.0 7.5	—	nV/ $\sqrt{\text{Hz}}$
Equivalent Input Noise Current $f = 10\text{ Hz}$ $f = 1.0\text{ kHz}$	28	i_n	—	0.33 0.15	—	pA/ $\sqrt{\text{Hz}}$

Figure 1. Maximum Power Dissipation versus Temperature

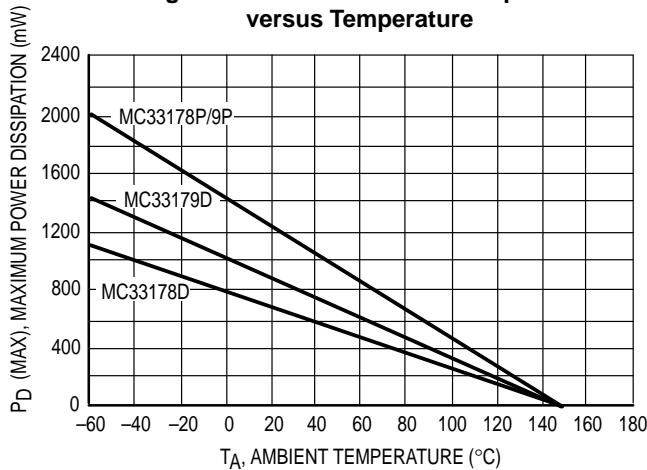


Figure 2. Input Offset Voltage versus Temperature for 3 Typical Units

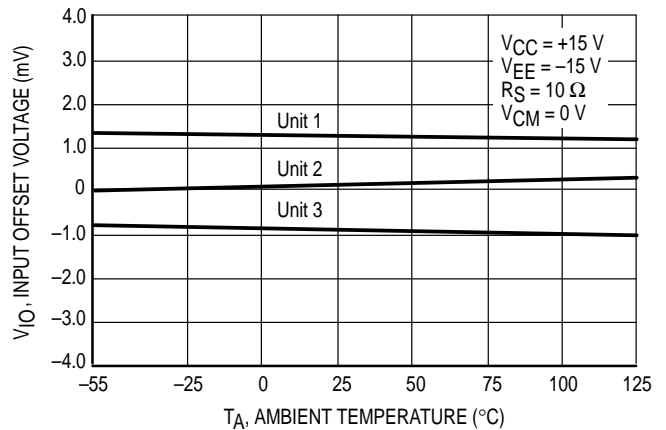


Figure 3. Input Bias Current versus Common Mode Voltage

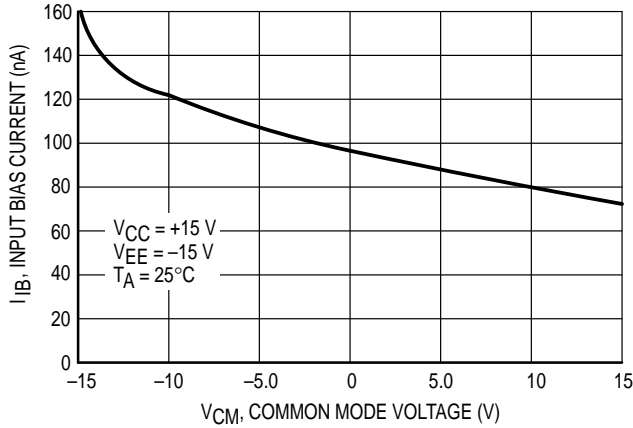


Figure 4. Input Bias Current versus Temperature

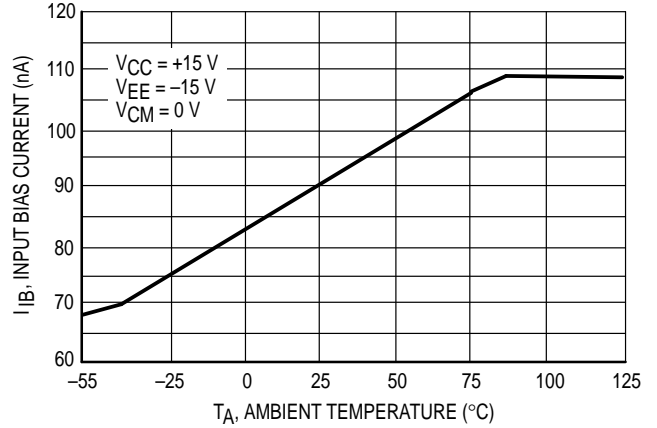


Figure 5. Input Common Mode Voltage Range versus Temperature

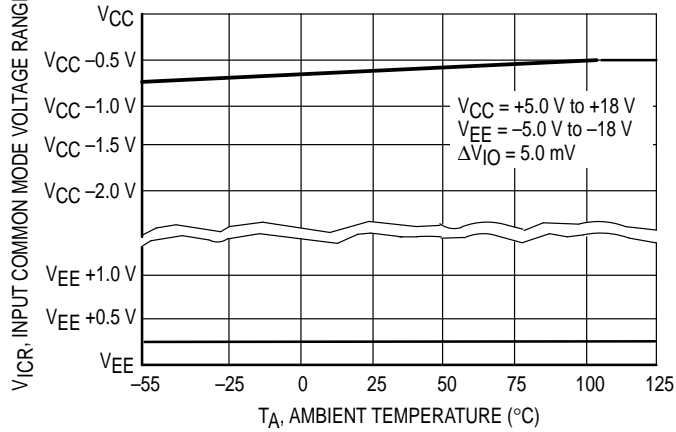


Figure 6. Open Loop Voltage Gain versus Temperature

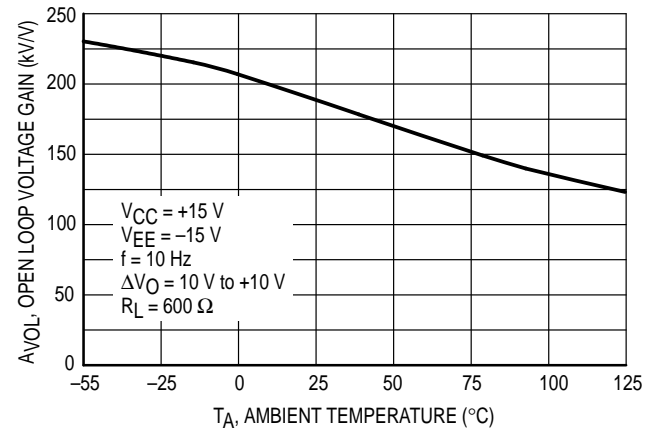


Figure 7. Voltage Gain and Phase versus Frequency

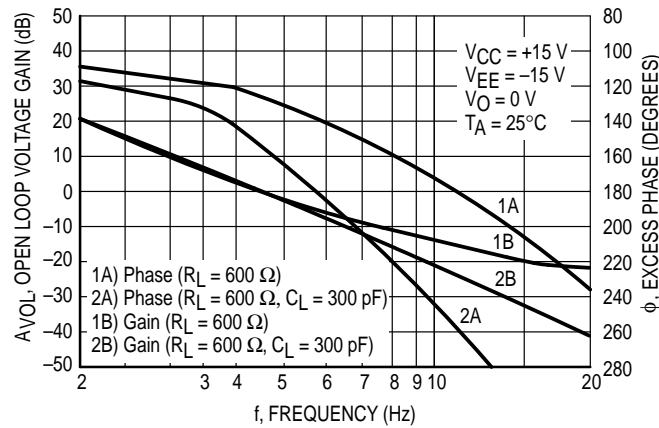


Figure 8. Output Voltage Swing versus Supply Voltage

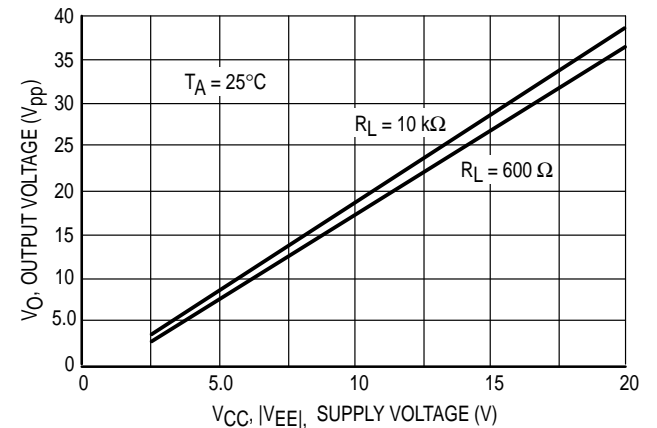


Figure 9. Output Saturation Voltage versus Load Current

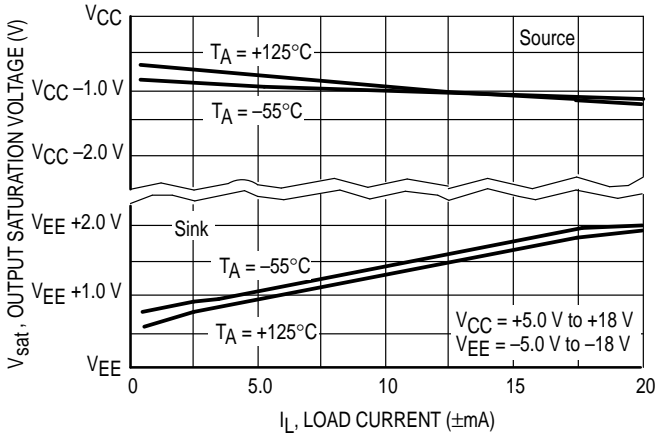


Figure 10. Output Voltage versus Frequency

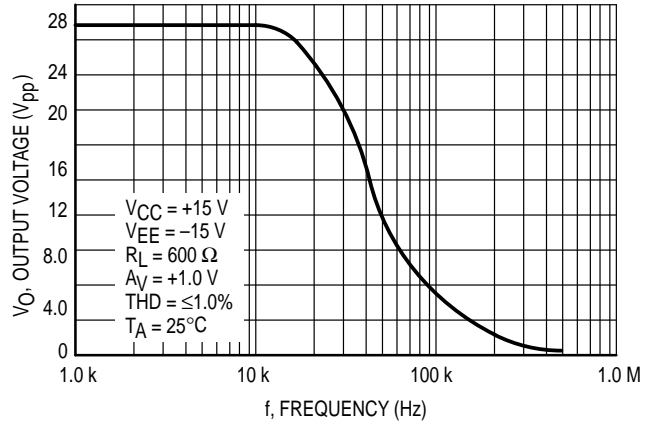


Figure 11. Common Mode Rejection versus Frequency Over Temperature

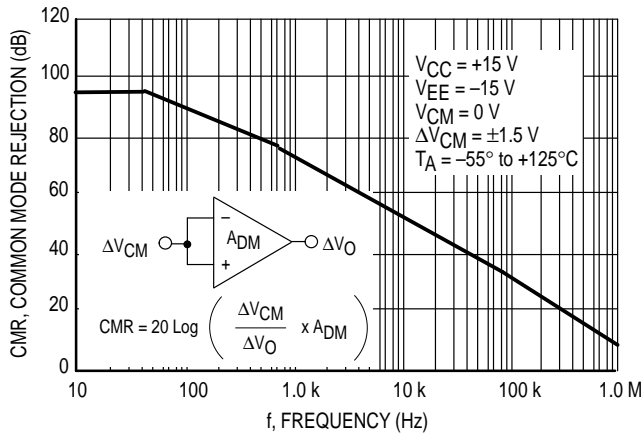


Figure 12. Power Supply Rejection versus Frequency Over Temperature

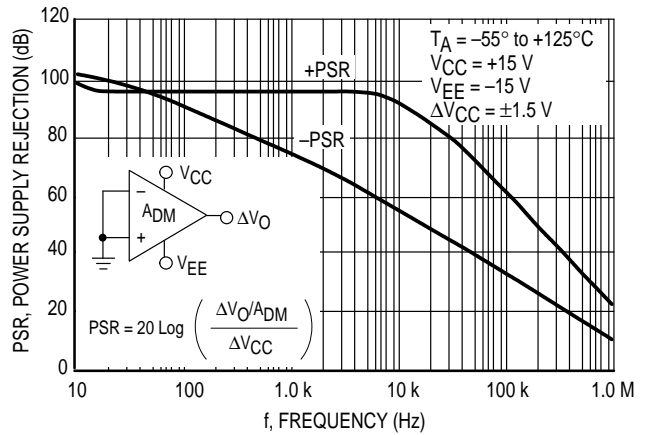


Figure 13. Output Short Circuit Current versus Output Voltage

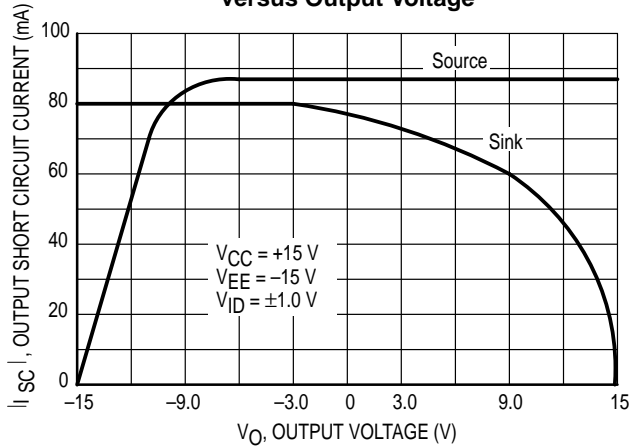


Figure 14. Output Short Circuit Current versus Temperature

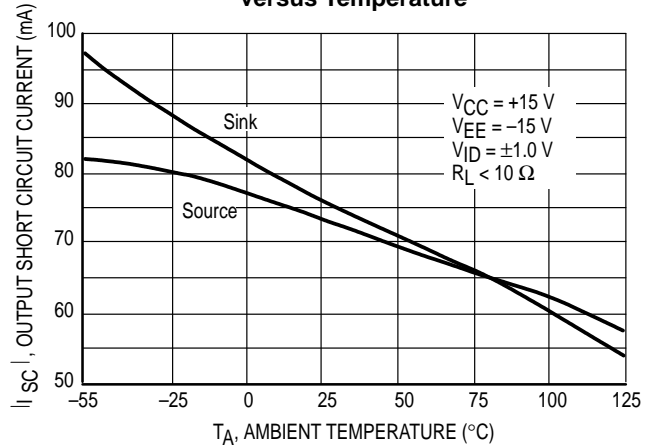


Figure 15. Supply Current versus Supply Voltage with No Load

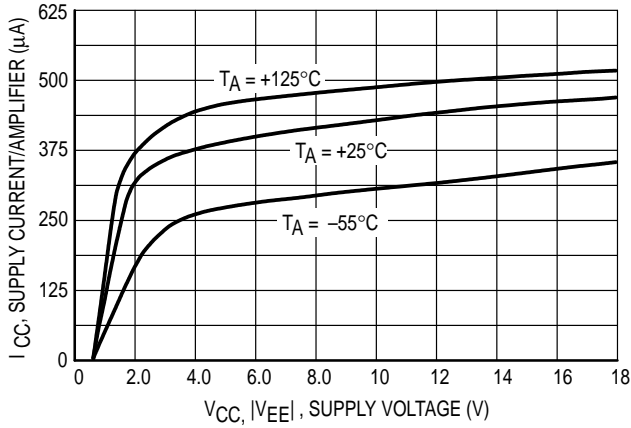


Figure 16. Normalized Slew Rate versus Temperature

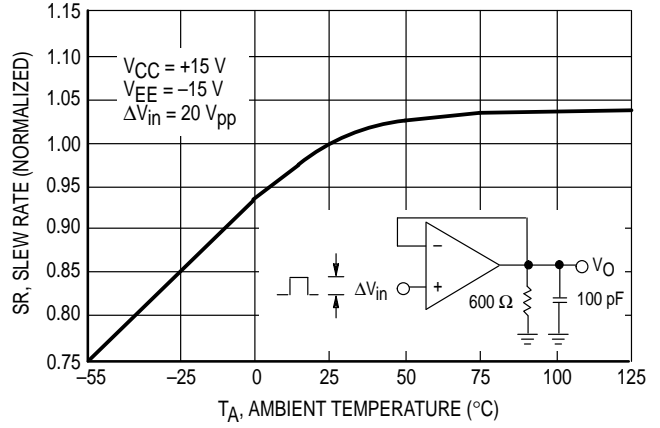


Figure 17. Gain Bandwidth Product versus Temperature

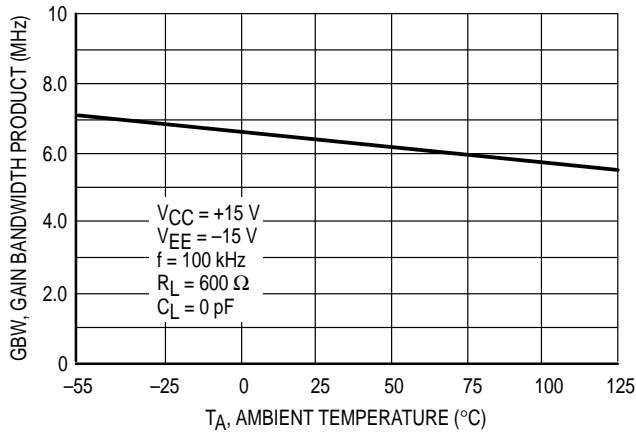


Figure 18. Voltage Gain and Phase versus Frequency

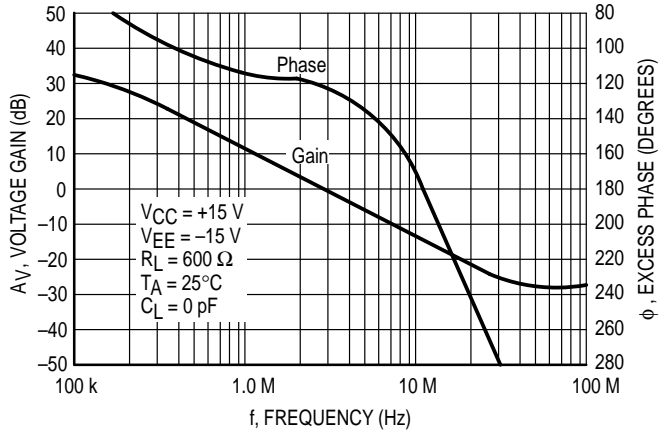


Figure 19. Voltage Gain and Phase versus Frequency

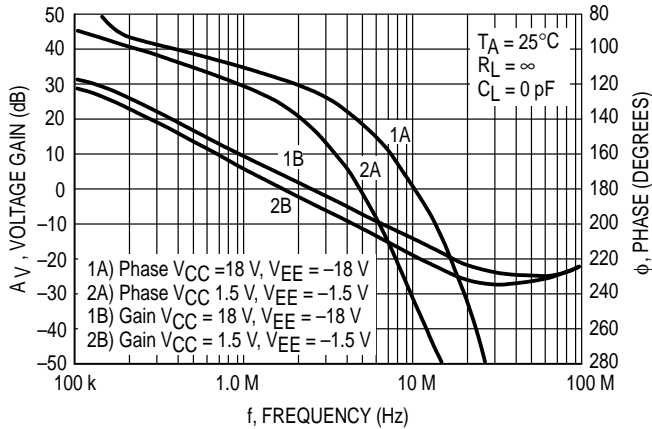


Figure 20. Open Loop Gain Margin versus Temperature

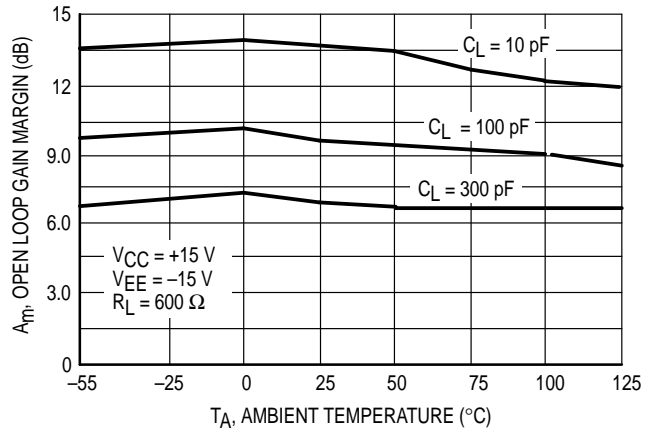


Figure 21. Phase Margin versus Temperature

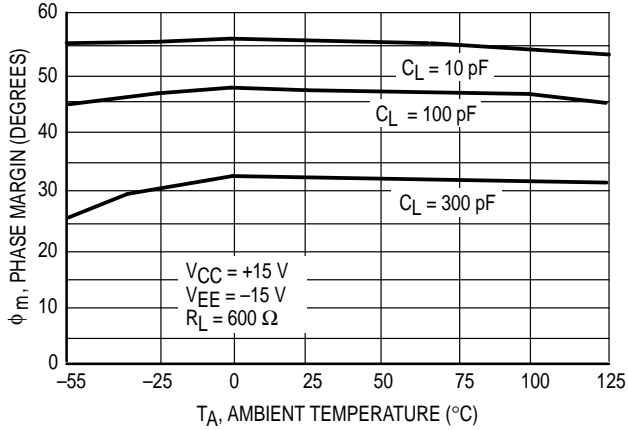


Figure 22. Phase Margin and Gain Margin versus Differential Source Resistance

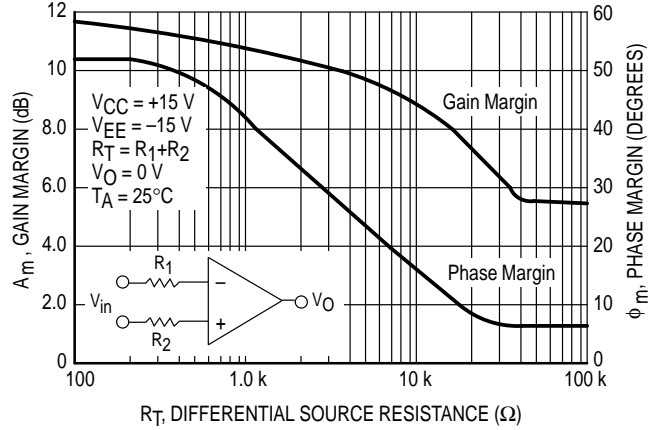


Figure 23. Open Loop Gain Margin and Phase Margin versus Output Load Capacitance

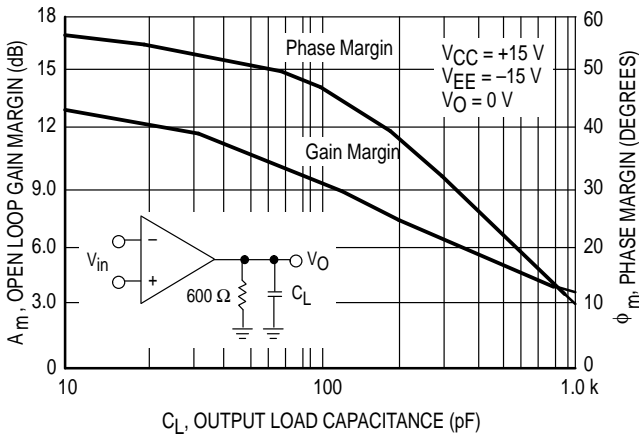


Figure 24. Channel Separation versus Frequency

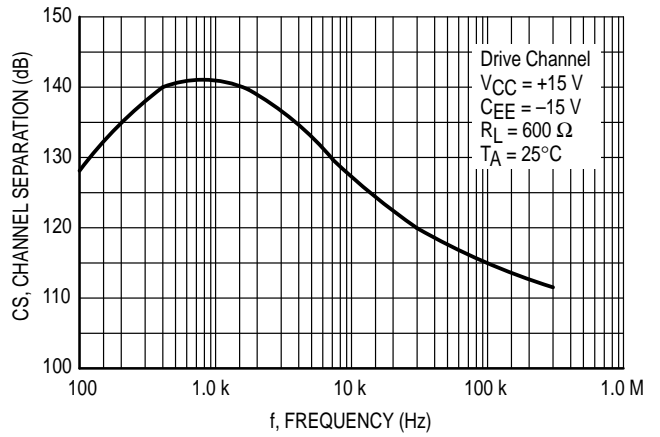


Figure 25. Total Harmonic Distortion versus Frequency

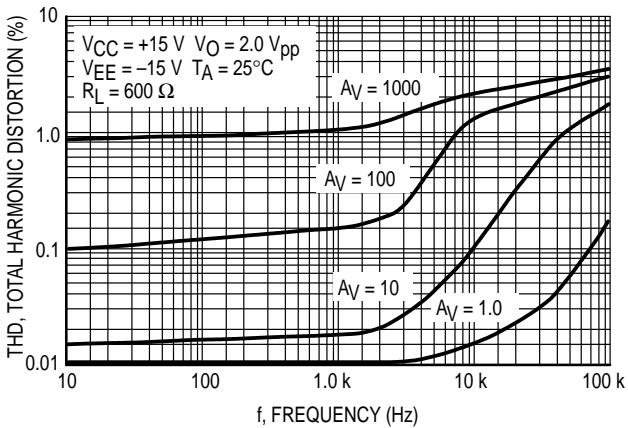


Figure 26. Output Impedance versus Frequency

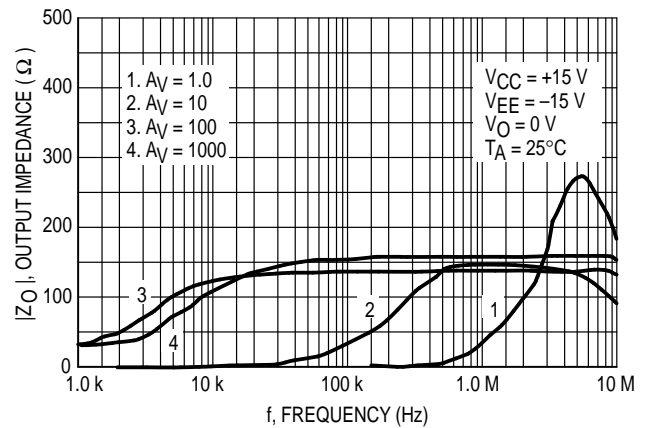


Figure 27. Input Referred Noise Voltage versus Frequency

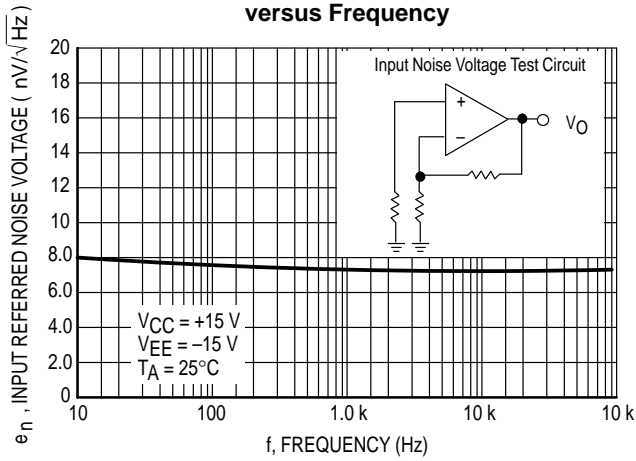


Figure 28. Input Referred Noise Current versus Frequency

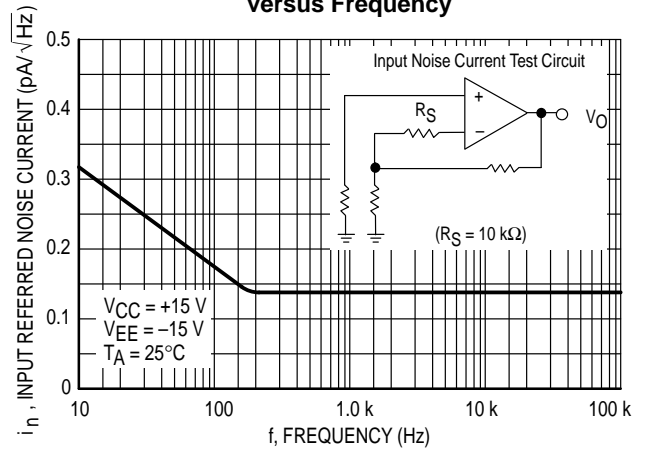


Figure 29. Percent Overshoot versus Load Capacitance

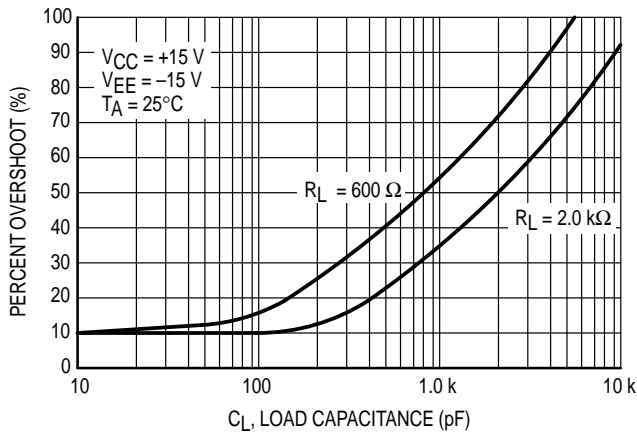


Figure 30. Noninverting Amplifier Slew Rate

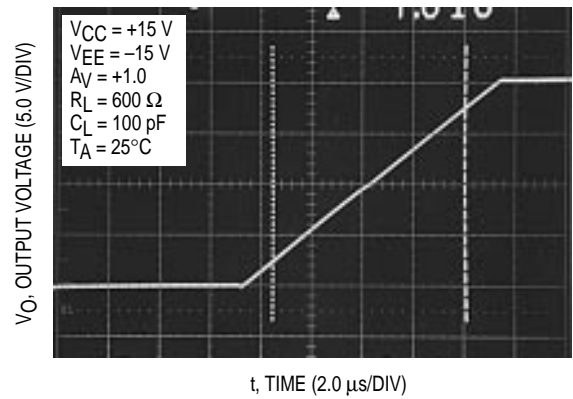


Figure 31. Small Signal Transient Response

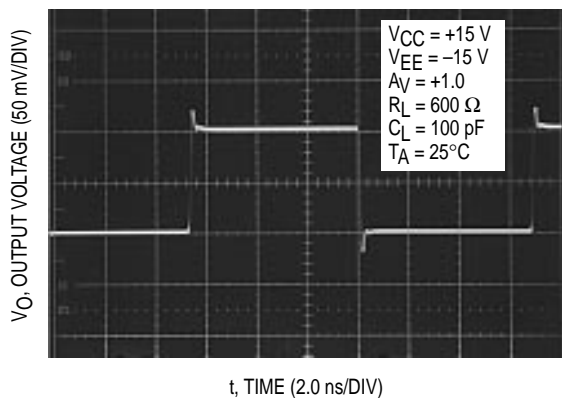


Figure 32. Large Signal Transient Response

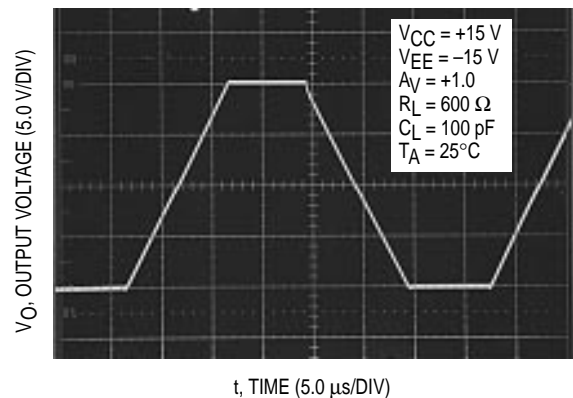
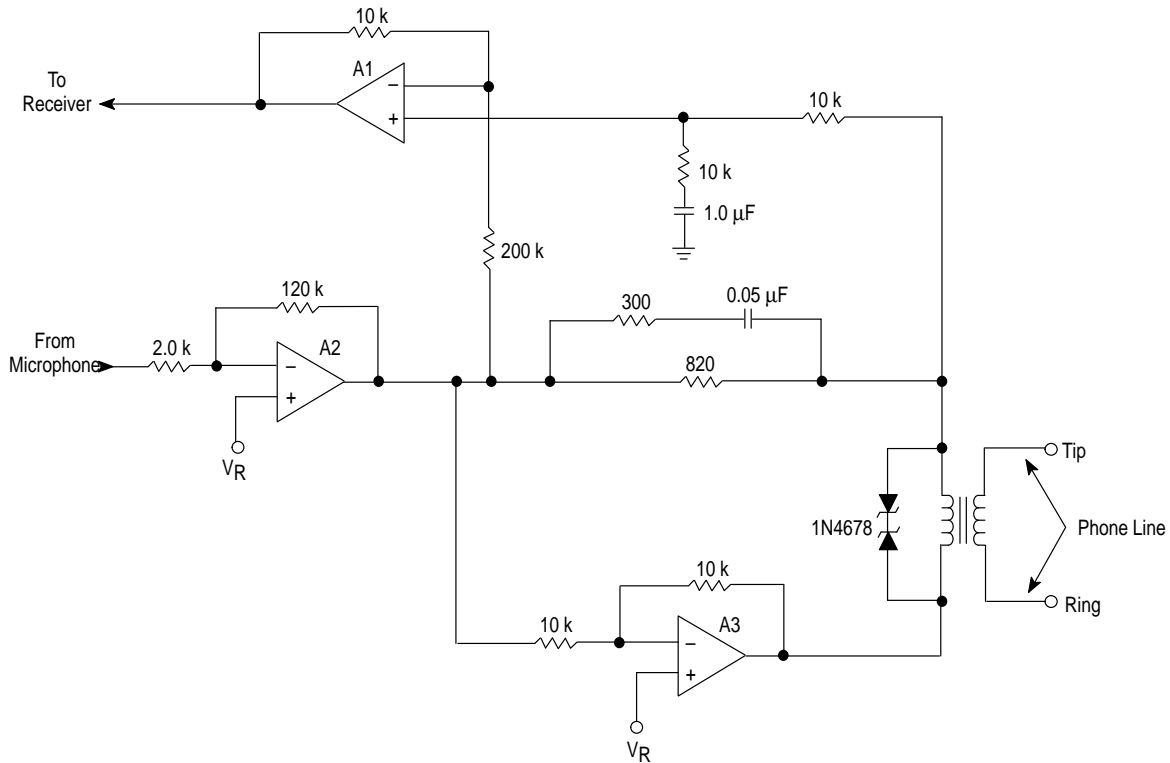


Figure 33. Telephone Line Interface Circuit



APPLICATION INFORMATION

This unique device uses a boosted output stage to combine a high output current with a drain current lower than similar bipolar input op amps. Its 60° phase margin and 15 dB gain margin ensure stability with up to 1000 pF of load capacitance (see Figure 23). The ability to drive a minimum 600 Ω load makes it particularly suitable for telecom applications. Note that in the sample circuit in Figure 33 both A2 and A3 are driving equivalent loads of approximately 600 Ω.

The low input offset voltage and moderately high slew rate and gain bandwidth product make it attractive for a variety of other applications. For example, although it is not single supply (the common mode input range does not include ground), it is specified at +5.0 V with a typical common mode rejection of 110 dB. This makes it an excellent choice for use with digital circuits. The high common mode rejection, which is stable over temperature, coupled with a low noise figure and low distortion, is an ideal op amp for audio circuits.

The output stage of the op amp is current limited and therefore has a certain amount of protection in the event of a short circuit. However, because of its high current output, it is especially important not to allow the device to exceed the maximum junction temperature, particularly with the MC33179 (quad op amp). Shorting more than one amplifier

could easily exceed the junction temperature to the extent of causing permanent damage.

Stability

As usual with most high frequency amplifiers, proper lead dress, component placement, and PC board layout should be exercised for optimum frequency performance. For example, long unshielded input or output leads may result in unwanted input/output coupling. In order to preserve the relatively low input capacitance associated with these amplifiers, resistors connected to the inputs should be immediately adjacent to the input pin to minimize additional stray input capacitance. This not only minimizes the input pole frequency for optimum frequency response, but also minimizes extraneous "pick up" at this node. Supplying decoupling with adequate capacitance immediately adjacent to the supply pin is also important, particularly over temperature, since many types of decoupling capacitors exhibit great impedance changes over temperature.

Additional stability problems can be caused by high load capacitances and/or a high source resistance. Simple compensation schemes can be used to alleviate these effects.

If a high source of resistance is used ($R_1 > 1.0 \text{ k}\Omega$), a compensation capacitor equal to or greater than the input capacitance of the op amp (10 pF) placed across the feedback resistor (see Figure 34) can be used to neutralize that pole and prevent outer loop oscillation. Since the closed loop transient response will be a function of that capacitance, it is important to choose the optimum value for that capacitor. This can be determined by the following Equation:

$$C_C = (1 + [R_1/R_2])^2 \times C_L (Z_O/R_2) \quad (1)$$

where: Z_O is the output impedance of the op amp.

For moderately high capacitive loads ($500 \text{ pF} < C_L < 1500 \text{ pF}$) the addition of a compensation resistor on the order of 20Ω between the output and the feedback loop will help to decrease miller loop oscillation (see Figure 35). For high capacitive loads ($C_L > 1500 \text{ pF}$), a combined compensation scheme should be used (see Figure 36). Both the compensation resistor and the compensation capacitor affect the transient response and can be calculated for optimum performance. The value of C_C can be calculated using Equation (1). The Equation to calculate R_C is as follows:

$$R_C = Z_O \times R_1/R_2 \quad (2)$$

Figure 34. Compensation for High Source Impedance

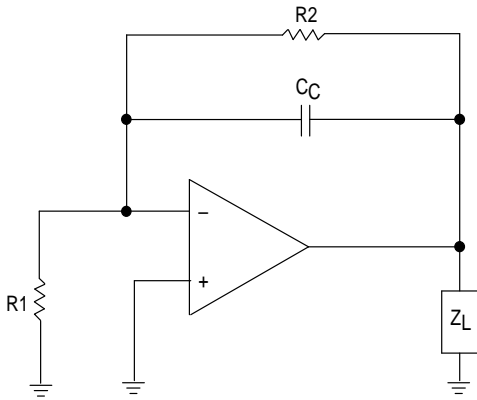


Figure 35. Compensation Circuit for Moderate Capacitive Loads

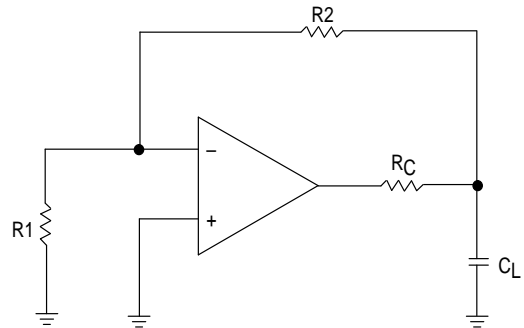
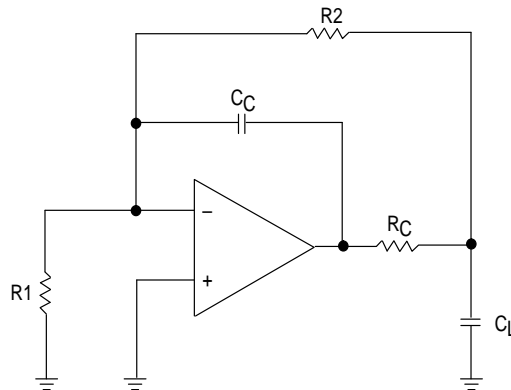


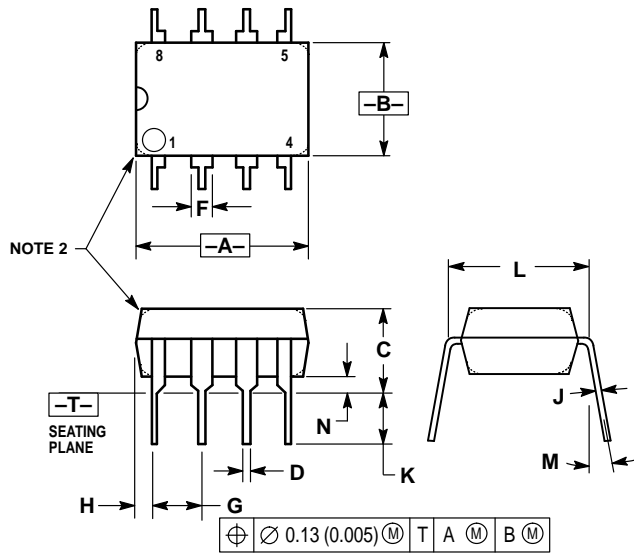
Figure 36. Compensation Circuit for High Capacitive Loads



MC33178 MC33179

OUTLINE DIMENSIONS

P SUFFIX PLASTIC PACKAGE CASE 626-05 ISSUE K

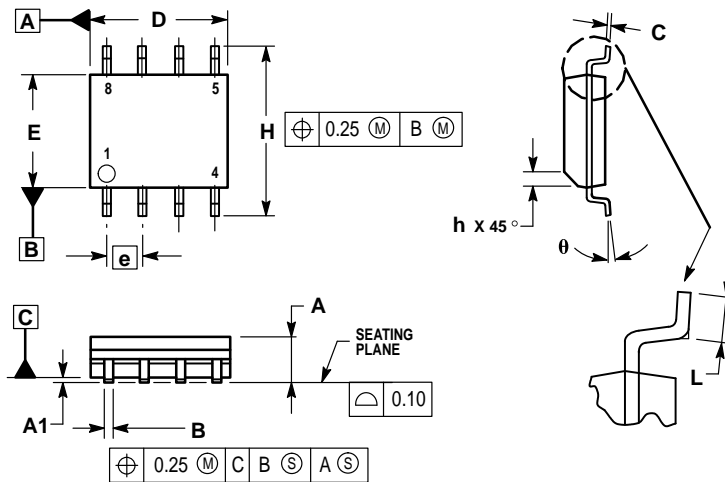


NOTES:

1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	10°		10°	
N	0.76	1.01	0.030	0.040

D SUFFIX PLASTIC PACKAGE CASE 751-05 (SO-8) ISSUE R



NOTES:

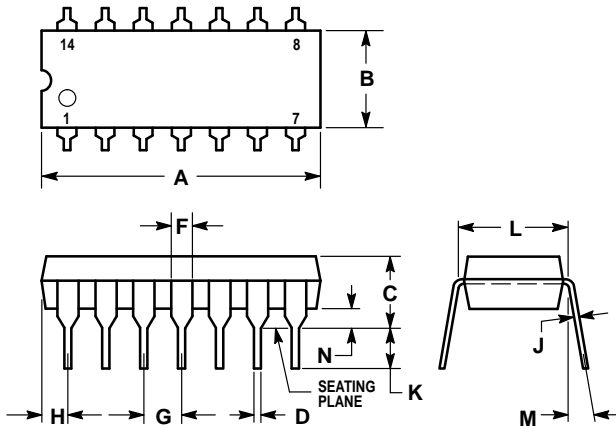
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0° 7°	

MC33178 MC33179

OUTLINE DIMENSIONS

P SUFFIX PLASTIC PACKAGE CASE 646-06 ISSUE L

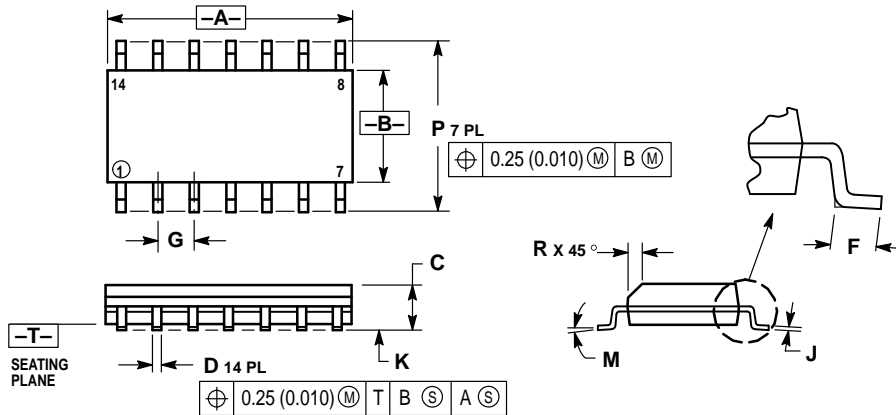


NOTES:

- LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSION B DOES NOT INCLUDE MOLD FLASH.
- ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

D SUFFIX PLASTIC PACKAGE CASE 751A-03 (SO-14) ISSUE F



NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
- MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
- DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

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