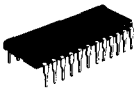
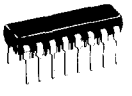
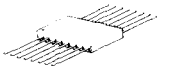
MC10,100/10,200 Series (-30 to +85°C)
MC10,500/10,600 Series (-55 to +125°C)

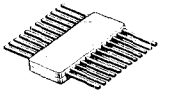
MECL 10,000 has an excellent speed-power product, has relatively slow rise and fall times, and transmission-line drive capability. The combination of versatile logic functions and the 2.0 ns propagation delay make MECL 10,000 a versatile family for data handling and processing systems.

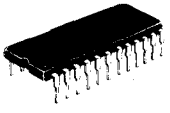
Circuit design with MECL 10,000 is unusually convenient. The differential amplifier input and emitter-follower output permit high fanout, the wired-OR option, and complementary outputs. MECL III is directly compatible with MECL 10,000, and can be used to extend the speed capability of the MECL 10,000 series.

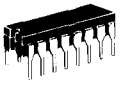

L SUFFIX
CERAMIC PACKAGE
CASE 623

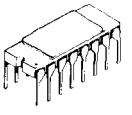

P SUFFIX
PLASTIC PACKAGE
CASE 648


F SUFFIX
CERAMIC PACKAGE
CASE 650


F SUFFIX
CERAMIC PACKAGE
CASE 652


P SUFFIX
PLASTIC PACKAGE
CASE 649


L SUFFIX
CERAMIC PACKAGE
CASE 620


AL SUFFIX
CERAMIC PACKAGE
CASE 690

FUNCTIONS AND CHARACTERISTICS (V_{CC} = 0, V_{EE} = -5.2 V, T_A = 25°C)

Function	Type① -30 to +85°C	Type① -55 to +125°C	Propagation Delay ns typ	Power Dissipation mW typ/pkg*	Case
Quad 2-Input NOR Gate With Strobe	MC10100	–	2.0	100	620
Quad OR/NOR Gate	MC10101	MC10501	2.0	100	620,648,650
Quad 2-Input NOR Gate	MC10102	MC10502	2.0	100	620,648,650
Quad 2-Input OR Gate	MC10103	–	2.0	100	620
Quad 2-Input AND Gate	MC10104	MC10504	2.7	140	620,648,650
Triple 2-3-2-Input OR/NOR Gate	MC10105	MC10505	2.0	90	620,648,650
Triple 4-3-3-Input NOR Gate	MC10106	MC10506	2.0	90	620,648,650
Triple 2-Input Exclusive OR/Exclusive NOR	MC10107	MC10507	2.5	110	620,648,650
Dual 4-5-Input OR/NOR Gate	MC10109	MC10509	2.0	60	620,648,650
Dual 3-Input 3-Output OR Gate	MC10110	–	2.4	160	620,648
Dual 3-Input 3-Output NOR Gate	MC10111	–	2.4	160	620,648
Quad Exclusive OR Gate	MC10113	–	2.5	175	620
Triple Line Receiver	MC10114	MC10514	2.4	145	620,648,650
Quad Line Receiver	MC10115	MC10515	2.0	110	620,648,650
Triple Line Receiver	MC10116	MC10516	2.0	85	620,648,650
Dual 2-Wide 2-3-Input OR-AND/OR-AND-INVERT Gate	MC10117	MC10517	2.3	100	620,648,650
Dual 2-Wide 3-Input OR-AND Gate	MC10118	MC10518	2.3	100	620,648,650
4-Wide 4-3-3-3-Input OR-AND Gate	MC10119	MC10519	2.3	100	620,648,650
4-Wide OR-AND/OR-AND-INVERT Gate	MC10121	MC10521	2.3	100	620,648,650
Triple 4-3-3-Input Bus Driver	MC10123	–	3.0	310	620
Quad MTTL to MECL Translator	MC10124	MC10524	3.5	380	620,648,650
Quad MECL to MTTL Translator	MC10125	MC10525	4.5	380	620,648,650
Dual MECL to MOS Translator	MC10127	–	–	–	620
Bus Driver	MC10128	–	12.0	700	620
Quad Bus Receiver	MC10129	–	10.0	750	620
Dual Latch	MC10130	MC10530	2.5	155	620,648,650
Dual Type D Master-Slave Flip-Flop	MC10131	MC10531	f = 160 MHz	235	620,648,650
Dual Multiplexer With Latch and Common Reset	MC10132	–	3.0	225	620,648
Quad Latch	MC10133	MC10533	4.0	310	620,648,650
Multiplexer with Latch	MC10134	–	3.0	225	620,648
Dual J-K Master-Slave Flip-Flop	MC10135	MC10535	f = 140 MHz	280	620,648,650
Universal Hexadecimal Counter	MC10136	MC10536	f = 150 MHz	625	620,650

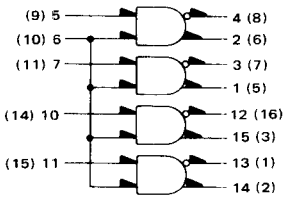
① L suffix denotes Dual In-Line Ceramic Package, P suffix denotes Dual In-Line Plastic Package, F suffix denotes flat package (i.e., MC10100L = Ceramic Dual In-Line Package, MC10100P = Plastic Dual In-Line Package and MC10500F = Ceramic Flat Package.)

*External Load Power not included.

2

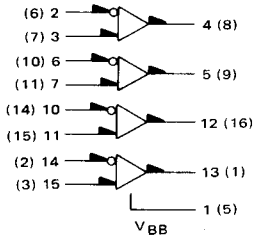
TRANSLATORS

MC10124
MC10525
Quad MTTL to MECL Translator



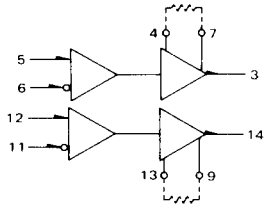
P_D = 380 mW typ/pkg (No Load)
t_{pd} = 3.5 ns typ

MC10125
MC10525
Quad MECL to MTTL Translator



P_D = 380 mW typ/pkg (No Load)
t_{pd} = 4.5 ns typ (50% to +1.5 Vdc out)

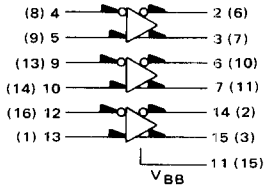
MC10127
Dual MECL to MOS Translator



V_{CC} = Gnd = Pins 1, 2, 15, 16
V_{EE} = Pin 8
V_{SS} = Pins 7, 9

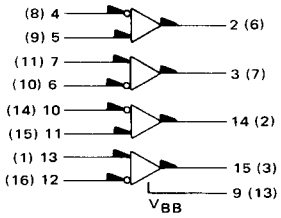
RECEIVERS

MC10114
MC10514
Triple Line Receiver



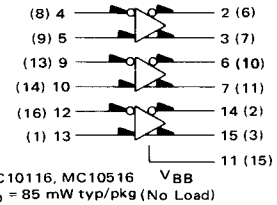
t_{pd} = 2.4 ns typ (Single Ended Input)
t_{pd} = 2.0 ns typ (Differential Input)
P_D = 145 mW typ/pkg (No Load)

MC10115
MC10515
Quad Line Receiver



P_D = 110 mW typ/pkg (No Load)
t_{pd} = 2.0 ns typ

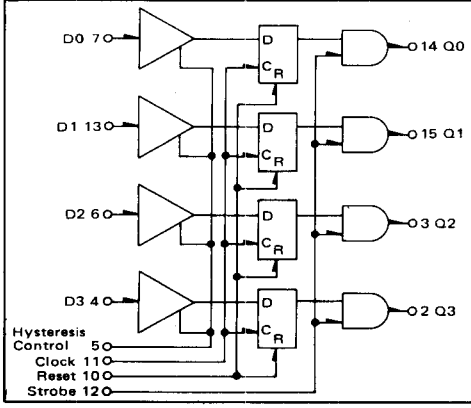
MC10116, MC10516
MC10216, MC10616
Triple Line Receiver



MC10116, MC10516
P_D = 85 mW typ/pkg (No Load)
t_{pd} = 2.0 ns typ

MC10216, MC10616
P_D = 100 mW typ/pkg (No Load)
t_{pd} = 1.8 ns typ

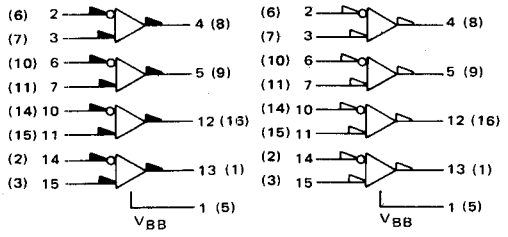
MC10129
Quad Bus Receiver



P_D = 750 mW typ/pkg (No Load)
t_{pd} = 10 ns typ

MC10525

Advance Information



Numbers at end of terminals denote pin numbers for L package (Case 620).

Numbers in parenthesis denote pin numbers for F package (Case 650).

CASE	V_{CC}	V_{EE}
620	Pin 9	Pin 8
650	Pin 13	Pin 12

The MC10525 is a quad translator for interfacing data and control signals between the MECL section and saturated logic sections of digital systems. The MC10525 incorporates differential inputs and Schottky TTL "totem pole" outputs. Differential inputs allow for use as an inverting/non-inverting translator or as a differential line receiver. The V_{BB} reference voltage is available for use in single-ended input biasing. The outputs of the MC10525 go to a low logic level whenever the inputs are left floating.

Power supply requirements are ground, +5.0 Volts and -5.2 Volts. Propagation delay of the MC10525 is typically 4.5 ns. The MC10525 has fanout of 6 MTTL loads. The dc levels are MECL 10,000 in and Schottky TTL, or MTTL out. This device has an input common mode noise rejection of ±1.0 Volt.

An advantage of this device is that MECL level information can be received, via balanced twisted pair lines, in the MTTL equipment. This isolates the MECL logic from the noisy MTTL environment. This device is useful in computers, instrumentation, peripheral controllers, test equipment and digital communications systems.

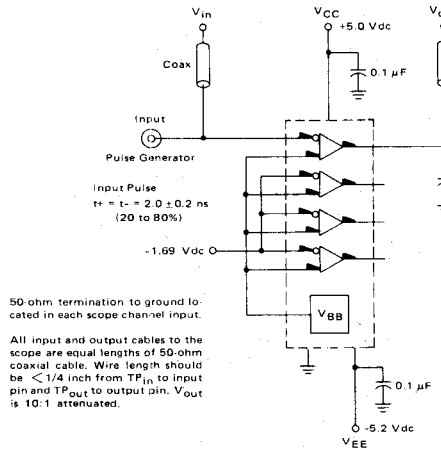
P_D = 380 mW typ/pkg (No Load)

t_{pd} = 4.5 ns typ (50% to +1.5 Vdc out)

Output Rise, Fall Times;
2.5 ns typ (20% to 80%)

V_{CCmax} = +7.00 Vdc

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



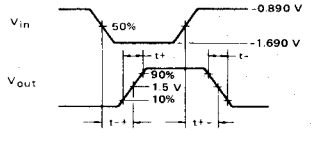
50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <1/4 inch from TP_{in} to input pin and TP_{out} to output pin. V_{out} is 10:1 attenuated.

C_L = 25 pF, including test fixture

One input from each gate must be tied to V_{BB} during testing.

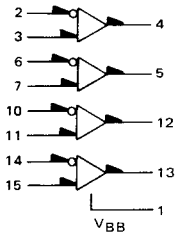
PROPAGATION DELAY

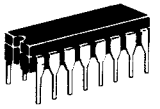


This is advance information and specifications are subject to change without notice.
See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Test procedures are shown for only one input, or for one set of input conditions. Other inputs or outputs are tested in the same manner.





L SUFFIX
CERAMIC PACKAGE
CASE 620

@ Test Temperature	$V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{IHH}	V_{ILH}	V_{IHL}	V_{ILL}	V_{BB}	V_{CC}	V_{EE}
	TEST VOLTAGE VALUES (Volts)										
-55°C	-0.880	-1.920	-1.255	-1.510	+0.170	-0.920	-1.830	-2.920	From Pin 1	+5.0	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	+0.280	-0.850	-1.720	-2.850		+5.0	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	+0.420	-0.820	-1.580	-2.820		+5.0	-5.2

Characteristic	Symbol	Pin Under Test	MC10525L Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{IHH}	V_{ILH}	V_{IHL}	V_{ILL}	V_{BB}	V_{CC}	V_{EE}	Gnd	Output Condition
Negative Power Supply Drain Current	I_E	8	–	–	–	–	40	–	–	mAdc	–	–	–	–	–	–	–	–	3,7,11,15	9	8	16	–
Positive Power Supply Drain Current	I_{CCH}	9	–	–	–	–	52	–	–	mAdc	2,6,10,14	–	–	–	–	–	–	–	3,7,11,15	9	8	16	–
	I_{CCL}	9	–	–	–	–	39	–	–	mAdc	–	–	–	–	–	–	–	–	3,7,11,15	9	8	16	–
Input Current	$I_{in\ H}$ ①	2	–	–	–	–	115	–	–	µAdc	2,6,10,14	–	–	–	–	–	–	–	3,7,11,15	9	8	16	–
		3	–	–	–	–	115	–	–	µAdc	3,7,11,15	–	–	–	–	–	–	–	2,6,10,14	9	8	16	–
Input Leakage Current	I_{CBO} ②	2	–	–	–	–	1.0	–	–	µAdc	–	–	–	–	–	–	–	–	3,7,11,15	9	2,6,8,10,14	16	–
		3	–	–	–	–	1.0	–	–	µAdc	–	–	–	–	–	–	–	–	2,6,10,14	9	3,7,8,11,15	16	–
Short-Circuit Current	I_{OS}	4	–	–	40	–	100	–	–	mA	–	2,6,10,14	–	–	–	–	–	–	3,7,11,15	9	8	4,16	
High Output Voltage	V_{OH} ③	4	2.5	–	2.5	–	–	2.5	–	Vdc	–	2,6,10,14	–	–	–	–	–	–	3,7,11,15	9	8	16	-2.0 mA
Low Output Voltage	V_{OL}	4	–	0.5	–	–	0.5	–	0.5	Vdc	2,6,10,14	–	–	–	–	–	–	–	3,7,11,15	9	8	16	12.0 mA
High Threshold Voltage	V_{OHA}	4	2.5	–	2.5	–	–	2.5	–	Vdc	–	6,10,14	–	2	–	–	–	–	3,7,11,15	9	8	16	-2.0 mA
Low Threshold Voltage	V_{OLA}	4	–	0.5	–	–	0.5	–	0.5	Vdc	6,10,14	–	2	–	–	–	–	–	3,7,11,15	9	8	16	12.0 mA
Indeterminate Input Protection Tests	V_{OLS1}	4	–	0.5	–	–	0.5	–	0.5	Vdc	–	–	–	–	–	–	–	–	–	9	2,3,6,7,8, 10,11,14,15	16	12.0 mA
	V_{OLS2}	4	–	0.5	–	–	0.5	–	0.5	Vdc	–	–	–	–	–	–	–	–	–	9	8	16	12.0 mA
Reference Voltage	V_{BB}	1	-1.440	-1.320	-1.350	–	-1.230	-1.240	-1.120	Vdc	–	–	–	–	–	–	–	–	3,7,11,15	–	–	–	–
Common Mode Rejection Tests	V_{OH}	4	2.5	–	2.5	–	–	2.5	–	Vdc	–	–	–	–	3	2	–	–	–	9	8	16	-2.0 mA
		4	2.5	–	2.5	–	–	2.5	–		–	–	–	–	–	–	3	2	–	9	8	16	-2.0 mA
	V_{OL}	4	–	0.5	–	–	0.5	–	0.5	Vdc	–	–	–	–	2	3	–	–	–	9	8	16	12.0 mA
		4	–	0.5	–	–	0.5	–	0.5		–	–	–	–	–	–	2	3	–	9	8	16	12.0 mA
Switching Times											Pulse In	Pulse Out	C_L (pF)										
Propagation Delay (50% to +1.5 Vdc)	t_{6+5-}	5	–	–	1.0	4.5	6.0	–	–	ns	6	5	25	–	–	–	–	–	3,7,11,15	9	8	16	–
	t_{6-5+}	5	–	–				–	–		6	5		–	–	–	–	–					–
	t_{2+4-}	4	–	–				–	–		2	4		–	–	–	–	–					–
	t_{2-4+}		–	–				–	–					–	–	–	–	–					–
Rise Time (+1.0 Vdc to 2.0 Vdc)	t_{4+}		–	–	–	–	3.3	–	–					–	–	–	–	–					–
Fall Time (+1.0 Vdc to 2.0 Vdc)	t_{4-}		–	–	–	–	3.3	–	–					–	–	–	–	–					–

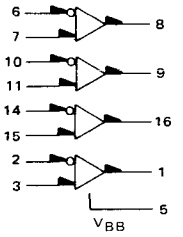
① Individually test each input, apply $V_{IH\ max}$ to pin under test.

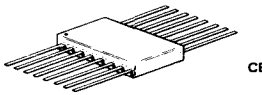
② Individually test each input, apply V_{EE} to pin under test.

③ Individually test each output, following example shown for pin 4.

ELECTRICAL CHARACTERISTICS

Each full temperature range MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Test procedures are shown for only one input, or for one set of input conditions. Other inputs or outputs are tested in the same manner.





F SUFFIX
CERAMIC PACKAGE
CASE 650

@ Test Temperature	TEST VOLTAGE VALUES (Volts)										
	V_{IH} max	V_{IL} min	V_{IHA}min	V_{ILA}max	V_{IHH}	V_{ILH}	V_{IHL}	V_{ILL}	V_{BB}	V_{CC}	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	+0.170	-0.920	-1.830	-2.920	From	+5.0	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	+0.280	-0.850	-1.720	-2.850	Pin	+5.0	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	+0.420	-0.820	-1.580	-2.820	5	+5.0	-5.2

Characteristic	Symbol	Pin Under Test	MC10525F Test Limits -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IH} max	V_{IL} min	V_{IHA}min	V_{ILA}max	V_{IHH}	V_{ILH}	V_{IHL}	V_{ILL}	V_{BB}	V_{CC}	V_{EE}	Gnd	Output Condition
Negative Power Supply Drain Current	I_E	12	—	—	—	—	40	—	—	mAdc	—	—	—	—	—	—	—	—	3,7,11,15	13	12	4	—
Positive Power Supply Drain Current	I_{CCH}	13	—	—	—	—	52	—	—	mAdc	2,6,10,14	—	—	—	—	—	—	—	3,7,11,15	13	12	4	—
	I_{CCL}	13	—	—	—	—	39	—	—	mAdc	—	—	—	—	—	—	—	—	3,7,11,15	13	12	4	—
Input Current	I_{in} H ①	6	—	—	—	—	115	—	—	μAdc	2,6,10,14	—	—	—	—	—	—	—	3,7,11,15	13	12	4	—
		7	—	—	—	—	115	—	—	μAdc	3,7,11,15	—	—	—	—	—	—	—	2,6,10,14	13	12	4	—
Input Leakage Current	I_{CBO} ②	6	—	—	—	—	1.0	—	—	μAdc	—	—	—	—	—	—	—	—	3,7,11,15	13	2,6,10,12,14	4	—
		7	—	—	—	—	1.0	—	—	μAdc	—	—	—	—	—	—	—	—	2,6,10,14	13	3,7,11,12,15	4	—
Short Circuit Current	I_{OS}	8	—	—	40	—	100	—	—	mA	—	2,6,10,14	—	—	—	—	—	—	3,7,11,15	13	12	4,8	—
High Output Voltage	V_{OH} ③	8	2.5		2.5	—	—	2.5	—	Vdc	—	2,6,10,14	—	—	—	—	—	—	3,7,11,15	13	12	4	2.0 mA
Low Output Voltage	V_{OL}	8	—	0.5	—	—	0.5	—	0.5	Vdc	2,6,10,14	—	—	—	—	—	—	—	3,7,11,15	13	12	4	12.0 mA
High Threshold Voltage	V_{OHA}	8	2.5	—	2.5	—	—	2.5	—	Vdc	—	2,10,14	—	6	—	—	—	—	3,7,11,15	13	12	4	-2.0 mA
Low Threshold Voltage	V_{OLA}	8	—	0.5	—	—	0.5	—	0.5	Vdc	2,10,14	—	6	—	—	—	—	—	3,7,11,15	13	12	4	12.0 mA
Indeterminate Input Protection Tests	V_{OLS1}	8	—	0.5	—	—	0.5	—	0.5	Vdc	—	—	—	—	—	—	—	—	—	13	2,3,6,7,10, 11,12,14,15	4	12.0 mA
	V_{OLS2}	8	—	0.5	—	—	0.5	—	0.5	Vdc	—	—	—	—	—	—	—	—	—	13	12	4	12.0 mA
Reference Voltage	V_{BB}	5	-1.440	-1.320	-1.350	—	-1.230	-1.240	1.120	Vdc	—	—	—	—	—	—	—	—	3,7,11,15	—	—	—	—
Common Mode Rejection Tests	V_{OH}	8	2.5		2.5	—	—	2.5	—	Vdc	—	—	—	—	7	6	—	—	—	13	12	4	2.0 mA
		8	2.5		2.5	—	—	2.5	—	—	—	—	—	—	—	—	7	6	—	13	12	4	-2.0 mA
	V_{OL}	8	—	0.5	—	—	0.5	—	0.5	Vdc	—	—	—	—	6	7	—	—	—	13	12	4	12.0 mA
		8	—	0.5	—	—	0.5	—	0.5	—	—	—	—	—	—	—	6	7	—	13	12	4	12.0 mA
Switching Times											Pulse In	Pulse Out	C_L (pF)										
Propagation Delay (50% to +1.5 Vdc)	t_{10+9-}	9	—	—	1.0	4.5	6.0	—	—	ns	10	9	25	—	—	—	—	—	3,7,11,15	13	12	4	—
	t_{10-9+}	9	—	—	↓	↓	↓	—	—		10	9	↓	—	—	—	—	—		↓	↓		—
	t_{8+8-}	8	—	—				—	—		6	8		—	—	—	—	—					—
	t_{8-8+}	↓	—	—				—	—		↓	↓		—	—	—	—	—					—
Rise Time (+1.0 Vdc to 2.0 Vdc)	t_{8+}		—	—	—	—	3.3	—	—					—	—	—	—	—					—
Fall Time (+1.0 Vdc to 2.0 Vdc)	t_{8-}	↓	—	—	—	—	3.3	—	—	↓	↓	↓	↓	—	—	—	—	—	↓	↓	↓	↓	—

① Individually test each input, apply $V_{IH\ max}$ to pin under test.
② Individually test each input, apply V_{EE} to pin under test.
③ Individually test each output, following example shown for pin 8.