MOTOROLA

Military 54LS259

8-Bit Addressable Latch

ELECTRICALLY TESTED PER: MIL-M-35810/31603

The 54LS259 is a high-speed 8-Bit Addressable Latch designed for general purpose storage applications in digital systems. It is a multi-functional device capable of storing single line data in eight addressable latches, and also a 1-of-8 decoder and demultiplexer with active HIGH outputs. The device also incorporates an active LOW common Clear for resetting all latches, as well as, an active LOW Enable.

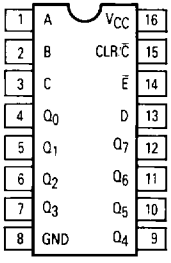
- Serial-to-Parallel Conversion
- Eight Bits of Storage with Output of Each Bit Available
- Random (Addressable) Data Entry
- Easily Expandable
- Common Clear

AVAILABLE AS:

1) JAN: JM35810/31603BXA
2) SMD: *
3) 883C: 54LS259/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CEDIP: E
CERFLAT: F
LCC: 2
***Call Factory for latest update**

CONNECTION DIAGRAM



PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION A)
A	1	1	2	GND
B	2	2	3	GND
C	3	3	4	GND
Q_0	4	4	5	V_{CC}
Q_1	5	5	7	OPEN
Q_2	6	6	8	OPEN
Q_3	7	7	9	OPEN
GND	8	8	10	GND
Q_4	9	9	12	OPEN
Q_5	10	10	13	OPEN
Q_6	11	11	14	OPEN
Q_7	12	12	15	OPEN
DATA (D)	13	13	17	V_{CC}
ENABLE (E)	14	14	18	GND
CLR (C)	15	15	19	GND
V_{CC}	16	16	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

FUNCTIONAL DESCRIPTION

The 54LS259 has four modes of operation as shown in the mode selection table. In the addressable latch mode, data on the Data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the Data or Address inputs.

In the one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other inputs in the LOW state. In the clear mode all outputs are LOW and unaffected by the address and data inputs.

When operating the 54LS259 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

MODE SELECTION

$\overline{E}$	$\overline{C}$	MODE
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH Eight-Channel Demultiplexer
H	L	Clear

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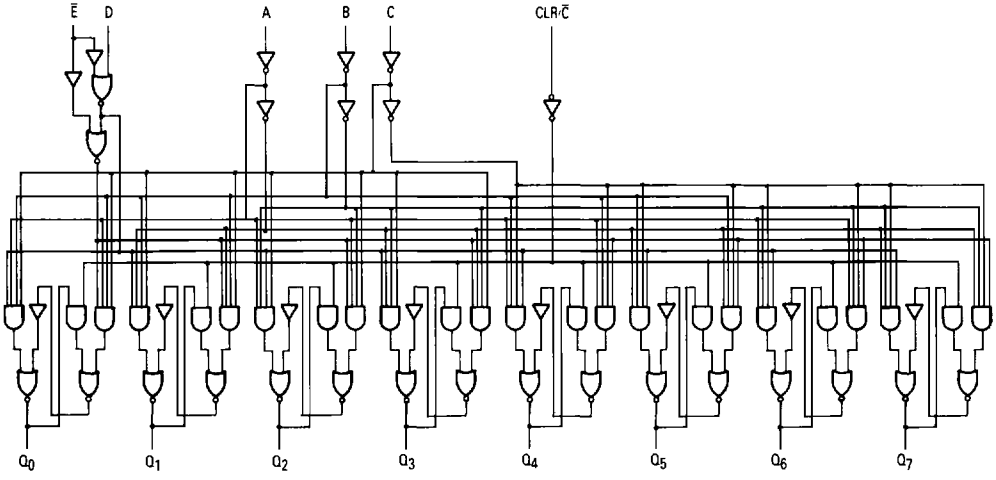
TRUTH TABLE

						Present Output States								
$\overline{C}$	$\overline{E}$	D	A	B	C	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	MODE
L	H	X	X	X	L	L	L	L	L	L	L	L	L	Clear
L	L	L	L	L	L	L	L	L	L	L	L	L	L	Demultiplex
L	L	H	L	L	L	H	L	L	L	L	L	L	L	
L	L	L	H	L	L	L	L	L	L	L	L	L	L	
L	L	H	H	L	L	L	H	L	L	L	L	L	L	
•	•	•		•				•						
•	•	•		•				•						
•	•	•		•				•						
•	•	•		•				•						
•	•	•		•				•						
L	L	H	H	H	H	L	L	L	L	L	L	L	H	
H	H	X	X	X	X	Q_{N-1}								Memory
H	I	I	L	L	L	L	Q_{N-1}	Q_{N-1}	Q_{N-1} →					Addressable
H	L	H	L	L	L	H	Q_{N-1}	Q_{N-1} →						Latch
H	L	L	H	L	L	Q_{N-1}	L	Q_{N-1} →						
H	L	H	H	L	L	Q_{N-1}	H	Q_{N-1} →						
•	•	•						•						
•	•	•						•						
•	•	•						•						
•	•	•						•						
•	•	•						•						
H	L	L	H	H	H	Q_{N-1} →						Q_{N-1}	L	
H	L	H	H	H	H	Q_{N-1} →						Q_{N-1}	H	

X = Don't Care
L = LOW Voltage Level
H = HIGH Voltage Level
Q_{N-1} = Previous Output State

LOGIC DIAGRAM



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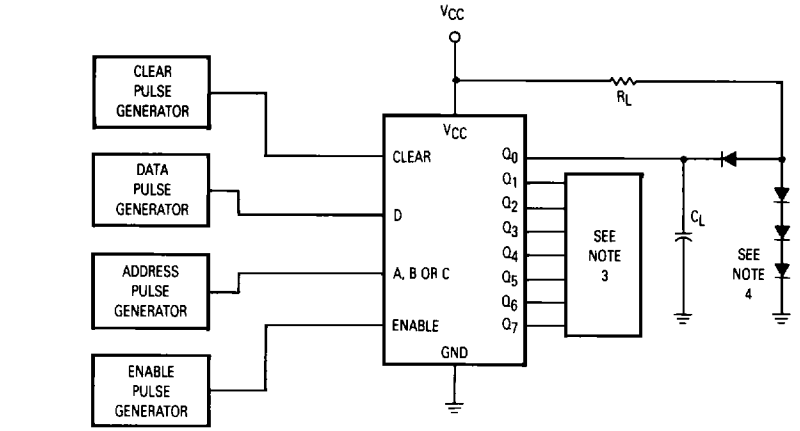
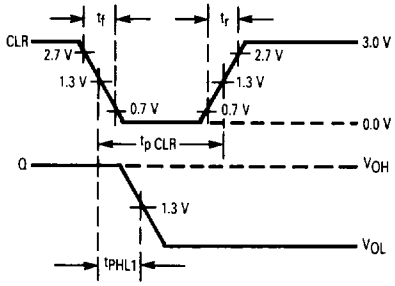
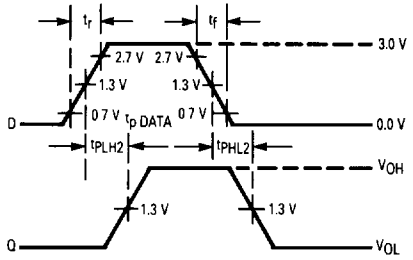
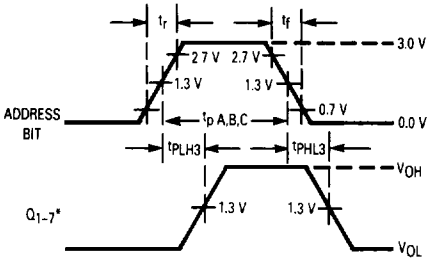
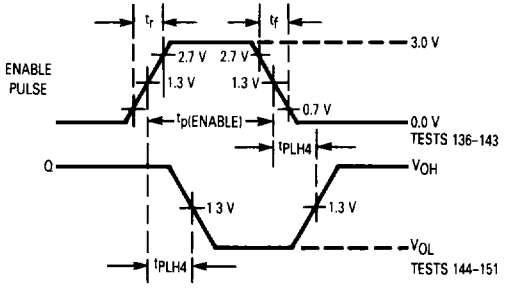
AC TEST CIRCUIT AND WAVEFORMS









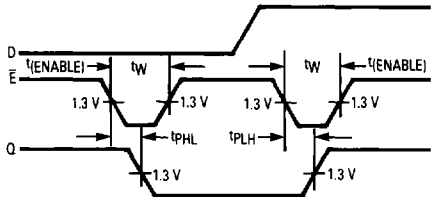


*For Q_0 output, waveform is inverted and t_{PLH3} and t_{PHL3} are interchanged.

NOTES:
1. R_L = 2.0 kΩ ± 5.0%.
2. C_L = 50 pF ± 10% including probe and jig capacitance.
3. All loads are the same as the Q_0 load.
4. All diodes are 1N3064 or equivalent.
5. The clear, enable, data and address pulse generators have the following characteristics: $t_r \leq 15$ ns, $t_f \leq 6.0$ ns, t_p = 30 ns, PRR ≤ 1.0 MHz, $t_{p(ENABLE)}$ = 17 ns, $t_{p(DATA)}$ = 22 ns, $t_{p(ADDRESS)}$ = 47 ns, t_{setup} = 17 ns, t_{HOLD} = 15 ns.
6. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open).

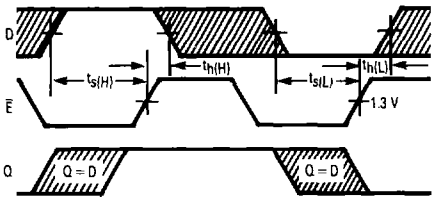
WAVEFORMS

TURN-ON AND TURN-OFF DELAYS, ENABLE TO OUTPUT AND ENABLE PULSE WIDTH



OTHER CONDITIONS: $\overline{CLR}$ = H, A, B, C = STABLE

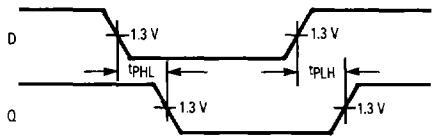
SETUP AND HOLD TIME, DATA TO ENABLE



OTHER CONDITIONS: $\overline{CLR}$ = H, (A, B, C) = STABLE

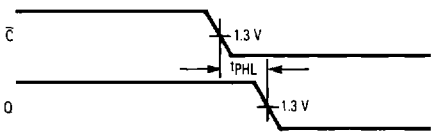
TURN-ON AND TURN-OFF DELAYS, DATA TO OUTPUT

OUTPUT



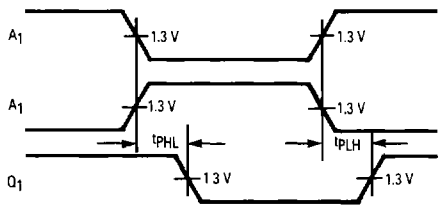
OTHER CONDITIONS: Ē = L, $\overline{CLR}$ = H, (A, B, C) = STABLE

TURN-ON DELAY, CLEAR TO OUTPUT



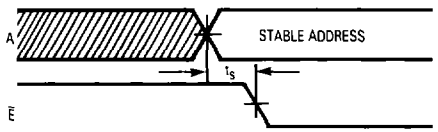
OTHER CONDITIONS: Ē = H

TURN-ON AND TURN-OFF DELAYS, ADDRESS TO OUTPUT



OTHER CONDITIONS: Ē = L, $\overline{CLR}$ = L, D = H

SETUP TIME, ADDRESS TO ENABLE
(SEE NOTES 1 AND 2)



OTHER CONDITIONS: $\overline{CLR}$ = H

NOTES:
1. The Address to Enable Setup Time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.
2. The shaded areas indicate when the inputs are permitted to change for predictable output performance.

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+25°C		+125°C		−55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = −0.4 mA, V_{IH} = 2.0 V, V_{IL} = 0.7 V, D & CLR = 2.0 V, E = (See Note 1).
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OL} = 4.0 mA, V_{IL} = 0.7 V, V_{IH} = 2.0 V, CLR = 2.0 V, D = 0.7 V, E = (See Note 1).
V_{IC}	Input Clamping Voltage		−1.5					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are GND.
I_{IL}	Logical "0" Input Current	−0.12	−0.36	−0.12	−0.36	−0.12	−0.36	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other inputs are open.
I_{IL}	Logical "0" Input Current	−0.005	−0.72	−0.005	−0.72	−0.005	−0.72	mA	V_{CC} = 5.5 V, $V_{IN(E)}$ = 0.4 V, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	μA	V_{CC} = 5.5 V, V_{IH} = 2.7 V.
I_{IHH}	Logical "1" Input Current		100		100		100	μA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V.
I_{OS}	Output Short Circuit Current	−15	−100	−15	−100	−100	−15	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V or GND, D & CLR = 5.0 V, E = GND, V_{OUT} = GND.
I_{CC}	Power Supply Current Off		36		36		36	mA	V_{CC} = 5.5 V, V_{IN} = GND (all inputs).
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.4, V_{INH} = 2.5 V.

NOTE:
1. Apply a 3.0 V, 0 V, 3.0 V momentary pulse 500 ns minimum prior to measurement.

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Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		−55°C			
	Static Parameters:	Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1} t_{PHL1}	Propagation Delay CLR to Q_n	3.0	32 27	3.0	42 37	3.0	42 37	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL2} t_{PHL2}	Propagation Delay D to Q_n	3.0	26 21	3.0	34 29	3.0	34 29	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH2} t_{PLH2}	Propagation Delay D to Q_n	3.0	37 32	3.0	48 43	3.0	48 43	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL3} t_{PHL3}	Propagation Delay A, B, C to Q_n	3.0	34 29	3.0	44 39	3.0	44 39	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH3} t_{PLH3}	Propagation Delay A, B, C to Q_n	3.0	43 38	3.0	56 51	3.0	56 51	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PHL4} t_{PHL4}	Propagation Delay E to Q_n	3.0	29 24	3.0	38 33	3.0	38 33	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.
t_{PLH4} t_{PLH4}	Propagation Delay E to Q_n	3.0	39 35	3.0	52 47	3.0	52 47	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF.