Intel® StrongARM* SA-1110 Microprocessor

Specification Update

April 2001

Notice: The SA-1110 may contain design defects or errors known as errata. Characterized errata that may cause the SA-1110's behavior to deviate from published specifications are documented in this specification update.

Order Number: 278259-022

Contents

Revision History

Date	Version	Description
4/3/01	022	Under Specification Change, modified item 5, “Power Supply Voltages and Currents: Section 12.3” (page 33) to include the B5 stepping. Under Documentation Changes, added item 11, “Memory Map: Section 2.4” (page 38), item 25, “Data Aborts: Section 7.3” (page 41), item 26, “GPIO Pin Output Set Register (GPSR) and Pin Output Clear Register (GPCR): Section 9.1.1.3” (page 41), item 29, “Interrupt Controller Pending Register (ICPR): Section 9.2.1.1” (page 43), item 31, “Interrupt Controller IRQ Pending Register (ICIP) and FIQ Pending Register (ICFP): Section 9.2.1.2” (page 44), item 33, “Real-Time Clock: Section 9.3” (page 45), item 35, “RTC Alarm Register (RTAR): Section 9.3.2” (page 45), item 39, “RTC Status Register (RTSR): Section 9.3.3” (page 46), item 42, “Transaction Summary: Section 10.1.5” (page 47), item 44, “MDCAS Registers with SDRAM and SMROM: Section 10.2.3.2” (page 47), item 45, “Static Memory Control Registers (MSC2 – 0): Section 10.2.4” (page 47), item 51, “DMA Device Address Register (DDARn): Section 11.6.1.1” (page 49), item 54, “DMA Control/ Status Register (DCSRn): Section 11.6.1.2” (page 51), item 56, “DMA Buffer A Transfer Count Register (DBTAn): Section 11.6.1.4” (page 51), item 58, “DMA Buffer B Transfer Count Register (DBTBn): Section 11.6.1.6” (page 52), item 60, “Frame Buffer: Section 11.7.1.2” (page 53), item 61, “LCD Enable (LEN): Section 11.7.3.1” (page 54), item 72, “LCD Disable Done Flag: Section 11.7.11.1” (page 56), item 73, “Base Address Update Flag: Section 11.7.11.2” (page 56), item 75, “Output FIFO Underrun Upper Panel Status (OUU) (read/write, maskable interrupt): Section 11.7.11.12” (page 57), item 80, “Serial Port 0 – USB Device Controller: Section 11.8” (page 60), item 81, “USB Operation: Section 11.8.1” (page 61), item 82, “UDC Endpoint 2 Control/Status Register: Section 11.8.9” (page 61), item 87, “4PPM Modulation: Section 11.10.2.1” (page 62), item 88, “CPU and DMA Register Access Sizes: Secti9on 11.10.2.11” (page 62), item 90, “Low-Power Mode (LPM): Section 11.10.4.2” (page 62), item 91, “IrDA Transmission Rate (ITR): Section 11.10.6.1” (page 63), item 92, “Loopback Mode (LBM): Section 11.10.6.2” (page 63), item 93, “Transmit Enable (TXE): Section 11.10.6.4” (page 63), item 94, “Receive Pin Polarity Select (RXP): Section 11.10.8.2” (page 63), item 95, “End/Error in FIFO Status (EIF) (read-only, nonmaskable interrupt): Section 11.10.10.1” (page 64), 96, “Framing Error Status (FRE) (read/write, nonmaskable interrupt): Section 11.10.10.6” (page 64), item 97, “CRC Error Status (CRE) (read-only, noninterruptible): Section 11.10.11.6” (page 64), 98, “Receiver Overrun Status (ROR) (read-only, noninterruptible): Section 11.10.11.7” (page 64), item 101, “UART Data Register: Section 11.11.6” (page 65), item 112, “Power Supply Voltages and Currents: Section 12.3” (page 68), item 113, “Timing Parameters: Section 13.6” (page 69), item 115, “Package and Pinout: Section 14” (page 70), and item 116, “Intel® StrongARM SA-1110 Device Identification (ID) Code Register: Section 16.6.2” (page 71).

Date	Version	Description
2/26/01	021	New Errata item 29, “USB Controller Endpoint 2 (IN) Transmits Incorrect Data” (page 32) has been added. Modified the workaround for 27, “Incorrect Values Are Read from RTTR and RCNR Registers Immediately After They Are Written” (page 28). Under Specification Change, added item 4, “DC Operating Conditions: Section 12.2” (page 33), and item 5, “Power Supply Voltages and Currents: Section 12.3” (page 33). Under Documentation Changes, added item 10, “Data Cache: Section 1.4.5” (page 38), item 12, “Coprocessors: Section 3.3” (page 39), item 13, “Internal Coprocessor Instructions: Section 5.1” (page 39), item 14, “Register 7 – Cache Control Operations: Section 5.2.8” (page 39), item 15, “Register 9 – Read-Buffer Operations: Section 5.2.10” (page 39), item 24, “Read Buffer: Section 6.4” (page 41), item 28, “Interrupt Controller: Section 9.2” (page 42), item 30, “Interrupt Controller FIQ Pending Register (ICFP): Section 9.2.1.2” (page 43), item 32, “Interrupt Controller Control Register (ICCR): Section 9.2.1.5” (page 44), item 34, “RTC Counter Register (RCNR): Section 9.3.1” (page 45), item 36, “RTC Status Register (RTSR): Section 9.3.3” (page 46), item 37, “RTC Status Register (RTSR): Section 9.3.3” (page 46), item 40, “RTC Trim Register (RTTR): Section 9.3.4” (page 46), item 47, “SDRAM Commands: Section 10.4.4” (page 48), item 59, “Frame Buffer: Section 11.7.1.2” (page 52), item 64, “Double-Pixel Data (DPD) Pin Mode: Section 11.7.3.9” (page 55), item 77, “LCD Controller Pin Timing Diagrams: Section 11.7.13” (page 57), item 78, “LCD Controller Pin Timing Diagrams: Section 11.7.13” (page 58), item 79, “LCD Controller Pin Timing Diagrams: Section 11.7.13” (page 59), item 85, “Sample Clock Direction (SCD): Section 11.9.2.3” (page 62), item 86, “Transmit Enable (TXE): Section 11.9.3.1” (page 62), item 103, “SSP Transmit and Receive FIFOs: Section 11.12.7.3” (page 65), item 107, “PPC Pin State Register: Section 11.13.4” (page 67), item 109, “PPC Sleep Mode Pin Direction Register: Section 11.13.6” (page 67), item 110, “PPC Pin Flag Register: Section 11.13.7” (page 67), item 111, “DC Operating Conditions: Section 12.2” (page 67), item 112, “Power Supply Voltages and Currents: Section 12.3” (page 68), and item 115, “Package and Pinout: Section 14” (page 70)
12/08/00	020	New Errata item 28, “Incorrect Address Decode in USB Controller” (page 29) has been added. Under Documentation Changes, added item 33, “Real-Time Clock: Section 9.3” (page 45), item 38, “RTC Status Register (RTSR): Section 9.3.3” (page 46), item 43, “DRAM Refresh Control Register (MDREFR): Section 10.2.2” (page 47), item 46, “SMROM Configuration Register (SMCNFG): Section 10.3” (page 48), item 49, “DMA Device Address Register (DDARn): Section 11.6.1.1” (page 48), item 50, “DMA Device Address Register (DDARn): Section 11.6.1.1” (page 49), item 52, “DMA Control/Status Register (DCSRn): Section 11.6.1.2” (page 50), item 53, “DMA Control/Status Register (DCSRn): Section 11.6.1.2” (page 50), item 55, “DMA Buffer A Transfer Count Register (DBTAn): Section 11.6.1.4” (page 51), item 57, “DMA Buffer B Transfer Count Register (DBTBn): Section 11.6.1.6” (page 52), item 66, “Palette DMA Request Delay (PDD): Section 11.7.3.10” (page 55), item 76, “LCD Controller Register Locations: Section 11.7.12” (page 57), item 83, “UDC Endpoint Data Register: Section 11.8.10” (page 61), item 84, “UDC Data Register: Section 11.8.12” (page 61), item 100, “UART Data Register: Section 11.11.6” (page 65), item 102, “SSP Transmit and Receive FIFOs: Section 11.12.7.3” (page 65), item 104, “SSP Data Register: Section 11.12.11” (page 66), item 105, “PPC Pin Direction Register: Section 11.13.3” (page 66), item 106, “PPC Pin State Register: Section 11.13.4” (page 66), and item 108, “PPC Pin Assignment Register: Section 11.13.5.2” (page 67).
10/20/00	019	New Errata item 27, “Incorrect Values Are Read from RTTR and RCNR Registers Immediately After They Are Written” (page 28) has been added. New Specification Change item 3, “Modifications in SDRAM/SMROM Data Input Hold Time” (page 33) has been added. Under Documentation Changes, added item 23, “Read Buffer: Section 6.4” (page 40), item 43, “DRAM Refresh Control Register (MDREFR): Section 10.2.2” (page 47), item 46, “SMROM Configuration Register (SMCNFG): Section 10.3” (page 48), item 59, “Frame Buffer: Section 11.7.1.2” (page 52), item 69, “Output Enable Polarity (OEP): Section 11.7.6.7” (page 56), item 74, “Output FIFO Underrun Upper Panel Status (OUU) (read/write, maskable interrupt): Section 11.7.11.12” (page 57), item 76, “LCD Controller Register Locations: Section 11.7.12” (page 57), item 99, “Sample Clock GPIO: Section 11.11.3.5” (page 64), item 111, “DC Operating Conditions: Section 12.2” (page 67), item 113, “Timing Parameters: Section 13.6” (page 69), and item 118, “Boundary Scan Interface Signals: Section 16.7” (page 71).

Date	Version	Description
9/12/00	018	Under Errata item 21, “Failure of Synchronous Serial Port (SSP) Receiver Overrun Status Bit to Generate Interrupt Request” (page 27) -- the workaround instructions have been modified. In Item 24, “Software Sleep Status Bit (PSSR:SSS) May Be Improperly Set After Sleep Wakeup” (page 28) the “affected steppings” have been modified (affects all steppings). New items 25, “Improper Operation of LCD Controller LCCR2 Register EFW (End of Frame Line Clock Wait Count)” (page 28) and 26, “Between Two Successive PCMCIA Accesses, Bus Arbiter Might Not Recognize Pending, Highest-Priority, Bus Access Request From LCD Controller” (page 28) have been added. Under Documentation Changes, removed documentation changes 1-6, 8-11, 13-20, 23-28, 30, 32, 34-36, 39-97 (having been incorporated into revision -003 of the developer’s manual) respective to Specification Update Revision 017. Under Documentation Changes, modified documentation change 21 (respective to revision 017) by removing the description for changing ‘9 bits’ to ‘9 bytes’ as this part of the modification was already implemented in revision -003 of the developer’s manual. Modified documentation change 22 (respective to revision 017) by removing the description for changing bits 24 and 25 as this part of the modification is no longer required. The new descriptions of these changes are now documentation changes 3 and 4. Under Documentation Changes, added item 16, “Register 14 – Debug Support (Breakpoints): Section 5.2.13” (page 39) item 17, “Data Caches (Dcaches): Section 6.2” (page 39), item 18, “Writes to a Bufferable and Noncacheable Location (B=1,C=0): Section 6.3.2.2” (page 40), item 19, “Unbufferable and Noncacheable Writes (B=0, C=0): Section 6.3.2.3” (page 40), item 20, “Writes to a Non-Bufferable and Cacheable Location (B=0, C=1): Section 6.3.2.4” (page 40), item 21, “Read Buffer (RB): Section 6.4” (page 40), item 22, “Read Buffer: Section 6.4” (page 40), item 41, “Sleep Mode: Section 9.5.3” (page 46), item 48, “8-, 16-, and 32-Bit Data Bus Operation: Section 10.6.1” (page 48), item 50, “DMA Device Address Register (DDARn): Section 11.6.1.1” (page 49), item 59, “Frame Buffer: Section 11.7.1.2” (page 52), item 62, “Passive/Active Display Select (PAS): Section 11.7.3.7” (page 54), item 63, “Passive/Active Display Select (PAS): Section 11.7.3.7” (page 54), item 65, “Palette DMA Request Delay (PDD): Section 11.7.3.10” (page 55)item 67, “Beginning-of-Frame Line Clock Wait Count (BFW): Section 11.7.5.4” (page 55), item 70, “DMA Channel 1 Current Address Register: Section 11.7.9” (page 56), item 71, “Output FIFO Underrun Lower Panel Status (OUL) (read only, maskable interrupt): Section 11.7.10” (page 56), item 74, “Output FIFO Underrun Upper Panel Status (OUU) (read/write, maskable interrupt): Section 11.7.11.12” (page 57), item 74, “Output FIFO Underrun Upper Panel Status (OUU) (read/write, maskable interrupt): Section 11.7.11.12” (page 57), item 76, “LCD Controller Register Locations: Section 11.7.12” (page 57), item 111, “DC Operating Conditions: Section 12.2” (page 67), item 112, “Power Supply Voltages and Currents: Section 12.3” (page 68), item 113, “Timing Parameters: Section 13.6” (page 69), item 114, “Timing Parameters: Section 13.6” (page 70), item 116, “Intel® StrongARM SA-1110 Device Identification (ID) Code Register: Section 16.6.2” (page 71), and item 117, “Boundary-Scan Interface Signals: Section 16.7” (page 71).

Date	Version	Description
6/22/00	017	Under Errata, changed the No Fix setting to Fix in the Status fields of Errata 13 — 16 and 18, established errata 17 as a No Fix, as well as adding the B4 step designator to the Affected Steppings fields for all forementioned. Also added two new errata (19 and 20) describing a failure to Reset UDC IN/OUT Data Packet Toggle Generation to DATA0/1 on Endpoints 1/2. And added errata describing the failure of the SSP bit to generate an interrupt request (21), describing the failure of the LCD Controller to operate correctly following reconfiguration events (22), and describing how a misaligned word access with a 16-bit data bus can generate incorrect data (23). Under Documentation Changes, added to documentation change 2 two tables to Section 13.1 describing output derating parameters for slow and fast output buffers, removed documentation changes 3—63 (having been incorporated into the revision 003 developer's manual) respective to Specification Update Revision 016. Also added updated information for the Reset Interrupt Mask, Receive Packet Error bit, Force Stall bit, and the UDC Control Register. Added information describing: Software Control of the UDC; a new section entitled "GPCLK Control Register 1"; changed section formally named "GPCLK Control Registers 1 and 2"; updated the table in the "GPCLK Register Locations" section. Made sentence corrections to the following sections: Serial Port 3 – UART; Baud Rate Divisor (BRD); Baud Rate Generation. Made general format corrections. Corrected bit assignment values to registers in Chapter 11. Rewrote sections 11.8.3, 11.8.3.4, 11.8.3.5, 11.8.3.6, 11.8.3.7, 11.8.3.3, 11.8.13.2, 11.8.13.13, 11.8.13.4, 11.8.13.5, 11.9, 9.3.4. Restructured Section 10.4.1. Added a note as appropriate in Chapters 9 and 11 to identify the use of a question mark as a value designator in register Reset fields. Added new section for GPCLK Register 1. Added new section describing software control of the UDC register. Rewrote Section 9.5.2.2, "exit Idle Mode." Added new data for the Force Stall bit.Added new output derating tables to Chapter 13. Updated GPCLK register locations table. Changed "899.78 MHz" to "900 Hz" as needed in Section 11.9. Updated section for GPCLK registers 1 and 2. Corrected baud rate divisor descriptions. Restructured Section 13.6. Corrected Figure 10-1. See Documentation Changes 41 through 97 for details.
4/6/00	016	Under Documentation Changes, added notes describing use definition of register reset value, listed in documentation changes 66–95. Corrected Transaction Formats figure (30) and corrected text and figure for Packet Formats (31). Added table footnote for GPIO functions and corrected USB web site listing. Corrected Figure 11-17 figure title and text located in paragraph above Figure 11-17. Corrected bit definitions for the MCCR0 register table. Corrected text in sections 11.8.3.8 and 11.8.12. Updated Table 12-3. Under Errata, added 5 errata documenting register reads/writes following SDRAM/SDROM reads and sleep requests and SDRAM refresh issues.
1/25/00	015	Under Documentation Changes, removed documentation changes #63 — #99 (referencing the 014 specification update) from the specification update and applied them to the developer's manual; added two changes documenting a change in the exit idle mode process (Chapter 9) and a change in the register summary table (Appendix A). Under Specification Changes, added one line to Specification Changes table.
1/11/00	014	Under Documentation Changes, added 38 documentation changes removing all references to SDLC, substituting SDLC information with GPCLK information. Made four changes substituting RDN+1 with RDF+1. Changed one line in the parameters definition list in section 10.5.8 and added one footnote for Figure 10-18. Also added GPCLKR0 register to Section 11.9.3.6. Under Errata, added one errata documenting UDC work-around procedure.
12/07/99	013	Under Errata, added nine errata; under Documentation Changes, changed output signals listed in Table 13-2; changes made to Section 10.1.7, Section 10.2.1, Section 10.2.2, Section 10.2.3, Section 10.2.4, Section 10.2.5, Section 10.3, Section 10.4.6, Section 10.5.1, Section 10.5.11, Section 10.7, Section 10.7.1, and Section 10.7.2; changed Section 13.6.SDLC feature changed from an errata to a specification change.
11/18/99	012	Under Documentation Changes, changed ID code and added stepping information in section 5.2.1.
11/15/99	011	Under Errata, added two errata; under Documentation Changes, changed title of section 13.2.
11/05/99	010	Under Documentation Changes, added sentence to end of first paragraph in section 9.5.2.2.
11/03/99	009	Under Documentation Changes, changed signal description of GPIO pin 25 in table in section 9.1.2; added note to end of section 11.11.6; deleted note to bit 3 of the RCSR register in section 9.6.1.2; revised bit 0 description of USB Device Controller (UDC) CR register in section 11.8.3.8; replaced section 11.10.2.3; corrected typo in table 9-3 title; changed sentence in section 10.8.

Date	Version	Description
10/08/99	008	Under Errata, added one errata; under Documentation Changes, added paragraph to section 16.6.3; added boundary-scan signals and pins table 16-2.
09/15/99	007	Under Documentation Changes, added footnote to GPIO Alternate Functions Table in Section 9.1.2.
08/19/99	006	Under Documentation Changes, changed settings for serial port 2 and serial port 4 in Table 11-6.
07/22/99	005	Under Documentation Changes, changed code example for section 6.2.3; changed last sentence of section 9.5.3; added output signals to table 13-2.
06/28/99	004	Under Documentation Changes, removed section 16.8; changed Test Unit Control Register's description of bit 10; added change to Section 9.5.7.7; changed Figure 10-6; added change to section 10.5.1; added change to section 10.1; added change to section 10.2.2.and description of MDREFR:EAPD and MDREFR:KAPD bits; added step #8 to section 10.7.1; removed the SA-1110 Tool Chains and Operating Systems Table from the brief datasheet and the developer's manual; added change to section 9.5.6; added change to section 11.13.1; added change to section 11.13.6; added change to section 10.5.5.
05/18/99	003	Under Documentation Changes, added changes to the PPSR and PSDR register drawing graphics; added changes to the OS Timer Interrupt Enable register; added change to the Big and Little Endian DMA Transfers graphic; corrected peripheral pin assignments; changed 15 timing diagrams; changed bit 31 description in the DRAM Refresh Control Register; added changes to section 10.4.7; added changes to section 10.7.1; added changes to section 10.8.
04/19/99	002	Under Document Changes, added changes to section 1.1; section 9.1.2.1; section 3.1; section 10.2.4; and section 10.6.
03/26/99	001	This is the new specification update document. It contains all identified errata published prior to this date.

Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
Intel® StrongARM* SA-1110 Microprocessor Developer's Manual	278240-003

Nomenclature

Errata are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the SA-1110 microprocessor. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum s intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

|	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata (Sheet 1 of 2)

No.	Steppings						Page	Status	ERRATA
	A0	B0	B1	B2	B4	B5			
1	X	X	X	X	X	X	20	No Fix	Incorrect Sign-Extended Value in Register After a Read Buffer Allocate
2	X	X	X	X	X	X	20	No Fix	LCD Ghost Lines
3	X						20	Fixed	High Current on VDDX During Reset
4	X						20	Fixed	High Current on VDDX During Sleep
5	X						20	Fixed	LCD State Machine Throughput Fails Using SDRAM at Full-Memory Clock Frequency
6	X						21	Fixed	USB Stalls When More Than One USB Client Is Present
7	X						21	Fixed	SDRAM Auto-Power-Up Failure
8	X						21	Fixed	SDRAM RAS Precharge Counter May Not Work in the Presence of SMROM
9	X	X					21	Fixed	DRAM Refresh Corrupting ROM/Flash Burst of 4/8 Timing
10	X	X	X				22	Fixed	Data Contention Caused by Hardware, Software, or Watchdog Reset During SDRAM/SMROM Reads
11	X	X	X				23	Fixed	Erroneous SMROM Precharge All (PALL) Command with Mode Register Set (MRS) Command After Hardware, Software, Watchdog, or Sleep Reset
12	X	X	X				23	Fixed	UDC Not Responding to IN Packet After Receiving an SOF Packet
13	X	X	X				23	Fixed	Corruption of Internal Register Reads/Writes Following SDRAM/SDROM Reads
14	X	X	X	X			24	Fixed	Failure on Sleep Request During Variable Latency I/O to Perform SDRAM Self-Refresh and Enter Sleep
15	X	X	X	X			24	Fixed	Failure on Sleep Request During CBR Refreshes to Perform SDRAM Self-Refresh Prior to Entering Sleep
16				X			25	Fixed	Erroneous SDRAM Power-Down-Exit and Power-Down Following Self-Refresh and Sleep Entry
17	X	X	X	X	X	X	26	No Fix	Corruption of Internal Register Reads/Writes Following Reads from SDRAM on 16-bit Data Busses at Full Memory Clock Frequency
18	X	X	X	X			26	Fixed	Failure on Sleep Request During SDRAM Read/Write Bursts to Precharge SDRAM Row Prior to Performing SDRAM Self-Refresh and Entering Sleep
19	X	X	X	X			26	Fixed	Failure to Reset UDC OUT Data Packet Toggle Checking to DATA0 on Endpoint 1 After a Sequence of Setting/Clearing Force Stall Bit (UDCCS1:FST) and Clearing Sent Stall Bit (UDCCS1:SST)

Errata (Sheet 2 of 2)

No.	Steppings						Page	Status	ERRATA
	A0	B0	B1	B2	B4	B5			
20	X	X	X	X			27	Fixed	Failure to Reset UDC IN Data Packet Toggle Generation to DATA0 on Endpoint 2 After a Sequence of Setting/Clearing Force Stall Bit (UDCCS2:FST) and Clearing Sent Stall Bit (UDCCS2:SST)
21	X	X	X	X	X	X	27	Eval	Failure of Synchronous Serial Port (SSP) Receiver Overrun Status Bit to Generate Interrupt Request
22	X	X	X	X	X	X	27	No Fix	LCD Controller Fails to Operate Correctly Following Reconfiguration
23	X	X	X	X	X	X	27	No Fix	Misaligned Word Accesses with 16-Bit Data Bus May Produce Incorrect Data
24	X	X	X	X	X	X	28	No Fix	Software Sleep Status Bit (PSSR:SSS) May Be Improperly Set After Sleep Wakeup
25	X	X	X	X	X	X	28	No Fix	Improper Operation of LCD Controller LCCR2 Register EFW (End of Frame Line Clock Wait Count)
26	X	X	X	X	X	X	28	No Fix	Between Two Successive PCMCIA Accesses, Bus Arbiter Might Not Recognize Pending, Highest-Priority, Bus Access Request From LCD Controller
27	X	X	X	X	X	X	28	No Fix	Incorrect Values Are Read from RTTR and RCNR Registers Immediately After They Are Written
28	X	X	X	X	X		29	Fixed	Incorrect Address Decode in USB Controller
29	X	X	X	X	X		32	Fixed	USB Controller Endpoint 2 (IN) Transmits Incorrect Data

Specification Changes

No.	Steppings						Page	Status	Specification Changes
	A0	B0	B1	B2	B4	B5			
1	X	X	X	X	X	X	33	Eval	SDLC Feature
2	X	X	X	X	X	X	33	No Fix	SDLC Feature Not Supported
3	X	X	X	X	X	X	33	No Fix	Modifications in SDRAM/SMROM Data Input Hold Time
4	X	X	X	X	X	X	33	No Fix	DC Operating Conditions: Section 12.2
5	X	X	X	X	X	X	33	No Fix	Power Supply Voltages and Currents: Section 12.3

Specification Clarifications

No.	Steppings						Page	Status	Specification Clarifications
	A0	B0	B1	B2	B4	B5			
									None for this revision of this specification update.

Documentation Changes (Sheet 1 of 4)

No.	Document Revision	Page	Status	Documentation Changes
1	278240-002	36	Doc	GPCLK Control Register 1: Section 11.9.3
2	278240-002	36	Doc	HSSP Data Register: Section 11.10.9
3	278240-002	36	Doc	Receiver Overrun Flag (ROR) (read-only, noninterruptible): Section 11.11.8.6
4	278240-002	36	Doc	External Clock Prescaler (ECP): Section 11.12.3.11
5	278240-002	36	Doc	USB Operation: Section 11.8
6	278240-002	36	Doc	Packet Formats: Section 11.8.1.5
7	278240-002	37	Doc	UDC Data Register: Section 11.8.12
8	278240-002	38	Doc	Bit 2 Reserved: Section 11.8.3.3
9	278240-002	38	Doc	Suspend/Resume Interrupt Mask (SRM): Section 11.8.3.7
10	278240-003	38	Doc	Data Cache: Section 1.4.5
11	278240-003	38	Doc	Memory Map: Section 2.4
12	278240-003	39	Doc	Coprocessors: Section 3.3
13	278240-003	39	Doc	Internal Coprocessor Instructions: Section 5.1
14	278240-003	39	Doc	Register 7 – Cache Control Operations: Section 5.2.8
15	278240-003	39	Doc	Register 9 – Read-Buffer Operations: Section 5.2.10
16	278240-003	39	Doc	Register 14 – Debug Support (Breakpoints): Section 5.2.13
17	278240-003	39	Doc	Data Caches (Dcaches): Section 6.2
18	278240-003	40	Doc	Writes to a Bufferable and Noncacheable Location (B=1,C=0): Section 6.3.2.2
19	278240-003	40	Doc	Unbufferable and Noncacheable Writes (B=0, C=0): Section 6.3.2.3
20	278240-003	40	Doc	Writes to a Non-Bufferable and Cacheable Location (B=0, C=1): Section 6.3.2.4
21	278240-003	40	Doc	Read Buffer (RB): Section 6.4
22	278240-003	40	Doc	Read Buffer: Section 6.4
23	278240-003	40	Doc	Read Buffer: Section 6.4
24	278240-003	41	Doc	Read Buffer: Section 6.4
25	278240-003	41	Doc	Data Aborts: Section 7.3
26	278240-003	41	Doc	GPIO Pin Output Set Register (GPSR) and Pin Output Clear Register (GPCR): Section 9.1.1.3

Documentation Changes (Sheet 2 of 4)

No.	Document Revision	Page	Status	Documentation Changes
27	278240-003	42	Doc	GPIO Alternate Functions: Section 9.1.2
28	278240-003	42	Doc	Interrupt Controller: Section 9.2
29	278240-003	43	Doc	Interrupt Controller Pending Register (ICPR): Section 9.2.1.1
30	278240-003	43	Doc	Interrupt Controller FIQ Pending Register (ICFP): Section 9.2.1.2
31	278240-003	44	Doc	Interrupt Controller IRQ Pending Register (ICIP) and FIQ Pending Register (ICFP): Section 9.2.1.2
32	278240-003	44	Doc	Interrupt Controller Control Register (ICCR): Section 9.2.1.5
33	278240-003	45	Doc	Real-Time Clock: Section 9.3
34	278240-003	45	Doc	RTC Counter Register (RCNR): Section 9.3.1
35	278240-003	45	Doc	RTC Alarm Register (RTAR): Section 9.3.2
36	278240-003	46	Doc	RTC Status Register (RTSR): Section 9.3.3
37	278240-003	46	Doc	RTC Status Register (RTSR): Section 9.3.3
38	278240-003	46	Doc	RTC Status Register (RTSR): Section 9.3.3
39	278240-003	46	Doc	RTC Status Register (RTSR): Section 9.3.3
40	278240-003	46	Doc	RTC Trim Register (RTTR): Section 9.3.4
41	278240-003	46	Doc	Sleep Mode: Section 9.5.3
42	278240-003	47	Doc	Transaction Summary: Section 10.1.5
43	278240-003	47	Doc	DRAM Refresh Control Register (MDREFR): Section 10.2.2
44	278240-003	47	Doc	MDCAS Registers with SDRAM and SMROM: Section 10.2.3.2
45	278240-003	47	Doc	Static Memory Control Registers (MSC2 – 0): Section 10.2.4
46	278240-003	48	Doc	SMROM Configuration Register (SMCNFG): Section 10.3
47	278240-003	48	Doc	SDRAM Commands: Section 10.4.4
48	278240-003	48	Doc	8-, 16-, and 32-Bit Data Bus Operation: Section 10.6.1
49	278240-003	48	Doc	DMA Device Address Register (DDARn): Section 11.6.1.1
50	278240-003	49	Doc	DMA Device Address Register (DDARn): Section 11.6.1.1
51	278240-003	49	Doc	DMA Device Address Register (DDARn): Section 11.6.1.1
52	278240-003	50	Doc	DMA Control/Status Register (DCSRn): Section 11.6.1.2
53	278240-003	50	Doc	DMA Control/Status Register (DCSRn): Section 11.6.1.2
54	278240-003	51	Doc	DMA Control/Status Register (DCSRn): Section 11.6.1.2

Documentation Changes (Sheet 3 of 4)

No.	Document Revision	Page	Status	Documentation Changes
55	278240-003	51	Doc	DMA Buffer A Transfer Count Register (DBTAn): Section 11.6.1.4
56	278240-003	51	Doc	DMA Buffer A Transfer Count Register (DBTAn): Section 11.6.1.4
57	278240-003	52	Doc	DMA Buffer B Transfer Count Register (DBTBn): Section 11.6.1.6
58	278240-003	52	Doc	DMA Buffer B Transfer Count Register (DBTBn): Section 11.6.1.6
59	278240-003	52	Doc	Frame Buffer: Section 11.7.1.2
60	278240-003	53	Doc	Frame Buffer: Section 11.7.1.2
61	278240-003	54	Doc	LCD Enable (LEN): Section 11.7.3.1
62	278240-003	54	Doc	Passive/Active Display Select (PAS): Section 11.7.3.7
63	278240-003	54	Doc	Passive/Active Display Select (PAS): Section 11.7.3.7
64	278240-003	55	Doc	Double-Pixel Data (DPD) Pin Mode: Section 11.7.3.9
65	278240-003	55	Doc	Palette DMA Request Delay (PDD): Section 11.7.3.10
66	278240-003	55	Doc	Palette DMA Request Delay (PDD): Section 11.7.3.10
67	278240-003	55	Doc	Beginning-of-Frame Line Clock Wait Count (BFW): Section 11.7.5.4
68	278240-003	56	Doc	Pixel Clock Divider: Section 11.7.6.1
69	278240-003	56	Doc	Output Enable Polarity (OEP): Section 11.7.6.7
70	278240-003	56	Doc	DMA Channel 1 Current Address Register: Section 11.7.9
71	278240-003	56	Doc	Output FIFO Underrun Lower Panel Status (OUL) (read only, maskable interrupt): Section 11.7.10
72	278240-003	56	Doc	LCD Disable Done Flag: Section 11.7.11.1
73	278240-003	56	Doc	Base Address Update Flag: Section 11.7.11.2
74	278240-003	57	Doc	Output FIFO Underrun Upper Panel Status (OUU) (read/write, maskable interrupt): Section 11.7.11.12
75	278240-003	57	Doc	Output FIFO Underrun Upper Panel Status (OUU) (read/write, maskable interrupt): Section 11.7.11.12
76	278240-003	57	Doc	LCD Controller Register Locations: Section 11.7.12
77	278240-003	57	Doc	LCD Controller Pin Timing Diagrams: Section 11.7.13
78	278240-003	58	Doc	LCD Controller Pin Timing Diagrams: Section 11.7.13
79	278240-003	59	Doc	LCD Controller Pin Timing Diagrams: Section 11.7.13
80	278240-003	60	Doc	Serial Port 0 – USB Device Controller: Section 11.8
81	278240-003	61	Doc	USB Operation: Section 11.8.1
82	278240-003	61	Doc	UDC Endpoint 2 Control/Status Register: Section 11.8.9
83	278240-003	61	Doc	UDC Endpoint Data Register: Section 11.8.10
84	278240-003	61	Doc	UDC Data Register: Section 11.8.12
85	278240-003	62	Doc	Sample Clock Direction (SCD): Section 11.9.2.3

Documentation Changes (Sheet 4 of 4)

No.	Document Revision	Page	Status	Documentation Changes
86	278240-003	62	Doc	Transmit Enable (TXE): Section 11.9.3.1
87	278240-003	62	Doc	4PPM Modulation: Section 11.10.2.1
88	278240-003	62	Doc	CPU and DMA Register Access Sizes: Secti9on 11.10.2.11
89	278240-003	62	Doc	HP-SIR * Enable (HSE): Section 11.10.4.1
90	278240-003	62	Doc	Low-Power Mode (LPM): Section 11.10.4.2
91	278240-003	63	Doc	IrDA Transmission Rate (ITR): Section 11.10.6.1
92	278240-003	63	Doc	Loopback Mode (LBM): Section 11.10.6.2
93	278240-003	63	Doc	Transmit Enable (TXE): Section 11.10.6.4
94	278240-003	63	Doc	Receive Pin Polarity Select (RXP): Section 11.10.8.2
95	278240-003	64	Doc	End/Error in FIFO Status (EIF) (read-only, nonmaskable interrupt): Section 11.10.10.1
96	278240-003	64	Doc	Framing Error Status (FRE) (read/write, nonmaskable interrupt): Section 11.10.10.6
97	278240-003	64	Doc	CRC Error Status (CRE) (read-only, noninterruptible): Section 11.10.11.6
98	278240-003	64	Doc	Receiver Overrun Status (ROR) (read-only, noninterruptible): Section 11.10.11.7
99	278240-003	64	Doc	Sample Clock GPIO: Section 11.11.3.5
100	278240-003	65	Doc	UART Data Register: Section 11.11.6
101	278240-003	65	Doc	UART Data Register: Section 11.11.6
102	278240-003	65	Doc	SSP Transmit and Receive FIFOs: Section 11.12.7.3
103	278240-003	65	Doc	SSP Transmit and Receive FIFOs: Section 11.12.7.3
104	278240-003	66	Doc	SSP Data Register: Section 11.12.11
105	278240-003	66	Doc	PPC Pin Direction Register: Section 11.13.3
106	278240-003	66	Doc	PPC Pin State Register: Section 11.13.4
107	278240-003	67	Doc	PPC Pin State Register: Section 11.13.4
108	278240-003	67	Doc	PPC Pin Assignment Register: Section 11.13.5.2
109	278240-003	67	Doc	PPC Sleep Mode Pin Direction Register: Section 11.13.6
110	278240-003	67	Doc	PPC Pin Flag Register: Section 11.13.7
111	278240-003	67	Doc	DC Operating Conditions: Section 12.2
112	278240-003	68	Doc	Power Supply Voltages and Currents: Section 12.3
113	278240-003	69	Doc	Timing Parameters: Section 13.6
114	278240-003	70	Doc	Timing Parameters: Section 13.6
115	278240-003	70	Doc	Package and Pinout: Section 14
116	278240-003	71	Doc	Intel® StrongARM SA-1110 Device Identification (ID) Code Register: Section 16.6.2
117	278240-003	71	Doc	Boundary-Scan Interface Signals: Section 16.7
118	278240-003	71	Doc	Boundary Scan Interface Signals: Section 16.7

Identification Information

Markings

Package Markings	Voltage (V)	Package Type	Speed (MHz)	Stepping[2]
SL3Z4 (MM#827856)[1]	1.55	256PBGA	133	B1
SL3Z5 (MM#827859)[1]	1.75	256PBGA	206	B1
GDS1110AB[1]	1.55	256PBGA	133	B2
GDS1110BB[1]	1.75	256PBGA	206	B2
GDS1110AC	1.55	256PBGA	133	B4
GDS1110BC	1.75	256PBGA	206	B4
GDS1110AD	1.55	256PBGA	133	B5
GDS1110BD	1.75	256PBGA	206	B5

NOTES:
1. This device can no longer be ordered.
2. This value may be read from the ID register Register 0

Errata

1. Incorrect Sign-Extended Value in Register After a Read Buffer Allocate

Problem: After a read buffer allocate, a Load Register Signed Halfword (LDRSH) or a Load Register Signed Byte (LDRSB) will not return the correct value in the register, due to long propagation delays in the sign extend logic.

Affected Step: A0, B0, B1, B2, B4, and B5

Workaround: Execute the command twice and the data is guaranteed to be correctly sign-extended for the second read.

Status: No Fix

2. LCD Ghost Lines

Problem: The SA-1110 LCD when driving a color passive display has diagonal ghost lines and flicker. These ghost lines are image dependent and are more evident with intensities 3 and 11.

Affected Step: A0, B0, B1, B2, B4, and B5

Workaround: None. There is a marked improvement by setting bits 11:10 in LCD Control Register 0 (Address 0h B010 0000) to 0x8. The actual setting of bits 11:10 should be experimented with to determine the best LCD performance.

Status: No Fix

3. High Current on VDDX During Reset

Problem: The SA-1110 exhibits high VDDX current under the scenario of power-on reset and hardware reset with subsequent VDD failure.

Affected Step: A0

Workaround: Use external logic to ensure that VDD powers up with VDDX and cannot be held low when hardware reset is asserted. In a typical application, this would require that VDD be enabled if either PWR_EN = 1 or nRESET = 0.

Status: Fixed

4. High Current on VDDX During Sleep

Problem: The SA-1110 exhibits high VDDX current (2.5 mA) during sleep.

Affected Step: A0

Workaround: None identified.

Status: Fixed

5. LCD State Machine Throughput Fails Using SDRAM at Full-Memory Clock Frequency

Problem: The LCD controller fails when the frame buffer is read from SDRAM that does burst transfers at the full-memory clock frequency (one-half CPU frequency). When using other memory types, which cannot burst at full-memory clock frequency, or using SDRAM at half-memory clock frequency (one-fourth CPU frequency), the LCD controller works correctly.

Affected Step: A0

Workaround: Set up SDRAM used for the LCD frame buffer to run at half-memory clock frequency.

Status: Fixed

6. USB Stalls When More Than One USB Client Is Present

Problem: When multiple USB clients are present, the USB stalls after the master completes a transmission to another device. The USB does not respond when the master addresses it.

Affected Step: A0

Workaround: Do not allow multiple clients on the USB bus.

Status: Fixed

7. SDRAM Auto-Power-Up Failure

Problem: If the memory controller is configured to allow SDRAM auto-power-down of minimum possible duration (SDCKE 1 low for exactly one and one-half memory clocks), the subsequent auto-power-up (SDCKE 1 goes high and appropriate SDCLK 2:1 starts running) may not work correctly.

Affected Step: A0

Workaround: For SDRAM transfers, increase RAS precharge time (MDCNFG:TRP2 or MDCNFG:TRP0) to be greater than or equal to 5. This forces the first SDRAM transfer following auto-power-up to be delayed, such that SDCKE 1 can be sampled high upon a rising edge of SDCLK 2:1 prior to sampling the next ACT command.

Status: Fixed

8. SDRAM RAS Precharge Counter May Not Work in the Presence of SMROM

Problem: Because SMROM does not require the use of the SA-1110's counter for minimum SDRAM RAS precharge time, this counter is overridden during SMROM transfers. The override logic does not consistently use upper address bits to distinguish between SDRAM and SMROM. Therefore, when like-numbered SMROM and SDRAM chip selects (for example, nCS 0 and nRAS/nSDCS 0) are enabled, the RAS precharge counter may not work for those SDRAM chip selects.

Affected Step: A0

Workaround: Avoid enabling like-numbered chip selects for SMROM and SDRAM. For example, enable SMROM only on nCS 1:0 and SDRAM only on nRAS/nSDCS 3:2.

Status: Fixed

9. DRAM Refresh Corrupting ROM/Flash Burst of 4/8 Timing

Problem: Asynchronous DRAM and SDRAM refreshes are allowed to interrupt burst transfers to any static, asynchronous memory type (ROM, SRAM, VLIO, or Flash) between 32-bit transfers. This works properly when any of those memory types are configured for non-burst timings (MCSx:RTx = 0 or 1). But when ROM/Flash is configured for burst timings (MSCx:RTx = 2 or 3), burst-of-4/8 aligned addresses may erroneously use the burst access time (MCSx:RDNx) rather than the intended non-burst access time (MSCx:RDFx). This happens when the refresh request (internally generated) occurs just prior to a burst-of-4/8 unaligned address. The problem affects burst-of-4 timings on either 16-bit or 32-bit data busses, or burst-of-8 timings on 16-bit busses.

Affected Step: A0 and B0

Workaround: Use non-burst timing (MSCx:RTx = 0) for ROM/Flash.

Status: Fixed

10. Data Contention Caused by Hardware, Software, or Watchdog Reset During SDRAM/SMROM Reads

Problem: If a SA-1110 hardware, software, or watchdog reset occurs while SDRAM/SMROM is executing a read command, the SA-1110 de-asserts all control pins: SDCKE 1:0, SDCLK 2:0, nCS 3:0, nRAS/nSDCS 3:0, nSDRAS, nSDCAS, nWE, nOE, and nCAS/DQM 3:0. This correctly prevents new commands from being started. But, because SDCKE 1:0 and SDCLK 2:0 are de-asserted within a few cycles of the last read command, that read may not complete. Instead, SDRAM/SMROM may continue to drive D 31:0 during reset assertion and after reset de-assertion: until a few cycles after SDCKE 1:0 and SDCLK 2:0 are asserted again and the final read data is driven. This continuous D 31:0 drive by SDRAM/SMROM may contend with read data from other memory devices or write data from the SA-1110 itself.

Affected Step: A0, B0, and B1

Workarounds (2) for Hardware Reset: Use the following workarounds for a hardware reset:

1. Do not use hardware reset after the initial power-on hardware reset.
2. During each assertion of the SA-1110's hardware reset pin (nRESET=0), temporarily remove power from SDRAM/SMROM VDD and VDDQ pins.

Workaround for Software Reset: Prior to executing a software reset, all outstanding SDRAM and SMROM transfers must be allowed to complete and the banks must be disabled via writes to the MDCNFG and SMCNFG registers.

1. If burst reads from SMROM are not already enabled, enable them without changing the number of row address bits, CAS latency, or RAS latency.
   a. Write MDCAS00, MDCAS01, and MDCAS02 with their present number of leads 1's, but filled through the 96th bit with the 2-bit repeating pattern of 0 followed by 1 (see Section 10.2.3.2 for explanation).
   b. Force a mode register set (MRS) command by writing SMCNFG with its present value. The MRS configures the SMROMs' internal mode registers for a burst length of eight.
2. If the instruction cache is not already enabled, enable it by setting bit 12 of the coprocessor 15 control register (see Chapter 5 and Chapter 6). This causes subsequent fetches to be performed as 8-word bursts.
3. Align the store instruction which alters SMCNFG to an 8-word address boundary. Locate the store instructions that alter MDCNFG and RSRR at the subsequent two addresses. Aligning these three instructions to the start of a cache line ensures that they are fetched together and executed prior to any other SMROM read.

Workaround for Watchdog Reset: Do not use watchdog reset. The combination of watchdog interrupt and software reset may be used instead of watchdog reset.

Status: Fixed

11. Erroneous SMROM Precharge All (PALL) Command with Mode Register Set (MRS) Command After Hardware, Software, Watchdog, or Sleep Reset

Problem: After any type of reset (hardware, software, watchdog, or sleep), an SMROM mode register set (MRS) command may be followed in less than three SDCLK cycles by an unnecessary SMROM precharge all (PALL) command. According to SMROM specifications, a minimum of three cycles is required between issue of MRS and any subsequent command. Issue of the unnecessary PALL command is dependent upon the precise timing of reset within the SDCLK cycle, and upon use of MDREFR:K0DB2=1.

Affected Step: A0, B0, and B1

Workaround: Confirm that SMROM are insensitive to the issue of unnecessary PALL commands that follow MRS commands by less than three SDCLK cycles.

Status: Fixed

12. UDC Not Responding to IN Packet After Receiving an SOF Packet

Problem: The host requests data from the UDC by sending an IN packet to Endpoint 2. The UDC must respond with a NAK signal if it does not currently have any data stored in the FIFO. Sporadically, the UDC does not respond with a NAK signal after an SOF packet is received.

Affected Step: A0, B0, and B1

Workaround: Connect a USB hub between the UDC and the host system.

Status: Fixed

13. Corruption of Internal Register Reads/Writes Following SDRAM/SDROM Reads

Problem: Reads and writes, from and to internal registers other than memory controller registers, can be corrupted if they immediately follow reads from SDRAM or SMROM, shown as follows:

1. Register reads immediately following reads from SDRAM on 16-bit data busses (MDCNFG:DWIDn=1), with SDCLK running at full memory clock frequency (MDREFR:KnDB2=0), and using delayed data latching.
2. Register reads/writes immediately following reads from SDRAM or SMROM on 32-bit data busses (MDCNFG:DWIDn=0), with SDCLK running at full memory clock frequency (MDREFR:KnDB2=0), and using non-delayed data latching*.

Note: See Section 10.2.3.2 of SA-1110 Developer's Manual for a description of delayed and non-delayed data latching. Delayed data latching must be used at high core clock frequencies (e.g.- 206MHz) and non-delayed data latching must be used at low core clock frequencies (e.g.- 100MHz).

Affected Step: A0, B0, and B1

Workaround: The following workaround applies:

1. For SDRAM on 16-bit data busses, use SDCLK running at half memory clock frequency (MDREFR:KnDB2=1)
2. For SDRAM or SMROM on 32-bit data busses, use either:
   - — a higher core clock frequency and delayed data latching, or;
   - — set the SDCLK to run at half memory clock frequency (MDREFR:KnDB2=1).

Status: Fixed

14. Failure on Sleep Request During Variable Latency I/O to Perform SDRAM Self-Refresh and Enter Sleep

Problem: If the memory controller receives a request to enter sleep mode during a variable latency I/O (VLIO) transfer, the SA-1110 may fail to put SDRAM into self-refresh (with SLFRSH command) and fail to enter sleep mode. In this case the corresponding VLIO chip select (nCS[3, 4, or 5]) and byte enables (nCAS/DQM[3:0]) may remain asserted indefinitely. This problem applies to sleep entry requests initiated by either software or a power supply fault.

Affected Step: A0, B0, B1, B2, Fixed on B4

Workaround: Initiate SDRAM self-refresh and sleep mode only by software, not BATT_FAULT=1 or VDD_FAULT=1 power supply fault. Prior to entering sleep disable CBR refresh, force all SDRAM into self-refresh, disable all SDRAM banks, clear self-refresh, and clear SDRAM clock enable. The following software sequence must be fully contained in the instruction cache before execution. Also, all sources of interrupt and DMA activity must be stopped before execution of the software sequence. After step 5 of this sequence is complete, BATT_FAULT=1 or VDD_FAULT=1 may be used to enter sleep (instead of step 6) and/or subsequently to maintain sleep mode.

1. Write Static Memory Control Register(s) to clear the RT field(s) (MSCx:RT = 0) for any bank(s) that were configured for VLIO.
2. Write the DRAM Refresh Control Register to clear the DRI field (MDREFR[15:4]=0), while maintaining all other bits at their current values.
3. Write the DRAM Refresh Control Register to set the SLFRSH bit (MDREFR[31] = 1), while maintaining all other bits at their current values.
4. Write the DRAM Configuration Register to clear the DE bits (MDCNFG[17,16,1,0] = 0): any or all other MDCNFG bits may also be cleared.
5. Write the DRAM Refresh Control Register to clear the SLFRSH bit (MDREFR[31] = 0), and clear the E1PIN bit (MDREFR[20] = 0), while maintaining all other bits at their current values
6. Write the Power Manager Control Register to set the SF bit (PMCR[0]=1).

Status: Fixed

15. Failure on Sleep Request During CBR Refreshes to Perform SDRAM Self-Refresh Prior to Entering Sleep

Problem: When the memory controller receives a request to enter sleep mode during a SDRAM/DRAM CBR refresh, the SA-1110 may fail to put SDRAM into self-refresh (with SLFRSH command) prior to entering sleep mode. Sleep mode is entered. This problem applies to sleep entry requests initiated by either software or a power supply fault.

Affected Step: A0, B0, B1, B2, Fixed on B4

Workaround: Initiate SDRAM self-refresh and sleep mode only by software, not BATT_FAULT=1 or VDD_FAULT=1 power supply fault. Prior to entering sleep disable CBR refresh, force all SDRAM into self-refresh, disable all SDRAM banks, clear self-refresh, and clear SDRAM clock enable. The following software sequence must be fully contained in the instruction cache before execution. Also, all sources of interrupt and DMA activity must be stopped before execution of the software sequence. After step 5 of this sequence is complete, BATT_FAULT=1 or VDD_FAULT=1 may be used to enter sleep (instead of step 6) and/or subsequently to maintain sleep mode.

1. Write Static Memory Control Register(s) to clear the RT field(s) (MSCx:RT = 0) for any bank(s) that were configured for VLIO.

2. Write the DRAM Refresh Control Register to clear the DRI field (MDREFR[15:4]=0), while maintaining all other bits at their current values.
3. Write the DRAM Refresh Control Register to set the SLFRSH bit (MDREFR[31] = 1), while maintaining all other bits at their current values.
4. Write the DRAM Configuration Register to clear the DE bits (MDCNFG[17,16,1,0] = 0): any or all other MDCNFG bits may also be cleared.
5. Write the DRAM Refresh Control Register to clear the SLFRSH bit (MDREFR[31] = 0), and clear the E1PIN bit (MDREFR[20] = 0), while maintaining all other bits at their current values
6. Write the Power Manager Control Register to set the SF bit (PMCR[0]=1).

Status: Fixed

16. Erroneous SDRAM Power-Down-Exit and Power-Down Following Self-Refresh and Sleep Entry

Problem: If the memory controller receives a request to enter sleep mode while any SDRAM banks are enabled, and SDRAM are properly put into self-refresh (with SLFRSH command), and sleep mode is properly entered, the SA-1110 may subsequently perform erroneous SDRAM Power-Down-Exit (PWRDNX) and Power-Down (PWRDN) commands. The PWRDNX command erroneously takes SDRAM out of self-refresh. The PWRDN command returns SDRAM to a low power state, but leaves it without CBR or self-refresh throughout sleep. This problem applies to sleep entry requests initiated by either software or a power supply fault.

Affected Step: B2, Fixed on B4

Workaround: Initiate SDRAM self-refresh and sleep mode only by software, not BATT_FAULT=1 or VDD_FAULT=1 power supply fault. Prior to entering sleep disable CBR refresh, force all SDRAM into self-refresh, disable all SDRAM banks, clear self-refresh, and clear SDRAM clock enable. The following software sequence must be fully contained in the instruction cache before execution. Also, all sources of interrupt and DMA activity must be stopped before execution of the software sequence. After step 5 of this sequence is complete, BATT_FAULT=1 or VDD_FAULT=1 may be used to enter sleep (instead of step 6) and/or subsequently to maintain sleep mode.

1. Write Static Memory Control Register(s) to clear the RT field(s) (MSCx:RT = 0) for any bank(s) that were configured for VLIO.
2. Write the DRAM Refresh Control Register to clear the DRI field (MDREFR[15:4]=0), while maintaining all other bits at their current values.
3. Write the DRAM Refresh Control Register to set the SLFRSH bit (MDREFR[31] = 1), while maintaining all other bits at their current values.
4. Write the DRAM Configuration Register to clear the DE bits (MDCNFG[17,16,1,0] = 0): any or all other MDCNFG bits may also be cleared.
5. Write the DRAM Refresh Control Register to clear the SLFRSH bit (MDREFR[31] = 0), and clear the E1PIN bit (MDREFR[20] = 0), while maintaining all other bits at their current values.
6. Write the Power Manager Control Register to set the SF bit (PMCR[0]=1).

Status: Fixed

17. Corruption of Internal Register Reads/Writes Following Reads from SDRAM on 16-bit Data Busses at Full Memory Clock Frequency

Problem: If a read from SDRAM on a 16-bit data bus (MDCNFG:DWID0=1 or MDCNFG:DWID2=1) running at full memory clock frequency (MDREFR:K1DB2=0 or MDREFR:K2DB2=0, respectively) is immediately followed by a core read/write from/to an internal register other than memory controller registers, the register read/write data may be corrupted.

Affected Step: A0, B0, B1, B2, B4, and B5

Workaround: Configure all SDRAM for 32-bit data busses (MDCNFG:DWID0=MDCNFG:DWID2=0) or configure all SDRAM to run at half-memory clock frequency (MDREFR:K1DB2=MDREFR:K2DB2=1).

Status: No Fix

18. Failure on Sleep Request During SDRAM Read/Write Bursts to Precharge SDRAM Row Prior to Performing SDRAM Self-Refresh and Entering Sleep

Problem: When the memory controller receives a request to enter sleep mode during a burst read or write with SDRAM, the SA-1110 may fail to precharge the currently active SDRAM row prior to putting SDRAM into self-refresh (with SLFRSH command) and entering sleep mode. Because it is an illegal SDRAM operation to attempt self-refresh while a row is active, the resulting SDRAM behavior is indeterminate. However, the SA-1110 enters sleep mode. This problem applies to sleep entry requests initiated by either software or a power supply fault.

Affected Step: A0, B0, B1, B2, Fixed on B4

Workaround: Initiate SDRAM self-refresh and sleep mode only by software, not BATT_FAULT=1 or VDD_FAULT=1 power supply fault. Prior to entering sleep disable CBR refresh, force all SDRAM into self-refresh, disable all SDRAM banks, clear self-refresh, and clear SDRAM clock enable. The following software sequence must be fully contained in the instruction cache before execution. Also, all sources of interrupt and DMA activity must be stopped before execution of the software sequence. After step 5 of this sequence is complete, BATT_FAULT=1 or VDD_FAULT=1 may be used to enter sleep (instead of step 6) and/or subsequently to maintain sleep mode.

1. Write Static Memory Control Register(s) to clear the RT field(s) (MSCx:RT = 0) for any bank(s) that were configured for VLIO.
2. Write the DRAM Refresh Control Register to clear the DRI field (MDREFR[15:4]=0), while maintaining all other bits at their current values.
3. Write the DRAM Refresh Control Register to set the SLFRSH bit (MDREFR[31] = 1), while maintaining all other bits at their current values.
4. Write the DRAM Configuration Register to clear the DE bits (MDCNFG[17,16,1,0] = 0): any or all other MDCNFG bits may also be cleared.
5. Write the DRAM Refresh Control Register to clear the SLFRSH bit (MDREFR[31] = 0), and clear the E1PIN bit (MDREFR[20] = 0), while maintaining all other bits at their current values
6. Write the Power Manager Control Register to set the SF bit (PMCR[0]=1).

Status: Fixed

19. Failure to Reset UDC OUT Data Packet Toggle Checking to DATA0 on Endpoint 1 After a Sequence of Setting/Clearing Force Stall Bit (UDCCS1:FST) and Clearing Sent Stall Bit (UDCCS1:SST)

Problem: When the UDC receives a command from the host (for example the ClearFeature(HALT) command) which requires the endpoint to reset its data packet toggle flag to DATA0 so that when

the host sends the next data packet to Endpoint 1, the UDC should expect the data packet to be of type DATA0. The UDC fails to reset its data packet toggle flag to DATA0 (and actually leaves it in its current state) after executing the proper sequence of setting the Force Stall Bit (UDCCS1:FST), clearing the Force Stall Bit, and then clearing the Sent Stall Bit (UDCCS1:SST).

Affected Step: A0, B0, B1, B2, Fixed on B4

Workaround: None.

Status: Fixed

20. Failure to Reset UDC IN Data Packet Toggle Generation to DATA0 on Endpoint 2 After a Sequence of Setting/Clearing Force Stall Bit (UDCCS2:FST) and Clearing Sent Stall Bit (UDCCS2:SST)

Problem: When the UDC receives a command from the host (for example the ClearFeature(HALT) command), it requires the endpoint to reset its data packet toggle flag to DATA0. Therefore, the next data packet sent from Endpoint 2 to the host, must be of type DATA0. The UDC fails to reset its data packet toggle flag to DATA0 (and actually sets it to DATA1) after executing the proper sequence of setting the Force Stall Bit (UDCCS2:FST), clearing the Force Stall Bit, and then clearing the Sent Stall Bit (UDCCS2:SST).

Affected Step: A0, B0, B1, Fixed on B4

Workaround: None.

Status: Fixed

21. Failure of Synchronous Serial Port (SSP) Receiver Overrun Status Bit to Generate Interrupt Request

Problem: Non-maskable interrupt is not generated when the Receiver Overrun (ROR) status bit is set in the SSP status register. In addition, the ROR bit is set when data is placed in the ninth entry of the 12-entry receive FIFO.

Affected Step: A0, B0, B1, B2, B4, and B5

Workaround: The SSP Status Register ROR bit can be polled to determine if a receiver overrun has occurred. Software must detect if there was missing data due to an overrun. This can be accomplished by methods such as counting data packets, or adding a CRC packet, or implementing a checksum algorithm.

Status: Eval

22. LCD Controller Fails to Operate Correctly Following Reconfiguration

Problem: If the LCD Controller is configured and enabled following a reset event, and is subsequently disabled and reconfigured for different display characteristics, unpredictable behavior may result when the LCD controller is re-enabled.

Affected Step: A0, B0, B1, B2, B4, and B5

Workaround: Configure and enable the LCD Controller only one time after a reset event.

Status: No Fix

23. Misaligned Word Accesses with 16-Bit Data Bus May Produce Incorrect Data

Problem: If a misaligned word (32-bit) access is attempted with the data bus configured for 16-bit operation, address bus bit 1 does not toggle as required to support the access. Additionally, the data bytes being transferred may be erroneously swapped.

Affected Step: A0, B0, B1, B2, B4, and B5

Workaround: Do not configure SA-1110 for operation with 16-bit data bus.

Status: No Fix

24. Software Sleep Status Bit (PSSR:SSS) May Be Improperly Set After Sleep Wakeup

Problem: The software sleep status bit (PSSR:SSS) may inadvertently be set after sleep wakeup, even though the part was not put into sleep mode by setting the force sleep (PMCR:SF) bit.

Affected Step: A0, B0, B1, B2, B4, and B5

Workaround: Use a bit in the PWER registers as a substitute for the PSSR:SSS bit. You must choose a bit in PWER that corresponds to a bit set as an output in the GPDR in the application system. For example, if you use bit 5 of PWER as a flag to indicate whether the part went to sleep via software or hardware, then define PWER[5]=1 to mean that the part went to sleep via software. If you boot from a hard reset (RCSR:HWR = 1), ignore PWER[5]. When you are going to sleep via software, then the last thing to do before setting PMCR:SF bit, is to set PWER[5]=1. When the part wakes up, if RCSR:SMR bit is set (sleep mode reset), then read the PWER[5] bit to see if it was in sleep due to software (= 1) or not (= 0). This bit in the PWER register is now a substitute for the PSSR:SSS bit.

Status: No Fix

25. Improper Operation of LCD Controller LCCR2 Register EFW (End of Frame Line Clock Wait Count)

Problem: When the SA-1110's LCCR2: EFW (End of Frame Line Clock Wait Count) is **not** zero, LCCR1: ELW (End of Line Pixel Clock Wait Count) is mistakenly loaded into the End of Frame Wait Counter.

Affected Step: A0, B0, B1, B2, B4, and B5

Workaround: Always program LCCR2: EFW to zero. Use LCCR2: BFW (Beginning of Frame Line Clock Wait Count) to delay the next frame.

Status: Eval

26. Between Two Successive PCMCIA Accesses, Bus Arbiter Might Not Recognize Pending, Highest-Priority, Bus Access Request From LCD Controller

Problem: Between two successive accesses to the SA-1110's PCMCIA Interface, the Bus Arbiter might not recognize a pending, highest-priority request from the LCD Controller and, therefore, the LCD Controller is not granted bus access as it should be.

Affected Step: A0, B0, B1, B2, B4, and B5

Workaround: To unlock the Bus Arbiter, follow the PCMCIA access with a "dummy" store-to or load-from uncached/unbuffered memory space.

Status: Eval

27. Incorrect Values Are Read from RTTR and RCNR Registers Immediately After They Are Written

Problem: A read back of the RTTR or RCNR register immediately after a load of the RTTR or RCNR register does not read back the loaded value. This is caused by a long propagation delay through the read back logic.

Affected Step: A0, B0, B1, B2, B4, and B5

Workaround: At least a 32 µsec delay is needed for the values to propagate through the RTC logic before the stored value can be read back correctly. You may generate this delay by performing multiple reads, but only using the result of the last read.

Status: No fix.

28. Incorrect Address Decode in USB Controller

Problem: Generally, SA-1110 USB functionality is limited to a USB bus with a maximum of two USB devices, this bus would include the SA-1110 USB device. Alternately, there may be three or more USB devices on the bus if the SA-1110 USB device is assigned address 0x4. The following paragraphs explain in detail this environment.

The SA-1110 USB controller may incorrectly decode an address on the bus causing one of these problems:

1. USB Port responds to the wrong address
2. USB Port accepts data to the wrong address
3. Port may freeze because of various address and endpoint combinations on the bus

SA-1110 USB Port Responds to the Wrong Address

There are two conditions where the SA-1110 USB Port responds to an incorrect address:

1. Three or more devices and hubs in a system when the SA-1110 device is assigned to address 0x4
2. Three or more devices in a system when the SA-1110 device is assigned to an address other than 0x4

The SA-1110 USB functions properly when it is the only device in a system or with only one other device. In this case the SA-1110 USB device did not fail in laboratory tests. The following paragraphs explain what happens when an SA-1110 USB device is in a system with two or more other USB devices.

If an SA-1110 device is assigned to address 0x4, the error was not duplicated in the lab. However, if these conditions occur:

- An installed SA-1110 USB device is disconnected from your system,
- Another USB device is connected, and
- The SA-1110 USB device is re-connected,

Then the SA-1110 USB device will fail because it is no longer assigned to address 0x4.

After the SA-1110 USB device is disconnected, the host frees-up address 0x4 and it is assigned to the next device plugged into the system. If the SA-1110 device is simply disconnected and re-connected without disconnecting or connecting any other USB devices, the host again assigns address 0x4 to the SA-1110 device and the error does not occur.

If the SA-1110 USB device is not assigned to address 0x4, an error will occur. If the SA-1110 USB device is connected after address 0x4 has been assigned to another USB device, the failure occurs immediately. If the SA-1110 USB device is connected before address 0x4 has been assigned, no failure occurs unless the SA-1110 USB device is disconnected and re-connected. Hence, the major problem is when another device is assigned to address 0x4 in a system before the SA-1110 device is assigned an address.

Other address and endpoint combinations cause the SA-1110 USB device to incorrectly respond, thereby causing contention on the USB Bus. The table below shows some of the more likely combinations that cause an incorrect response. If the SA-1110 USB device is assigned to the address in the SA-1110 Device column and there is an access to the address and endpoint combination shown in the Other Devices column, the SA-1110 USB device incorrectly responds.

Other SA-1110 Erroneous Response Cases

Other Devices			SA-1110 Device	
Address	**Endpoint**	**crc**	**address**	**endpoint**
0x0F	0x0	0x03	0x00	0x1
0x04	0x0	0x05	0x00	0x2
0x0B	0x0	0x04	0x00	0x2
0x02	0x1	0x03	0x08	0x1
0x0D	0x1	0x02	0x08	0x1
0x06	0x1	0x04	0x08	0x2
0x09	0x1	0x05	0x08	0x2

USB Port Accepts Data to the Wrong Address

A few cases exist where the SA-1110 USB device incorrectly decodes an address and incorrectly accepts data that was intended for another USB device. This error only occurs during an OUT transaction, and could cause data corruption to the SA-1110 USB device. All of these cases occur when a particular address, endpoint, and CRC combination is incorrectly compared (by the SA-1110 USB) to the address assigned to the SA-1110 USB device and endpoint 0x1. The table below shows some of the address, endpoint, and CRC combinations that cause this error.

Some Addresses that cause the SA-1110 to Accept Bad Data

Other Devices			SA-1110 Device	
Address	**Endpoint**	**crc**	**address**	**endpoint**
0x02	0x1	0x03	0x08	0x1
0x0D	0x1	0x02	0x08	0x1
0x0F	0x0	0x03	0x00	0x1

The first two rows in the table above occur only with 16 or fewer devices in a system and where the SA-1110 USB device is assigned to address 0x8 and an OUT transaction occurs to address 0x2 or address 0xD at endpoint 0x1. The third row in the table above occurs only if 15 or more devices and hubs are in a system and where an OUT transaction occurs to address 0xF at endpoint 0 while the SA-1110 USB device has just been reset and does not yet have an address assigned. While these cases are rare and depend on the number of devices in the system as well as the type of transaction and the address being accessed, the error occurs if these conditions are met.

The SA-1110 USB Controller Freezes and Recovers

As with condition 1 and 2, condition 2 occurs when the SA-1110 USB device incorrectly decodes an address. In this case, however, the decode does not include an endpoint for the SA-1110 USB device. When this happens the SA-1110 USB device does not try to respond, rather it freezes while

waiting for more data to decode for a valid endpoint. This error, while frequently occurring, recovers as soon as a valid address, endpoint, and CRC combination are seen on the bus. The table below shows all of the combinations that cause the SA-1110 USB device to freeze when as many as 16 USB devices are in a system.

Addresses That Cause the SA-1110 USB Controller to Freeze

Other Devices			SA-1110 Device
address	endpoint	crc	address
0x04	0x2	0x00	0x00
0x09	0x3	0x00	0x00
0x03	0x4	0x00	0x01
0x0E	0x5	0x00	0x01
0x00	0x9	0x00	0x02
0x0D	0x8	0x00	0x02
0x07	0xF	0x00	0x03
0x0A	0xE	0x00	0x03
0x06	0x3	0x01	0x04
0x0B	0x2	0x01	0x04
0x01	0x5	0x01	0x05
0x0C	0x4	0x01	0x05
0x02	0x8	0x01	0x06
0x0F	0x9	0x01	0x06
0x05	0xE	0x01	0x07
0x08	0xF	0x01	0x07
0x00	0x0	0x02	0x08
0x0D	0x1	0x02	0x08
0x07	0x6	0x02	0x09
0x0A	0x7	0x02	0x09
0x04	0xB	0x02	0x0A
0x09	0xA	0x02	0x0A
0x03	0xD	0x02	0x0B
0x0E	0xC	0x02	0x0B
0x02	0x1	0x03	0x0C
0x0F	0x0	0x03	0x0C
0x05	0x7	0x03	0x0D
0x08	0x6	0x03	0x0D
0x06	0xA	0x03	0x0E
0x0B	0xB	0x03	0x0E
0x01	0xC	0x03	0x0F
0x0C	0xD	0x03	0x0F

While laboratory tests have shown this error will recover, it has not been fully characterized. It is suspected that either an SOF or EOP for another USB device causes the SA-1110 USB device to recover. However, in some cases an ACK to another address also helped the SA-1110 USB device recover. Since a wide variety of circumstances caused the SA-1110 USB device to easily recover, thorough testing was not done to find all recovery cases.

Affected Step: A0, B0, B1, B2, and B4

Workaround: None

Status: Fixed in B5

29. USB Controller Endpoint 2 (IN) Transmits Incorrect Data

Problem: If the SA-1110 system uses so much memory bandwidth that the USB transmit FIFO can underrun, the USB controller may transmit incorrect data to the host with no indication an error occurred. During normal operation, the USB controller requests data be put into the Endpoint 2 FIFO. This data is then transmitted to the host after the host sends an IN command. Between the core or DMA putting a data byte into the transmit FIFO and the serial shifter beginning a byte transmission, the SA-1110 can transmit an old byte. There is no indication an underrun or CRC error occurred during this transfer. This condition causes the host to use corrupt data without the USB controller or the host reporting an error. Using a checksum on the entire data transfer is only software recovery from this condition.

Affected Step: A0, B0, B1, B2, and B4

Workaround: To prevent the FIFO from being starved for data, allow enough bandwidth in the system for the core or DMA to service the USB endpoint 2 FIFO.

Alternatively, a software checksum can be used for the entire data transfer to indicate any incorrect data that may have been transferred.

Status: Fixed in B5 – To activate the fix you must set UDCCR Bit-7 to one each time that the SA-1110 is booted, i.e., you must add this fix to the SA-1110's USB initialization code.

Note: UDCCR Bit-7 is "reserved" in A0, B0, B1, B2, B4.

Specification Changes

1. SDLC Feature

The SDLC feature is not available in this release of the product.

2. SDLC Feature Not Supported

Effective January 2000, the SDLC feature is not supported by the SA-1110 device.

3. Modifications in SDRAM/SMROM Data Input Hold Time

Table 13-3 of the *Intel StrongARM SA-1110 Microprocessor Developer's Manual* and its underlying Note 1 have been changed. Specifically, the Tsdih guidelines for 133 MHz SA-1110 microprocessors using SDRAM or SMROM at 66 MHz have changed. Also, the Tsdih guidelines for 206 MHz SA-1110 microprocessors using SDRAM or SMROM at frequencies less than 103 MHz have also been changed.

Most significantly, for 133 MHz SA-1110 microprocessors with a 66 MHz SDRAM/SMROM clock, the specified read data latching mode has changed from delayed to non-delayed. The MDCASxx registers need to be programmed accordingly. Also, the Table 13-3 Note 2 technique of serpentine SDCLK routing delay must not be used with 133 MHz SA-1110 microprocessors.

For 206 MHz SA-1110 microprocessors using an SDRAM/SMROM clock frequency of less than 103 MHz, there are four options:

- Confirm that the system design satisfies the new Tsdih guidelines (see Table 13-3).
- Carefully use the Table 13-3 Note 2 technique to adjust the system design so that it satisfies the new Tsdih guidelines.
- Set MDREFR:KnDB2=1 to divide the SDRAM/SMROM clock frequency by two and automatically use non-delayed read data latching.
- Change the CPU frequency such that the new Tsdih guidelines are satisfied at the non-divided SDRAM/SMROM clock frequency.

4. DC Operating Conditions: Section 12.2

The new parameters for Table 12-2:

- Changed the Minimum for Vihc from 0.8 X VDDX to 2.4
- Removed 1 from ESD Nominal
- Added 1000 V to ESD Maximum

5. Power Supply Voltages and Currents: Section 12.3

The new parameters for the AC and AD version of the device are:

- Maximum Run Mode Power changed from TBD to 500 mW
- Typical Run Mode Power changed from 240 mW to 200 mW
- Maximum Idle Mode Power changed from TBD to 100 mW

- Maximum Sleep Mode Current changed from 65 to 75 uA

The new parameters for the BC and BD version of the device are:

- Maximum Run Mode Power changed from TBD to 1000 mW
- Typical Run Mode Power changed from 400 mW to 350 mW
- Maximum Idle Mode Power changed from TBD to 200 mW
- Vddi Max changed from 1.93 V to 2.10 V
- Vddi Min changed from 1.58 V to 1.65 V

Specification Clarifications

None for this revision of this specification update.

Documentation Changes

1. GPCLK Control Register 1: Section 11.9.3

Add the following Note just under the second paragraph of this subsection:

Note: A question mark (?) signifies that the Reset value of that bit is undefined when the processor has completed its reset cycle.

2. HSSP Data Register: Section 11.10.9

Add the following Note at the end of the fourth paragraph of this subsection:

Note: A question mark (?) signifies that the Reset value of that bit is undefined when the processor has completed its reset cycle.

3. Receiver Overrun Flag (ROR) (read-only, noninterruptible): Section 11.11.8.6

Add the following Note just under the second paragraph of this subsection:

Note: A question mark (?) signifies that the Reset value of that bit is undefined when the processor has completed its reset cycle.

4. External Clock Prescaler (ECP): Section 11.12.3.11

Add the following Note just under the second paragraph of this subsection:

Note: A question mark (?) signifies that the Reset value of that bit is undefined when the processor has completed its reset cycle.

Replace table header with the following:

"MCP Control Register 0: MCCR0"

In the table, Bits 16–23 are replicated twice; once on page 11-138 and on page 11-139. Delete page 11-139.

5. USB Operation: Section 11.8

Change footnote on this page to:

"Access the most recent revision of the Universal Serial Bus Specification via the World Wide Web at http://www.usb.org/."

6. Packet Formats: Section 11.8.1.5

Replace the paragraph just above Figure 11-17 with the following:

"A start–of–frame (SOF) is a special type of token packet that is issued by the host once every 1 ms. The SOF packets consist of a sync, a PID, a frame number (which is incremented after each frame is transmitted), and a CRC5 field, as shown in Figure 11-17. Even though the UDC on the SA-1110 does not make use of the frame number field, the presence of the SOF packets every 1ms prevents the UDC from entering suspend mode."

Replace Figure 11-17 figure title with the following:

"SOF Token Packet Format"

Replace the paragraph just above Figure 11-18 with the following:

"Data packets follow token packets, and are used to transmit data between the host and UDC. The two types of data packets as specified by the PID are: DATA0 and DATA1. These two types provide a mechanism to guarantee data sequence synchronization between the transmitter and receiver across multiple transactions. During the handshake phase, both communicate and agree which data token type to transmit first. For each subsequent packet transmitted, the data packet type is toggled (DATA0, DATA1, DATA0, and so on). A data packet consists of a sync, a PID, from 0 to 256 bytes of data, and a CRC16 field, as shown in the Figure 11-18."

Replace Figure 11-18 with the following:

8 bits	8 bits	0–256 bytes	16 bits
Sync	PID	Data	CRC16

7. UDC Data Register: Section 11.8.12

Replace the text for this section with the following:

"The UDC data register (UDCDR) is an 8–bit register corresponding to both the top and bottom entries of the transmit and receive FIFOs, respectively. The UDC receive logic places data into the top of the receive FIFO. The data is transferred down the FIFO to the lowest location that is empty. When the UDCDR is read, the bottom entry of the 8-bit receive FIFO is accessed. After the read, the bottom FIFO entry is invalidated. This causes all FIFO data to automatically transfer down one location.

When the UDCDR is written, the topmost 8-bit transmit FIFO entry is accessed. After a write, the data is automatically transferred down the FIFO to the lowest available location. The UDC transmit logic:

- acquires 8-bit data values from the bottom of the transmit FIFO, one at a time;
- places the data into a serial shifter;
- and transmits this data out via the UDC pins.

Each time a data value is taken from the bottom FIFO entry, the location is invalidated. This causes all data in the FIFO to automatically transfer down one location.

The following table shows the location of the top and bottom of the transmit and receive FIFOs in the UDC data register. Both FIFOs are cleared when the SA-1110 is reset, when zero is written to the UDE, and when the UDD is written to one. After either of these actions takes place, prime the transmit FIFO by writing up to sixteen 8-bit values to the UDCDR before enabling the UDC."

Replace the address header at the top of the table with the following:

"0h80000028"

8. Bit 2 Reserved: Section 11.8.3.3

Change this entire section (including title) to the following:

"Section 11.8.3.3 Resume Interrupt Mask (RESIM)

The resume interrupt mask (RESIM) bit masks or enables the resume interrupt request.

- When RESIM=1, the interrupt is masked. The RESIR bit in the Status/Interrupt Register cannot be set.
- When RESIM=0, the interrupt is enabled. Whenever a resume condition occurs, the RESIR bit is set.

A resume condition occurs after a suspend condition has occurred. A write of a 1 and then a write of a 0 to this bit resets the internal suspend state machine in order that future resume conditions are recognized.

Note: Programming RESIM=1 does not affect the current state of RESIR. It serves only to block future zero–to–one transitions of RESIR.

9. Suspend/Resume Interrupt Mask (SRM): Section 11.8.3.7

Change this entire section (including title) to the following:

"Section 11.8.3.7 Suspend Interrupt Mask (SUSIM)

The suspend interrupt mask (SUSIM) bit masks or enables the suspend interrupt request.

- When SUSIM=1, the interrupt is masked, and the SUSIR bit in the Status/Interrupt Register cannot be set.
- When SUSIM=0, the interrupt is enabled, and whenever a suspend condition occurs, the SUSIR bit is set.

Note: Programming SUSM=1 does not affect the current state of SUSIR. It serves only to block future zero–to–one transitions of SUSIR."

10. Data Cache: Section 1.4.5

The third sentence in the second paragraph has been changed and now appears as follows:

Unlike the main data cache, the minicache implements a least-recently-used (LRU) replacement algorithm.

11. Memory Map: Section 2.4

Added this note to the first and second bullets:

Note: The upper 64MBytes of each 128MByte static bank select cannot be accessed because only 26 bits of the physical address are available on external pins. Attempts to accesses any static bank selects upper 64Mbyte will actually cause an access to that bank selects lower 64MByte, because the missing (27th) physical address bit is ignored.

Added this note below Figure 2-3:

Note: The upper 64MBytes of each 128MByte static bank select cannot be accessed because only 26 bits of the physical address are available on external pins. Attempts to accesses any static bank selects

upper 64Mbyte will actually cause an access to that bank selects lower 64MByte, because the missing (27th) physical address bit is ignored.

12. Coprocessors: Section 3.3

Add this note to the end of section 3.3:

Note: The write buffer must be flushed prior to loading the read buffer in order to maintain coherency between the two buffers. But, if user-mode MCR access is enabled for the read buffer and the flush is attempted while in user mode, an undefined instruction exception will occur. In this case, the exception handler must perform the write buffer flush, then return to user mode to execute the read buffer load. Alternatively, an SWI instruction can be used as a service call to flush the write buffer.

13. *Internal Coprocessor Instructions*: Section 5.1

Add this note after the first paragraph of section 5.1:

Note: The write buffer must be flushed prior to loading the read buffer in order to maintain coherency between the two buffers. But, if user-mode MCR access is enabled for the read buffer and the flush is attempted while in user mode, an undefined instruction exception will occur. In this case, the exception handler must perform the write buffer flush, then return to user mode to execute the read buffer load. Alternatively, an SWI instruction can be used as a service call to flush the write buffer.

14. Register 7 – Cache Control Operations: Section 5.2.8

Add this note to the end of section 5.2.8:

Note: The write buffer must be flushed prior to loading the read buffer in order to maintain coherency between the two buffers. But, if user-mode MCR access is enabled for the read buffer and the flush is attempted while in user mode, an undefined instruction exception will occur. In this case, the exception handler must perform the write buffer flush, then return to user mode to execute the read buffer load. Alternatively, an SWI instruction can be used as a service call to flush the write buffer.

15. Register 9 – Read-Buffer Operations: Section 5.2.10

Add this note to the end of section 5.2.10:

Note: The write buffer must be flushed prior to loading the read buffer in order to maintain coherency between the two buffers. But, if user-mode MCR access is enabled for the read buffer and the flush is attempted while in user mode, an undefined instruction exception will occur. In this case, the exception handler must perform the write buffer flush, then return to user mode to execute the read buffer load. Alternatively, an SWI instruction can be used as a service call to flush the write buffer.

16. Register 14 – Debug Support (Breakpoints): Section 5.2.13

Added a paragraph immediately preceding the Data Breakpoint Control Register table. The paragraph now appears as follows:

The DBAR, DBVR, DBMR and DBCR registers are Read/Write registers. The IBCR is a Write-Only register.

17. Data Caches (Dcaches): Section 6.2

Removed the second to last sentence in the first paragraph, which was: “Replacements in the minicache use the same round-robin pointer mechanism as in the main data cache.” Changed the last sentence in the first paragraph. The first paragraph now appears as follows:

The SA-1110 contains two logically separate data caches: the main data cache and the mini data cache (or minicache). The main data cache, an 8 Kbyte write-back Dcache, has 256 lines of 32 bytes (8words) in a 32-way set-associative organization. It is intended for use during most data accesses. This cache allocates on loads to spaces marked B=1 and C=1. Replacements in the main data cache are selected according to a set of round-robin pointers. At reset, the pointer in each block of the Dcache points to way zero of each 32-way block. As lines are allocated, the pointers are incremented to the next way of the set. After way 31 is allocated, the next line fill replaces (and copies back to memory, if dirty) the data in way zero. The minicache is a 512-byte write-back cache. It has 16 lines of 32 bytes (8 words) in a two-way set-associative organization and provides an alternate caching structure for dealing with large data structures that could thrash the main data cache. This cache allocates on loads to spaces marked B=0 and C=1. Unlike the main data cache, the minicache implements a least-recently-used (LRU) replacement algorithm.

18. Writes to a Bufferable and Noncacheable Location (B=1,C=0): Section 6.3.2.2

The second sentence has been changed and a fourth sentence has been added. This section now appears as follows:

If the write buffer is enabled and the processor performs a write to a bufferable but noncacheable location and misses in the Dcaches, the data is placed in the write buffer and the CPU continues execution. The write buffer performs the external write sometime later. Store multiples are **not** merged in the write buffer when B = 1, C = 0.

19. Unbufferable and Noncacheable Writes (B=0, C=0): Section 6.3.2.3

Renamed this section title from: Unbufferable Writes (B=0).

20. Writes to a Non-Bufferable and Cacheable Location (B=0, C=1): Section 6.3.2.4

Section 6.3.2.4 added. The paragraph for this section appears as follows:

When store multiples occur to a page that is cacheable but not buffereable (B=0,C=1), the write data will be merged into the write buffer and burst writes will occur to memory.

21. Read Buffer (RB): Section 6.4

Changed the third sentence in the first paragraph. The paragraph now appears as follows:

The SA-1110 contains a software-programmable read buffer that can increase the performance of critical loop code by prefetching data. The RB enables the preallocation of read-only data into one of four 32-byte buffers without stalling the pipe. For subsequent loads that hit in the RB, data is sourced from the buffer instead of the Dcaches at a rate of 1 word per core clock (as long as the load address hits in the TLB of the DMMU). Also, because the programmer specifies which entry of the RB is used, critical data can be “locked” in to eliminate bus latency.

22. Read Buffer: Section 6.4

The third sentence in the fifth paragraph has been changed and now appears as follows:

It is possible for a portion of a cache block at a given virtual address to be contained in one RB entry while another portion of the same block is contained in another RB entry.

23. Read Buffer: Section 6.4

Add the following note to the end of this section:

Note: The Write Buffer must be drained before attempting to load the Read Buffer.

24. Read Buffer: Section 6.4

Replace the note at the end of section 6.4 with:

Note: The write buffer must be flushed prior to loading the read buffer in order to maintain coherency between the two buffers. But, if user-mode MCR access is enabled for the read buffer and the flush is attempted while in user mode, an undefined instruction exception will occur. In this case, the exception handler must perform the write buffer flush, then return to user mode to execute the read buffer load. Alternatively, an SWI instruction can be used as a service call to flush the write buffer.

25. Data Aborts: Section 7.3

Changed first paragraph. It now reads as:

The SA-1110 takes a data abort exception due to: MMU-generated exceptions, accessing reserved memory space.

26. GPIO Pin Output Set Register (GPSR) and Pin Output Clear Register (GPCR): Section 9.1.1.3

Changed the reset values for the GPIO Pin Output Set and Clear Registers (GPSR and GPCR) from undefined to ?. The word Reset was added to the left column in the row that indicates the reset value.

0h 9004 0008 **GPSR** **Write-Only**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				PS27	PS26	PS25	PS24	PS23	PS22	PS21	PS20	PS19	PS18	PS17	PS16	PS15	PS14	PS13	PS12	PS11	PS10	PS9	PS8	PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0
Reset	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description
n	PSn	GPIO output pin set n (where n = 0 through 27). 0 – Pin level unaffected. 1 – If pin configured as an output, set pin level high (one).
31..28	—	Reserved

0h 9004 000C **GPCR** **Write-Only**

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved				**PC27**	**PC26**	**PC25**	**PC24**	**PC23**	**PC22**	**PC21**	**PC20**	**PC19**	**PC18**	**PC17**	**PC16**	**PC15**	**PC14**	**PC13**	**PC12**	**PC11**	**PC10**	**PC9**	**PC8**	**PC7**	**PC6**	**PC5**	**PC4**	**PC3**	**PC2**	**PC1**	**PC0**
Reset	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

Bits	Name	Description
n	PCn	GPIO output pin clear n (where n = 0 through 27). 0 – Pin level unaffected. 1 – If pin configured as an output, clear pin level low (zero).
31..28	—	Reserved

27. GPIO Alternate Functions: Section 9.1.2

In row GPIO 19 in the Unit column, modify the contents to be Serial Port 4: SSP. This row now appears as follows:

Pin	Alternate Function	Direction	Unit	Signal Description
GP 19	SSP_CLK	Input	Serial port **4**:SSP	Sample clock input

28. Interrupt Controller: Section 9.2

Added the second sentence to the second paragraph, as follows:

The first level of the structure, represented by the interrupt controller IRQ pending register (ICIP) and the interrupt controller FIQ pending register (ICFP) contain the all-enabled and unmasked interrupt sources. The interrupt controller pending register (ICPR) shows both IRQ and FIQ pending interrupts. Interrupts are enabled at their source and unmasked in the interrupt controller mask register (ICMR). The ICIP contains the interrupts that are programmed to generate an IRQ interrupt. The ICFP contains all valid interrupts that are programmed to generate an FIQ interrupt. This routing is programmed via the interrupt controller level register (ICLR).

Made the following changes to Figure 9-2.

Changed Interrupt Level Register to Interrupt Controller Level Register (ICLR)

Changed Interrupt Mask Register to Interrupt Controller Mask Register (ICMR)

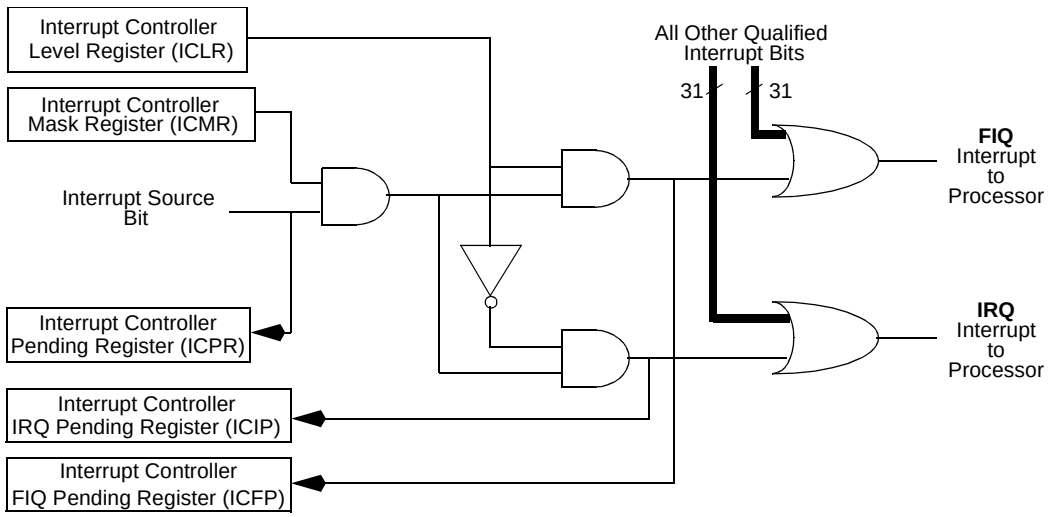
Changed Interrupt Pending Register to Interrupt Controller Pending Register (ICPR)

Changed IRQ Interrupt Pending Register to Interrupt Controller IRQ Pending Register (ICIP)

Changed FIQ Interrupt Pending Register to Interrupt Controller FIQ Pending Register (ICFP)

Figure 9-2 now appears as:

Figure 9-2. Interrupt Controller Block Diagram



29. Interrupt Controller Pending Register (ICPR): Section 9.2.1.1

Fixed the table below to show the DMA controller is the source module for channel service requests 5 through 0.

Bit Position	Unit	Source Module	# of Level 2 Sources	Bit Field Description
IP 25	Peripheral	DMA controller	3	Channel 5 service request.
IP 24			3	Channel 4 service request.
IP 23			3	Channel 3 service request.
IP 22			3	Channel 2 service request.
IP 21			3	Channel 1 service request.
IP 20			3	Channel 0 service request.
IP 19		Serial port 4b	3	SSP service request.
IP 18		Serial port 4a	8	MCP service request.
IP 17		Serial port 3	6	UART service request.
IP 16		Serial port 2	6+6	UART/HSSP service request.
IP 15		Serial port 1b	6	UART service request.
IP 14		Reserved	—	Reserved.
IP 13		Serial port 0	6	UDC service request.
IP 12		LCD controller	12	LCD controller service request.

30. Interrupt Controller FIQ Pending Register (ICFP): Section 9.2.1.2

Changed register address from 0h 90005 0010 to 0h 9005 0010 (removed extra 0 from 90005).

0h 9005 0010 **ICFP** **Read-Only**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FP31	FP30	FP29	FP28	FP27	FP26	FP25	FP24	FP23	FP22	FP21	FP20	FP19	FP18	FP17	FP16	FP15	FP14	FP13	FP12	FP11	FP10	FP9	FP8	FP7	FP6	FP5	FP4	FP3	FP2	FP1	FP0

Bits	Name	Description
31..0	—	These flags reflect the OR of the reset state of the individual interrupt status bits at the source unit.

31. Interrupt Controller IRQ Pending Register (ICIP) and FIQ Pending Register (ICFP): Section 9.2.1.2

Changed the reset values for the Interrupt Controller IRQ and FIQ Pending Registers (ICIP and ICFP) from undefined to 0. Added the word Reset to the left column in the row that indicates the reset value.

0h 9005 0000 **ICIP** **Read-Only**

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP31	IP30	IP29	IP28	IP27	IP26	IP25	IP24	IP23	IP22	IP21	IP20	IP19	IP18	IP17	IP16	IP15	IP14	IP13	IP12	IP11	IP10	IP9	IP8	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31..0	—	These flags reflect the OR of the reset state of the individual interrupt status bits at the source unit.

0h 9005 0010 **ICFP** **Read-Only**

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FP31	FP30	FP29	FP28	FP27	FP26	FP25	FP24	FP23	FP22	FP21	FP20	FP19	FP18	FP17	FP16	FP15	FP14	FP13	FP12	FP11	FP10	FP9	FP8	FP7	FP6	FP5	FP4	FP3	FP2	FP1	FP0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
31..0	—	These flags reflect the OR of the reset state of the individual interrupt status bits at the source unit.

32. Interrupt Controller Control Register (ICCR): Section 9.2.1.5

Changed reset value for Bit 12 from ? to 0.

0h 9005 000C																ICCR															Read/Write
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																															DIM
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

33. Real-Time Clock: Section 9.3

Changed the third and fourth sentences in the second paragraph. The paragraph now appears as follows:

In addition to the counter [RTC counter register (RCNR)], the RTC incorporates a 32-bit alarm register (RTAR). The RTAR may be programmed with a value to be compared against the counter. RCNR is incremented on each rising edge of the 1-Hz clock. Throughout each 1-Hz clock period RCNR is compared to RTAR. If the values match and the alarm interrupt is enabled, then a status bit is set. This status bit is also routed to the interrupt controller and may be programmed to generate a CPU interrupt.

In the third paragraph, modified the first sentence. The paragraph now appears as follows:

Another status bit is available that is set whenever the 1 Hz clock interrupt occurs. Each status bit may be cleared by writing a one to the status register in the desired bit position. The 1-Hz clock is generated by dividing down the 32.768-kHz crystal oscillator output. This divider logic is programmable to allow the user to trim the counter to adjust for inherent inaccuracies in the crystal frequency. This trimming mechanism permits the user to adjust the RTC to an accuracy of +/- 5 seconds per month. The trimming procedure is described later in this section.

Added the following note.

Note: The 32.768 kHz crystal may take 2-10 seconds to stabilize after a hardware reset. The Power Manager Oscillator Status Register (0x9002001c) bit Oscillator OK (bit 0) is set when the 32.768 kHz clock has stabilized after a hardware reset.

34. RTC Counter Register (RCNR): Section 9.3.1

Added this note at the end of section 9.3.1.

Note: When a value is written to the RTC registers RTTR or RCNR registers, the value is stored correctly, but doing a read immediately after the write will read an incorrect value. At least a 32 µsec delay is needed for the values to propagate through the RTC logic before the stored value can be read back correctly. You may generate this delay by performing multiple reads, but only using the result of the last read.

35. RTC Alarm Register (RTAR): Section 9.3.2

Modified the second sentence. The paragraph now appears as follows:

The real-time clock alarm register is a 32-bit register that is readable and writable by the processor. Throughout each 1-Hz clock period, RCNR is compared to RTAR. If the two are equal and the enable bit is set, then the alarm bit in the RTC status register is set. The value in this register is undefined after the assertion of nRESET.

36. RTC Status Register (RTSR): Section 9.3.3

Added this sentence to the end of the first paragraph:

The ALE interrupt enable bit must be set by software to allow the RTC assertion of the AL bit and the RTC alarm interrupt.

37. RTC Status Register (RTSR): Section 9.3.3

Changed the second sentence to read:

The HZE interrupt enable bit must be set by software to allow the RTC assertion of the HZ bit and the 1-Hz interrupt.

38. RTC Status Register (RTSR): Section 9.3.3

Changed AL and HZ bit descriptions.

0h 9001 0010 **RTSR** **Read/Write**

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																												**HZE**	**ALE**	**HZ**	**AL**
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?

Bits	Name	Description
0	AL	RTC alarm interrupt detected. 0 – No alarm interrupt has been detected. 1 – An alarm interrupt has been detected (RTNR matched RTAR).
1	HZ	1-Hz rising-edge interrupt detected. 0 – No rising-edge interrupt has been detected. 1 – A rising-edge interrupt has been detected.

39. RTC Status Register (RTSR): Section 9.3.3

Added this note at the end of section 9.3.3.

Note: When the AL bit goes high indicating that the alarm has occurred, the alarm interrupt bit (ALE) must first be disabled (by writing a 0 to it) before the AL bit can be cleared (by writing a 0 to it).

40. RTC Trim Register (RTTR): Section 9.3.4

Added this note at the end of section 9.3.4.

Note: When a value is written to the RTC registers RTTR or RCNR registers, the value is stored correctly, but doing a read immediately after the write will read an incorrect value. At least a 32 µsec delay is needed for the values to propagate through the RTC logic before the stored value can be read back correctly. You may generate this delay by performing multiple reads, but only using the result of the last read.

41. Sleep Mode: Section 9.5.3

The second sentence has been changed and now appears as follows:

In the transition from run or idle to sleep mode, the SA-1110 performs an orderly shutdown of on-chip activity, applies an internal reset to the processor, and then negates the PWR_EN pin indicating to the external system that the VDDI (1.5-V supply) can be driven to zero volts.

42. Transaction Summary: Section 10.1.5

Changed the title of table 10-1 from SA-1110 Transactions to:

Table 10-1. SA-1110 Transactions On 32-Bit Data Buses

43. DRAM Refresh Control Register (MDREFR): Section 10.2.2

Added the following sentence to the end of the first paragraph:

Writes to reserved bits are ignored and reads return zeros.

44. MDCAS Registers with SDRAM and SMROM: Section 10.2.3.2

Replaced the first paragraph with these paragraphs:

See Table 10-3 “Timing Interpretations of Possible SDRAM/SMROM MDCAS Settings” on page 10-20 for a description of possible MDCAS encodings for SDRAM or SMROM. nSDCAS asserts as indicated by the first "1" to "0" transition: similar to the behavior of nCAS/DQM for asynchronous DRAM. But, because the least significant bit of MDCAS goes out on nSDCAS one CPU cycle after the assertion of nRAS/nSDCS, the RAS-to-CAS delay is one CPU cycle greater than the number of leading 1's. Thus, a RAS-to-CAS delay of N memory cycles (2N CPU cycles) corresponds to 2N-1 leading 1's. When using MDREFR: KnDB2=0, the number of leading 1's must be 3, 5, 7, ... to achieve a RAS-to-CAS delay of 2, 3, 4, . . . SDCLK cycles. When using MDREFR: KnDB2=1, the number of leading 1's must be 3, 7, 11, . . . to achieve a RAS-to-CAS delay of 1, 2, 3, . . . SDCLK cycles.

For SDRAM, nSDCAS remains asserted throughout the burst, regardless of subsequent transitions programmed into MDCAS. For SMROM, nSDCAS is asserted only through the first column address. In either case, subsequent "0" to "1" transitions must be programmed to reference the data input latch delay (MDCNFG:TDL0,2 or SMCNFG:CL0,2) for every beat of the burst. There must be exactly one or two "0" bits between the leading 1's for RAS-to-CAS delay and the next "1". The option of using one such "0" bit is referred to as "non-delayed read data latching" in the Table 13-3 SDRAM/SMROM timing specifications and guidelines. The option of using two such "0" bits, referred to as "delayed read data latching", provides an additional half memory cycle of read data setup time. The latter option is ignored unless MDREFR:KnDB2=0, and is useful under the following common circumstances (evaluated for specific load):

45. Static Memory Control Registers (MSC2 – 0): Section 10.2.4

Added a second paragraph to the description of RTx 1..0 in the register table.

Bits	Name	Description

1..0	RTx 1..0	ROM type. 00 – Nonburst ROM or Flash memory. 01 – Nonburst ROM or SRAM for nCS 2:0 variable latency I/O for nCS 5:3. 10 – Burst-of-four ROM or Flash (with nonburst writes). 11 – Burst-of-eight ROM or Flash (with nonburst writes). All four types support reads of any burst length. Burst-of-four and burst-of-eight types refer to the use of burst read timings, where modulo four or eight addresses within a burst require the same access times as nonburst reads, but shorter access times are allowed for every other beat. Read bursts are always address aligned to their burst length. The data size of writes to types 00, 10, and 11 must always be less than or equal to the width of the corresponding external data bus: no larger than a single 32-bit word write to a 32-bit data bus, and no larger than a 16-bit half-word write to a 16-bit data bus. Unexpected results, including data loss or corruption, may occur if larger data size writes are attempted.

46. SMROM Configuration Register (SMCNFG): Section 10.3

Added the following sentence to the end of the first paragraph:

Writes to reserved bits are ignored and reads return zeros.

47. SDRAM Commands: Section 10.4.4

Changed row PALL under column nCAS/DQM3:0 from 4'b1111 to 4'b0000.

Command	SA-1110 Pins								
	SDCKE (at clock n-1)	SDCKE (at clock n)	nRAS/ nSDCS3:0	SDRAS	SDCAS	nWE	nCAS/ DQM3:0	DRA14-11, DRA9-0	DRA10
PALL	1	x	0	0	1	0	4'b0000	x	1

48. 8-, 16-, and 32-Bit Data Bus Operation: Section 10.6.1

This section title has been changed to 8-, 16-, and 32-Bit Data Bus Operation (was previously "32-Bit Data Bus Operation).

49. DMA Device Address Register (DDARn): Section 11.6.1.1

Changed the reset values for bits 31:26 from 0 to ?.

DDARn **Read/Write**

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DA 31	DA 30	DA 29	DA 28	DA 27	DA 26	DA 25	DA 24	DA 23	DA 22	DA 21	DA 20	DA 19	DA 18	DA 17	DA 16	DA 15	DA 14	DA 13	DA 12	DA 11	DA 10	DA 9	DA 8	DS 3	DS 2	DS 1	DS 0	DW	BS	E	RW
Reset	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

(Sheet ? of ?)

50. DMA Device Address Register (DDARn): Section 11.6.1.1

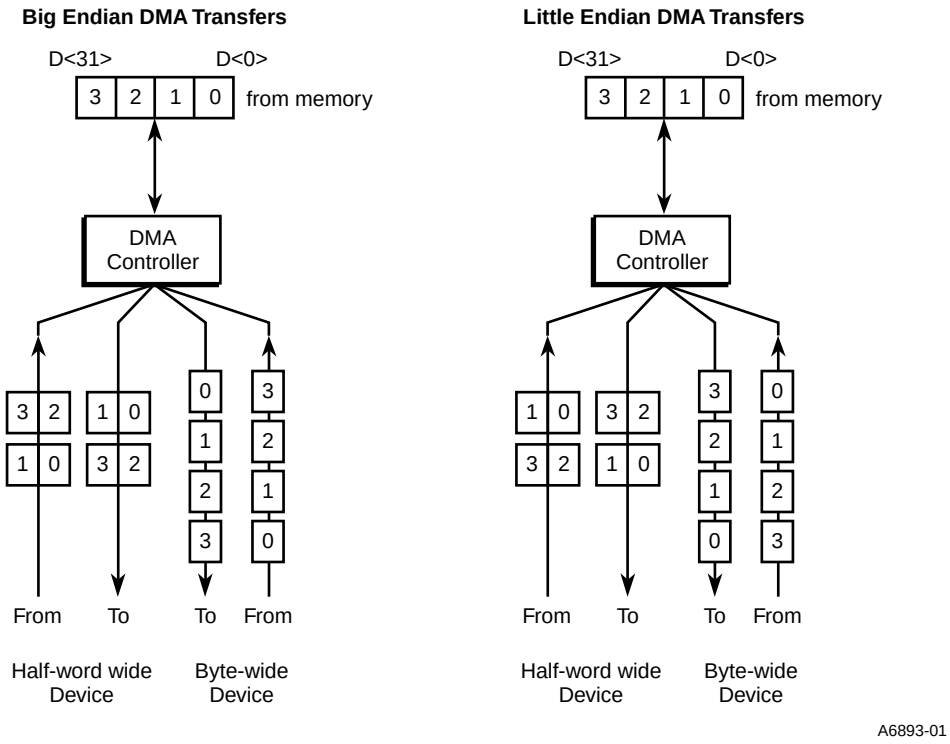
The values for the BS column for Serial Port 4 in Table 11-6 have been changed and now appear corrected in the table. The value for the DS 3:0 column for MCP receive (audio) in Table 11-6 has been changed and is now corrected in the table.

Table 11-6 Valid Settings for the DDARn Register

Unit Name	Function	Device Address	DDAR Fields					
			DA 31:8	DS 3:0	DW	BS	E	RW
Serial port 4	MCP transmit (audio)	0x 8006 0008	0x818002	1010	1	**0**	0/1	0
	MCP receive (audio)	0x 8006 0008	0x818002	1011	1	**0**	0/1	1
	MCP transmit (telecom)	0x 8006 000C	0x818003	1100	1	**0**	0/1	0
	MCP receive (telecom)	0x 8006 000C	0x818003	1101	1	**0**	0/1	1
	SSP transmit	0x 8007 006C	0x81C01B	1110	1	**0**	0/1	0
	SSP receive	0x 8007 006C	0x81C01B	1111	1	**0**	0/1	1

51. DMA Device Address Register (DDARn): Section 11.6.1.1

Corrected Figure 11-2.



52. DMA Control/Status Register (DCSRn): Section 11.6.1.2

Changed DMA control/status register bit-0 from RUNE to RUN and changed the reset value of BIU (Bit 7) from ? to 0.

DCSRn **Read/Write**

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																								**BIU**	**STRTB**	**DONEB**	**STRTA**	**DONEA**	**ERROR**	**IE**	**RUN**
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?0	0	?	?	?	?	?	?	?	?	0	?	?	?	?	?	?	?

(Sheet ? of ?)

53. DMA Control/Status Register (DCSRn): Section 11.6.1.2

Add this note to the end of Section 11.6.1.2:

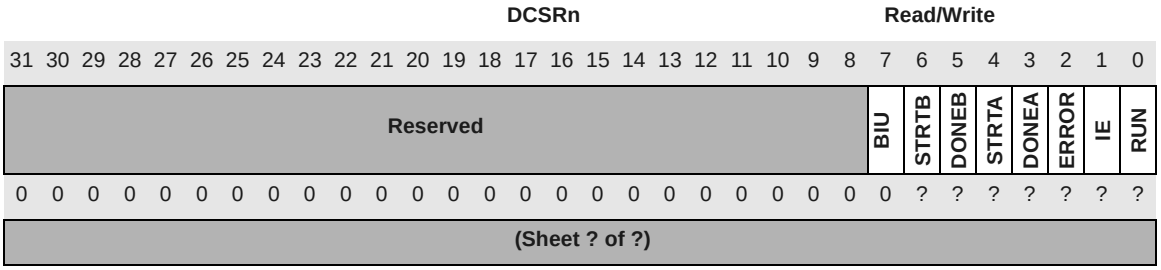
Note: Never clear the BIU bit by writing to DCSR_Clear because this leaves the DMA status register bit BIU (viewed via DCSR_Read) in an undefined state and can only be recovered by reset. Always write 0x7F to DCSR_Clear to clear DCSRn before programming the DMA channel.

54. DMA Control/Status Register (DCSRn): Section 11.6.1.2

Modified the first sentence of the first paragraph. The paragraph now reads as:

DCSR1 - DCSR5 are each a group of three 32-bit read/write registers that contain control and status bits for the channel (refer to Section 11.6.3, “DMA Register List” on page 11-13 for physical addresses and functions of each group). The following figure shows the format for this register; question marks indicate that the values are unknown at reset.

Changed DMA control/status register reset values for the Reserved bits to 0.



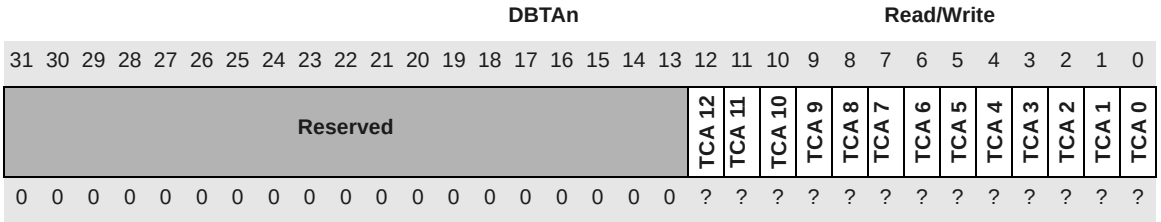
55. DMA Buffer A Transfer Count Register (DBTAn): Section 11.6.1.4

Changed the DMA buffer A transfer count register description in the table from transfer count is 8 Kbyte. to transfer count is 8191 bytes.

Bits	Name	Description
12..0	TCA 12..0	Transfer count (buffer A). This field is a 13-bit value and contains the current transfer count (in bytes) for the transfer to or from buffer A. The maximum value programmed via this transfer count is 8191 bytes.
31..13	—	Reserved. These bits are reserved and read as zeros. Writes to this field have no effect.

56. DMA Buffer A Transfer Count Register (DBTAn): Section 11.6.1.4

Changed DMA Buffer A Transfer Count register reset values for the Reserved bits to 0.



57. DMA Buffer B Transfer Count Register (DBTBn): Section 11.6.1.6

Change the DMA buffer B transfer count register description in the table from transfer count is 8 Kbyte. to transfer count is 8191 bytes.

Bits	Name	Description
12..0	TCB 12..0	Transfer count (buffer B). This field is a 13-bit value and contains the current transfer count (in bytes) for the transfer to or from buffer B. The maximum value programmed via this transfer count is 8191 bytes.
31..13	—	Reserved. These bits are reserved and read as zeros. Writes to this field have no effect.

58. DMA Buffer B Transfer Count Register (DBTBn): Section 11.6.1.6

Changed DMA Buffer B Transfer Count register reset values for the Reserved bits to 0.

DBTBn **Read/Write**

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved																			**TCB 12**	**TCB 11**	**TCB 10**	**TCB 9**	**TCB 8**	**TCB 7**	**TCB 6**	**TCB 5**	**TCB 4**	**TCB 3**	**TCB 2**	**TCB 1**	**TCB 0**
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?	?	?	?	?	?

(Sheet ? of ?)

59. Frame Buffer: Section 11.7.1.2

In the first table in this section, 0x - 4 bits per pixel has been changed to 00 - 4 bits per pixel. The first table in this section now appears as follows:

Bit	Name	Description
13..12	PBS	Pixel bit size. 0**0** – 4 bits per pixel, 16-entry palette, 32 bytes of palette buffer transferred each frame to palette. 01 – 8 bits per pixel, 256-entry palette, 512 bytes of palette buffer transferred each frame to palette. 10 – 12 bits per pixel in passive mode (PAS=0), 16 bits per pixel in active mode (PAS=1). Palette unused, however, 32 bytes of “dummy” palette data is transferred each frame to palette. Palette data must be zero-filled. 11 – Reserved. **Note**: Two 4-bit pixels are packed into each byte, and 12-bit pixels are right justified on half-word boundaries.

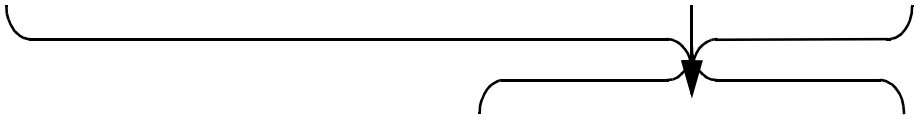
Also in this section, changed 254 to 255 in Figure 11-3. The figure now appears as follows:

Figure 11-3. Palette Buffer Format

Individual Palette Entry

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Color	Unused		PBS*		Red (R)				Green (G)				Blue (B)			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mono	Unused		PBS*		Unused								Monochrome (M)			

***Note:** Pixel bit size (PBS) is contained only within the first palette entry (palette entry 0).



16- or 256-Entry Palette Buffer

Bit	31	16	15	0
Base + 0x0	Palette entry 1		Palette entry 0	
Base + 0x4	Palette entry 3		Palette entry 2	
.				
.				
Base + 0x1C	Palette entry 15		Palette entry 14	
Base + 0x20	Palette entry 17		Palette entry 16	
.				
.				
.				
Base + 0x1FC	Palette entry 255		Palette entry 254	
Base + 0x200	**Start of Encoded Pixel Data**			

Note: Entries 16 through **255** do not exist for 4-, 12- and 16-bit/pixel modes.

Little Endian Palette Entry Ordering

Bit	31	16	15	0
Base + 0x0	Palette Entry 0		Palette Entry 1	
Base + 0x4	Palette Entry 2		Palette Entry 3	
.				
.				

Big Endian Palette Entry Ordering

60. Frame Buffer: Section 11.7.1.2

Changed the formula elements from Line(sXColumns) to LinesXColumns.

4 bits/pixel: $$FrameBufferSize = 32 + 16 + \left(\frac{LinesXColumns}{2}\right) + (2(nXLines))$$

8 bits/pixel: $FrameBufferSize = 512 + 16 + (LinesXColumns) + (nXLines)$

12 or 16 bits/pixel: $FrameBufferSize = 32 + 16 + 2(LinesXColumns)$

61. LCD Enable (LEN): Section 11.7.3.1

Modified the seventh sentence of the paragraph. The sentence now reads as:

Completion of the current frame is signalled by the LCD when it sets the LCD disable done (LDD) status within the LCD status register that generates an interrupt request.

62. Passive/Active Display Select (PAS): Section 11.7.3.7

In the third paragraph, the fifth and sixth sentences have been updated with a single sentence so that users can clear GAFR 6:9 in 4- or 8-bit /pixel mode.

Figure 11-9 shows which bits within each frame buffer entry (for 16-bit/pixel mode) and which bits within a selected palette entry (for 4- and 8-bit/pixel mode) are sent to the individual LCD data pins. In active mode, GPIO pins 2..9 are also used. Note that the user must configure GPIO pins 2..5 as outputs (for 4- and 8-bit/pixel mode), and GPIO pins 2..9 as outputs (for 16-bit/pixel mode) by setting the appropriate bits within the GPIO pin direction register (GPDR) and GPIO alternate function register (GAFR). See the General-Purpose I/O section for configuration information. When in 4- or 8-bits/pixel mode, the user should clear GAFR 6:9 to disable the LCD alternate function and, thereby, prevent unpredictable data from being driven onto GPIO 6:9. In general, the user may clear any number of GAFR bits 2..9, to allow the GPIO unit to assume control of unused GPIO pins for normal digital I/O depending on the required number of data pins

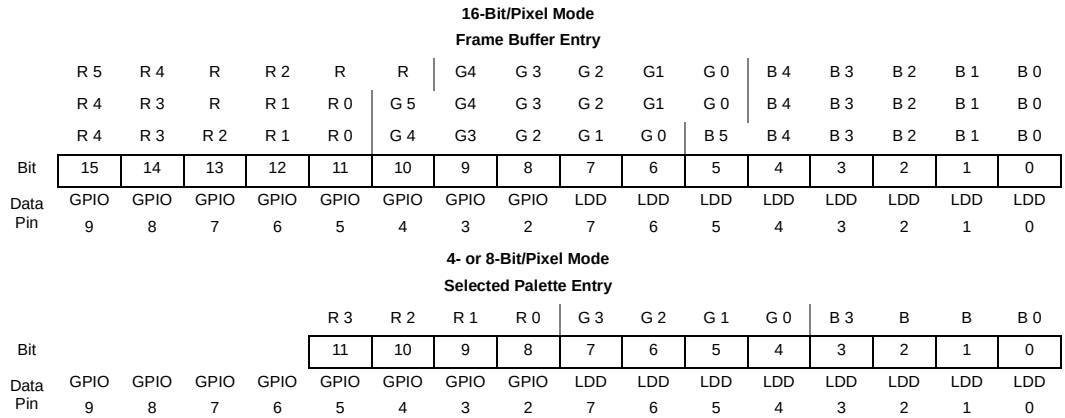
63. Passive/Active Display Select (PAS): Section 11.7.3.7

Removed the first sentence in Footnote 1, which was:

GPIO pins 6..0 are grounded by the LCD in this mode.

Also removed Vss from above GPIO9, GPIO8, GPIO7, and GPIO6 in Figure 11-9. Figure 11-9 and Footnote 1 appear as follows:

Figure 11-9. Frame Buffer/Palette Bits Output to LCD Data Pins in Active Mode



[1]However, if GAFR bit 6..9 are cleared within the system control module, these pins can be used as normal GPIO pins.

64. Double-Pixel Data (DPD) Pin Mode: Section 11.7.3.9

Changed the third sentence to read:

See Table 11-8 “Color/Gray-Scale Intensities and Modulation Rates” on page 11-23 and Figure 11-8 “Frame Buffer/Palette Bits Output to LCD Data Pins in Active Mode” on page 11-29 for a comparison of how the LCD’s data pins are used in each of its display modes.

65. Palette DMA Request Delay (PDD): Section 11.7.3.10

Removed last sentence from the third paragraph, which was “Note that writes to reserved bits are ignored and reads returns zeros.” The third paragraph now appears as follows:

The following table shows the location of all 10 bit-fields located in LCD control register 0 (LCCR0). The user must program the control bits within all other control registers before setting LEN=1 (a word write can be used to configure LCCR0 while setting LEN after all other control registers have been programmed), and also must disable the LCD controller when changing the state of any control bit within the LCD controller.

66. Palette DMA Request Delay (PDD): Section 11.7.3.10

Changed description of Bits 11:10 from Reserved to LCCR0 and added bit description.

11..10	LCCR0	LCD Control Register 0 Bits: 11 10 0 0 – Values after reset 0 1 – Vertical slant correction pattern 0, modulation rate is 4/15 and 11/15 1 0 – Vertical slant correction pattern 1, modulation rate is 4/15 and 11/15 1 1 – Reserved

67. Beginning-of-Frame Line Clock Wait Count (BFW): Section 11.7.5.4

Changed the second sentence in the second paragraph for the description of bits 15:10 in the LCD Control Register 2. The bit description now appears as follows:

0h B010 0024 LCCR2: LCD Control Register 2 Read/Write

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BFW								EFW								VSW						LPP									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15..10	VSW	Vertical sync pulse width. In active mode (PAS=1), value (from 1 to 64). Used to specify number of line clock periods to pulse the L_FCLK pin at the end of each frame after the end-of-frame wait (EFW) period elapses. Frame clock used as VSYNC signal in active mode. In passive mode (PAS=0), value (from 1 to 64). Used to specify number of extra line clock periods to insert after the end-of-frame. Note that the width of L_FCLK is not affected by VSW in passive mode and that line clock does transition during the insertion of the extra line clock waitstate periods. Also note that both EFW and BFW should be set to zero in passive mode. VSYNC width = (VSW+1).

68. Pixel Clock Divider: Section 11.7.6.1

In the second sentence in this section, changed the PCD value from 225 to 255. The second sentence now appears as follows:

PCD can be any value from 1 to 2**5**5 (0 is illegal) and is used to generate a range of pixel clock frequencies from CCLK/6 to CCLK/514 (where CCLK is the programmed frequency of the CPU clock).

69. Output Enable Polarity (OEP): Section 11.7.6.7

In the table describing LCCR3, the value in the description for the PCD row was modified, as indicated in bold. The PCD row now appears as follows:

0h B010 0028 **LCCR3: LCD Control Register 3** **Read/Write**

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved								**OEP**	**PCP**	**HSP**	**VSP**	**API**				**ACB**								**PCD**							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
7..0	PCD	Pixel clock divisor. Value (from **1** to 255). Used to specify the frequency of the pixel clock based on the CPU clock (CCLK) frequency. Pixel clock frequency can range from CCLK/6 to CCLK/514. Pixel Clock Frequency = CCLK/2(PCD+2). Note that PCD must be programmed with a value of 1 or greater (PCD = 8'h00 is illegal).

70. DMA Channel 1 Current Address Register: Section 11.7.9

Changed the title bar for the register description from Read/Write to Read Only. The title bar appears as follows:

0h B010 0014 **DCAR1: DMA Channel 1 Current Address Register** **Read Only**

71. Output FIFO Underrun Lower Panel Status (OUL) (read only, maskable interrupt): Section 11.7.10

Changed title from read/write to read only.

72. LCD Disable Done Flag: Section 11.7.11.1

Changed paragraph 11.7.11.1 title from LCD Disable Done Flag to LCD Disable Done Status.

Changed the first sentence to:

The LCD disable done (LDD) status is set after the LCD has been disabled and the frame that is active finishes being output to the LCD's data pins.

73. Base Address Update Flag: Section 11.7.11.2

Changed paragraph 11.7.11.2 title from Base Address Update Flag (BAU) (read-only, maskable interrupt) to Base Address Update Status (BAU) (read/write, maskable interrupt).

Changed the first sentence to:

The base address update status (BAU) is a read/write status bit that is set after the contents of the DMA base address register 1 are transferred to the DMA current Address register 1 and is cleared when it is written to a 1.

Changed the last two sentences to:

When dual-panel mode is enabled (SDS=1), both DMA channels are enabled, and BAU is set only after both channels' base address registers are transferred to their corresponding current address registers (1 and 2).

74. Output FIFO Underrun Upper Panel Status (OUU) (read/write, maskable interrupt): Section 11.7.11.12

Changed the reset value (bolded) and the name of bit 0 in the register table to match the name used in the description (LDD).

0h B010 0004 LCSR: LCD Status Register Read/Write and Read-Only

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved																				OUU	OOU	OUL	OOL	IUU	IOU	IUL	IOL	ABC	BER	BAU	LDD
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0**

Bits	Name	Description
0	LDD	LCD disable done flag. 0 – LCD has not been disabled and the last active frame completed. 1 – LCD has been disabled and the last active frame has just completed.

75. Output FIFO Underrun Upper Panel Status (OUU) (read/write, maskable interrupt): Section 11.7.11.12

Changed the description in the register definition table for bit 0 from LCD disable done flag to LCD disable done status.

Bits	Name	Description
0	LDD	LCD disable done status. 0 – LCD has not been disabled and the last active frame completed. 1 – LCD has been disabled and the last active frame has just completed.

76. LCD Controller Register Locations: Section 11.7.12

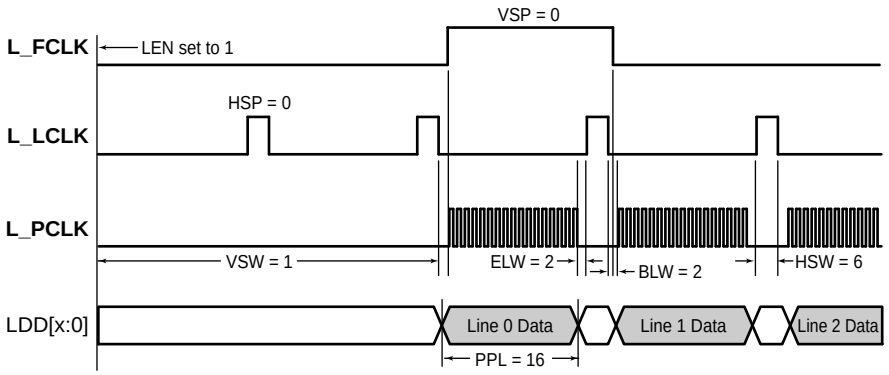
In the second sentence in this section, changed the figure references. The second sentence now appears as follows:

Figures 11-10 to **Figure 11-14** describe the LCD controller timing parameters.

77. LCD Controller Pin Timing Diagrams: Section 11.7.13

Changed the Notes: in Figure 11-10 to show the range of HSW as 1 to 64, not 0 to 64. The corrected figure is shown below:

Figure 11-10. Passive Mode Beginning-of-Frame Timing



Notes:

LEN - LCD enable:
0 - LCD is disabled.
1 - LCD is enabled.
VSP - Vertical sync polarity:
0 - Frame clock is active high, inactive low.
1 - Frame clock is active low, inactive high.
VSW - Vertical Sync Pulse Width:
1 to 64 horizontal sync clock periods to assert the vertical sync signal (hsync transitions).
HSP - Horizontal sync polarity:
0 - Line clock is active high, inactive low.
1 - Line clock is active low, inactive high.
ELW - End-of-line pixel clock wait count:
1 to 256 "dummy" pixel clock periods to wait after last pixel in line before asserting line clock (pixel clock does not transition).
BLW - Beginning-of-line pixel clock wait count:
1 to 256 "dummy" pixel clock periods to wait after line clock negated before asserting pixel clocks (pixel clock does not transition).
HSW - Horizontal sync pulse width:
1 to 64 "dummy" pixel clock periods to assert the line clock (pixel clock does not transition).
PPL - Pixels per line:
16 to 1024 pixels per line on the screen (must be programmed on 16 pixel multiples).
Frame clock asserted on first pixel clock of each frame, and is negated one "dummy" pixel clock period before the first pixel clock of the 2nd line.

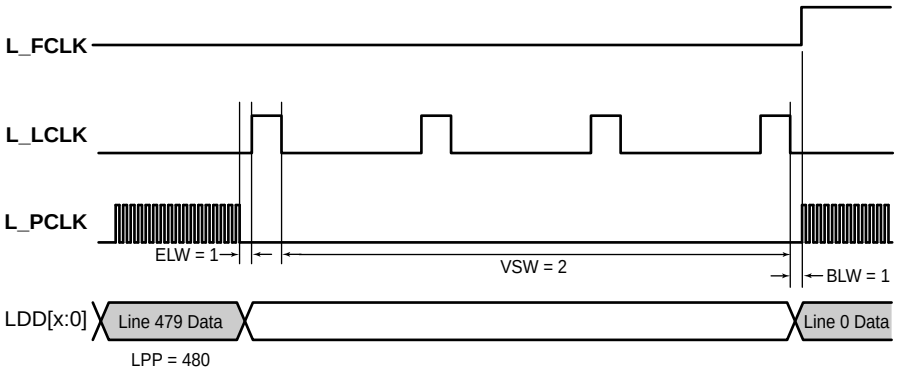
A4790-01

78. LCD Controller Pin Timing Diagrams: Section 11.7.13

In Figure 11-11 at the location where L_LCLK is deasserted just prior to Line 0 Data, there are two vertical bars depicting BLW = 1. Extended the right vertical bar upward to near L-LFCLK. At this point, changed L_FCLK to show a transition from deasserted to asserted (shown below.)

Also, changed the Notes: in Figure 11-11 to show the range of BLW as 1 to 256, not 0 to 256. The corrected figure is shown below:

Figure 11-11. Passive Mode End of Frame Timing



Notes:

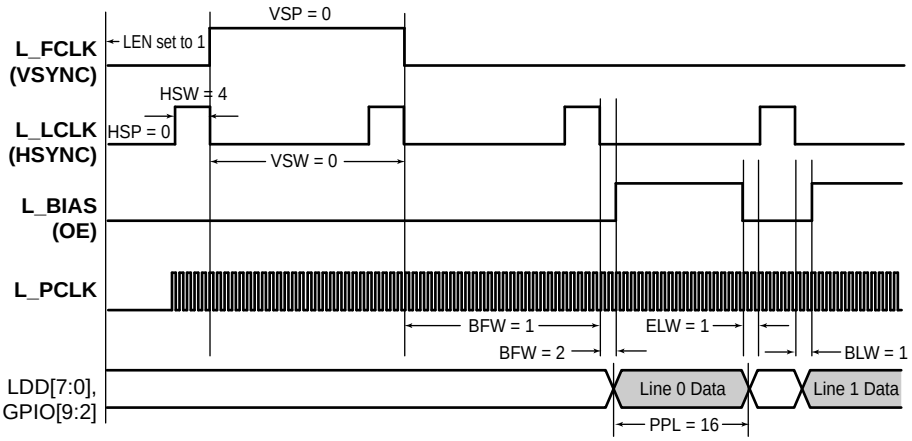
BLW - Beginning-of-line pixel clock wait count:
1 to 256 "dummy" pixel clock periods to wait after line clock is negated before asserting pixel clocks (pixel clock does not transition).
VSW - Vertical sync pulse width:
In passive mode, 1 to 64 line clock periods to wait between the end of one frame and the beginning of the next frame (line clock transitions).
ELW - End-of-line pixel clock wait count:
1 to 256 "dummy" pixel clock periods to wait after last pixel in line before asserting line clock (pixel clock does not transition).
LPP - Lines per panel:
1 to 1024 lines per panel.

A4791-01

79. LCD Controller Pin Timing Diagrams: Section 11.7.13

Corrected Notes: in Figure 11-13 to show the range of PPL as 16 to 1024 (not 1 to 1024.) The corrected figure is shown below:

Figure 11-13. Active Mode Timing



Notes:

LEN - LCD enable:
0 - LCD is disabled.
1 - LCD is enabled.
VSP - Vertical sync polarity:
0 - Vertical sync clock is active high, inactive low.
1 - Vertical sync clock is active low, inactive high.
VSW - Vertical sync width:
1 to 64 horizontal sync clock periods to assert the vertical sync signal (hsync transitions).
HSW - Horizontal sync pulse width:
1 to 64 pixel clock periods to assert the line clock (pixel clock transitions).
HSP - Horizontal sync polarity:
0 - Horizontal sync clock is active high, inactive low.
1 - Horizontal sync clock is active low, inactive high.
BFW - Beginning-of-frame horizontal sync clock wait count:
0 to 255 horizontal sync clock periods to wait at the beginning of each frame (hsync transitions).
BLW - Beginning-of-line pixel clock wait count:
1 to 256 pixel clock periods to wait after line clock negated before asserting pixel clocks (pixel clock transitions).
ELW - End-of-line pixel clock wait count:
1 to 256 pixel clock periods to wait after last pixel in line before asserting line clock (pixel clock transitions).
PPL - Pixels per line:
16 to 1024 pixels per line on screen.

A4793-02

80. Serial Port 0 – USB Device Controller: Section 11.8

Changed the reference to the *Universal Serial Bus Specification* in the last sentence of paragraph one from Revision 1.0 to Revision 1.1. The sentence now reads as:

However, the user should refer to the *Universal Serial Bus Specification*, Revision 1.1[1] for a full description of the USB protocol and its operation.

Also changed the footnote at the bottom of page 11-55 to read:

1. The latest revision of the *Universal Serial Bus Specification Revision 1.1* can be accessed via the World Wide Web Internet site at: http://www.teleport.com/~usb/

81. USB Operation: Section 11.8.1

Added this note to section 11.8.1:

Note: The UDC must only describe one device configuration to the USB host during the GET_DESCRIPTOR phase of the device interrogation. The reason is that if the host wanted to switch to a different configuration on the SA-1110, the UDC would be required to flush any data that is in the TX fifo. In order for the UDC to flush the TX fifo, the UDC must be disabled and re-enabled, which causes all UDC registers to be reset, and then the UDC will no longer respond to its host assigned address.

82. UDC Endpoint 2 Control/Status Register: Section 11.8.9

Changed the reset value of the TFS bit from 0 to ?.

0h 8000 0018 **UDCCS2** **Read/Write**

	7	6	5	4	3	2	1	0
	Reserved		**FST**	**SST**	**TUR**	**TPE**	**TPC**	**TFS**
Reset	0	0	0	0	0	0	0	?

83. UDC Endpoint Data Register: Section 11.8.10

Changed the Bottom of Endpoint 0 FIFO and Top of Endpoint 0 FIFO reset values from 0 to ?.

0h 8000 001C **UDCD0** **Read/Write**

	7	6	5	4	3	2	1	0
	Bottom of Endpoint 0 FIFO							
Reset	?	?	?	?	?	?	?	?
	Read Access							
	7	6	5	4	3	2	1	0
	Top of Endpoint 0 FIFO							
Reset	?	?	?	?	?	?	?	?

84. UDC Data Register: Section 11.8.12

Changed the Bottom of Receive FIFO and Top of Transmit FIFO reset values from 0 to ?.

0h 8000 0028 **UDCDR** **Read/Write**

	7	6	5	4	3	2	1	0
	Bottom of Receive FIFO							
Reset	?	?	?	?	?	?	?	?
	Read Access							
	7	6	5	4	3	2	1	0

	Top of Transmit FIFO							
Reset	?	?	?	?	?	?	?	?

85. Sample Clock Direction (SCD): Section 11.9.2.3

Change Bold text to Normal text in the Bit and Reset rows of the register.

Address: 0h 8002 0060					GPCLKR0		Read/Write	
Bit	7	6	5	4	3	2	1	0
	Reserved	Reserved	SCD	SCE	Reserved	Reserved	Reserved	SUS
Reset	?	?	?	?	?	?	?	0

86. Transmit Enable (TXE): Section 11.9.3.1

Changed - to ? in the Reset row of the register.

0h 8002 0064			GPCLKR1			Read/Write	
7	6	5	4	3	2	1	0
Reserved						TXE	Reserved
Reset	?	?	?	?	?	?	0	?

87. 4PPM Modulation: Section 11.10.2.1

Changed sentence at the bottom of Figure 11-26. The sentence now reads:

Receive data sample counter frequency = 6X timeslot frequency; each timeslot sampled on third clock.

88. CPU and DMA Register Access Sizes: Secti9on 11.10.2.11

Change the 2nd sentence of paragraph one. Paragraph one now reads as:

Bit positioning, byte ordering, and addressing of the HSSP is described in terms of little endian ordering. All ICP (HSSP and UART) registers are 8 bits wide and are located (except HSCR2) in the least significant byte of individual words. The ARM peripheral bus does not support byte or half-word operations. All reads and writes of the ICP by the CPU should be word–wide.

89. HP-SIR * Enable (HSE): Section 11.10.4.1

The second sentence has been changed and now appears as follows:

When HSE=0, HP-SIR * modulation is disabled, and if UART operation is enabled (ITR=0), it is used for normal serial transmission rather than IrDA communication.

90. Low-Power Mode (LPM): Section 11.10.4.2

Change the 1st sentence of the 2nd paragrph. The paragraph now reads as:

The following table shows the location of the bits within UART control register 4. Both bits are reset to zero. Note that the UART must be disabled (RXE=TXE=0) when changing the state of either of these two bits. Also note that writes to reserved bits are ignored and reads return zeros.

Changed the reset values of LPM and HSE from ? to 0.

	0h 8003 0010			UTCR4			Read/Write	
	7	6	5	4	3	2	1	0
	Reserved						LPM	HSE
Reset	0	0	0	0	0	0	0	0

Removed the note: Note: A question mark (?) signifies that the Reset value of that bit is undefined when the processor has completed its reset cycle.

91. IrDA Transmission Rate (ITR): Section 11.10.6.1

Changed the last two sentences in the paragraph. The paragraph now reads as:

The IrDA transmission rate (ITR) bit is used to select the transmission speed of the ICP. ITR selects the correct type of IrDA bit modulation to use (HP-SIR* or 4PPM), and enables the correct serial-to-parallel engine (UART or HSSP). When ITR=0, the HP-SIR* modulator is enabled along with serial port 2's UART. When ITR=1, the 4PPM modulator is enabled as well as the HSSP. Note after one of the two speeds is selected by programming the ITR bit of HSCR0, all further selection of UART and HSSP options is done by programming the control registers associated with each of the individual UART and HSSP units.

92. Loopback Mode (LBM): Section 11.10.6.2

Changed the fourth sentence. The paragraph now reads as:

The loopback mode (LBM) bit is used to enable and disable the ability of the HSSP's transmit and receive logic to communicate. When LBM=0, the HSSP operates normally. The transmit and receive data paths are independent and communicate via their respective pins. When LBM=1, the output of the transmit serial shifter is directly connected to the input of the receive serial shifter internally, and (if ITR=1) control of the TXD2 and RXD2 pins is given to the peripheral pin control (PPC) unit. Note that even though the IrDA standard permits only half-duplex operation, the HSSP does not restrict the user from transmitting and receiving data at the same time; both are fully independent units. This function is essential when using the HSSP in loopback mode.

93. Transmit Enable (TXE): Section 11.10.6.4

Changed the first sentence of the second paragraph. The paragraph now reads as:

TXE and RXE are the only HSCR0 control bits within the HSSP that are initialized when a hardware reset occurs. Clearing TXE to zero ensures the HSSP transmitter is disabled, giving control of the transmit pin to the PPC unit that configures TXD1 as an input following a reset of the SA-1110. Note that TXE is ignored when ITR=0 (enables UART operation). Also note that even though the IrDA standard permits only half-duplex operation, the HSSP does not restrict the user from transmitting and receiving data at the same time; both are fully independent units. This function is particularly useful when using the HSSP in loopback mode. See the Section 11.10.6.2, "Loopback Mode (LBM)" on page 11-97.

94. Receive Pin Polarity Select (RXP): Section 11.10.8.2

Under the Name column of the HSCR register table 2, added TXP in the bit 18 row and RXP in the bit 19 row.

Bits	Name	Description
18	TXP	Transmit pin polarity select. 0 – Data output from the HSSP, UART, or PPC is first inverted before being output to TXD2. 1 – Data output from the HSSP, UART, or PPC to TXD2 is true or non-inverted data.
19	RXP	Receive pin polarity select. 0 – Data input from RXD2 is first inverted before being used by the HSSP, UART, or PPC. 1 – Data input from RXD2 to the HSSP, UART, or PPC is true or non-inverted data.

95. End/Error in FIFO Status (EIF) (read-only, nonmaskable interrupt): Section 11.10.10.1

Changed the paragraph title to:

11.10.10.1 End/Error in FIFO Flag (EIF) (read-only, nonmaskable interrupt)

96. Framing Error Status (FRE) (read/write, nonmaskable interrupt): Section 11.10.10.6

Changed the RAB bit description in the HSSR0 register table.

Bits	Name	Description
2	RAB	Receiver abort. 0 – No abort has been detected for the incoming frame. 1– Abort detected during receipt of incoming frame. Two or more chips containing no pulses (0000), or invalid chips not contained within the stop flag, detected on receive pin. EOF bit set in receive FIFO next to last piece of “good” data received before the abort, interrupt requested.

97. CRC Error Status (CRE) (read-only, noninterruptible): Section 11.10.11.6

Changed the paragraph title to:

11.10.11.6 CRC Error Flag (CRE) (read-only, noninterruptible)

98. Receiver Overrun Status (ROR) (read-only, noninterruptible): Section 11.10.11.7

Changed the paragraph title to:

11.10.11.7 Receiver Overrun Flag (ROR) (read-only, noninterruptible)

Changed the description of the RSY bit in the HSSR1 register table.

Bits	Name	Description
0	RSY	Receiver synchronized flag (read-only). 0 – Receiver is in hunt mode or is disabled. 1 – Receiver logic is synchronized with the incoming data (no interrupt generated).

99. Sample Clock GPIO: Section 11.11.3.5

In the third paragraph, second sentence, modify the GPIO number as indicated in bold. The sentence now appears as follows:

When the external sample clock function is enabled, serial port 1 uses the GPIO 18 pin and serial port 3 uses **GPIO 20**.

100. UART Data Register: Section 11.11.6

Changed the reset values of Bottom of Receive FIFO Data and Top of Transmit FIFO Data from zero to ?.

0h 8005 0014 **UTDR** **Read/Write**

	10	9	8	7	6	5	4	3	2	1	0
	ROR	**FRE**	**PRE**	**Bottom of Receive FIFO Data**							
Reset	0	0	0	?	?	?	?	?	?	?	?

Read Access
Note: ROR, FRE, PRE are not read, but rather are transferred to corresponding status bits in UTSR1 each time a data value is transferred to UTDR.

	7	6	5	4	3	2	1	0
	Top of Transmit FIFO Data							
Reset	?	?	?	?	?	?	?	?

101. UART Data Register: Section 11.11.6

Changed reset values of bits 10:8 from0 to ?.

0h 8005 0014 **UTDR** **Read/Write**

	10	9	8	7	6	5	4	3	2	1	0
	ROR	**FRE**	**PRE**	**Bottom of Receive FIFO Data**							
Reset	?	?	?	?	?	?	?	?	?	?	?

102. SSP Transmit and Receive FIFOs: Section 11.12.7.3

In the fourth paragraph, deleted the fourth sentence and modified the last sentence. The paragraph now appears as follows:

The width of each entry within the FIFOs is 16 bits. However, the SSP supports data sizes of 4 through 16 bits. Any data that is less than 16-bits wide must be left-justified when writing or DMAing data to the transmit FIFO. Figure 11-35 shows the required data alignment for the transmit and receive FIFOs. The user must left-justify data to be transmitted, however, data read from the receiver is automatically right-shifted the appropriate amount, requiring no further modification before using the results.

103. SSP Transmit and Receive FIFOs: Section 11.12.7.3

Changed the title of Figure 11-36 from Transmit/Receive FIFO Data Format to Transmit FIFO Data Format.

104. SSP Data Register: Section 11.12.11

Changed the Top of Receive FIFO to the Top of Transmit FIFO and changed the reset values of Bottom of Receive FIFO and Top of Transmit FIFO from zero to ?.

0h 8007 006C **SSP Data Register: SSDR** **Read/Write**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Bottom of Receive FIFO															
Reset	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
	Read Access															

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Top of Transmit FIFO															
Reset	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
	Write Access															

105. PPC Pin Direction Register: Section 11.13.3

Changed the reserved bit reset values from 0 to 1 in the PPC pin direction register table. The eleventh sentence in the first paragraph now reads:

For reserved bits, writes are ignored and reads return one.

0h 9006 0000 **PPC Pin Direction Register: PPDR** **Read/Write**

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved										**SFRM**	**SCLK**	**RXD4**	**TXD4**	**RXD3**	**TXD3**	**RXD2**	**TXD2**	**RXD1**	**TXD1**	**L_BIAS**	**L_FCLK**	**L_LCLK**	**L_PCLK**	**LDD 7**	**LDD 6**	**LDD 5**	**LDD 4**	**LDD 3**	**LDD 2**	**LDD 1**	**LDD 0**
Reset	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	(Sheet ? of ?)																															

106. PPC Pin State Register: Section 11.13.4

Changed the reserved bit reset values from 0 to 1 and bits 21:0 to ? in the PPC pin state register table. The last sentence in the fourth paragraph now reads:

Note that this register is not reset and that for reserved bits, writes are ignored and reads return ones.

0h 9006 0004 **PPC Pin State Register: PPSR** **Read/Write**

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Reserved										**SFRM**	**SCLK**	**RXD4**	**TXD4**	**RXD3**	**TXD3**	**RXD2**	**TXD2**	**RXD1**	**TXD1**	**L_BIAS**	**L_FCLK**	**L_LCLK**	**L_PCLK**	**LDD 7**	**LDD 6**	**LDD 5**	**LDD 4**	**LDD 3**	**LDD 2**	**LDD 1**	**LDD 0**

Reset	1	1	1	1	1	1	1	1	1	1	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

(Sheet ? of ?)

107. PPC Pin State Register: Section 11.13.4

Changed the reset value of bit 15 from v to ?.

0h 9006 0004 PPC Pin State Register: PPSR Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved										SFRM	SCLK	RXD4	TXD4	RXD3	TXD3	RXD2	TXD2	RXD1	TXD1	L_BIAS	L_FCLK	L_LCLK	L_PCLK	LDD 7	LDD 6	LDD 5	LDD 4	LDD 3	LDD 2	LDD 1	LDD 0
1	1	1	1	1	1	1	1	1	1	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

108. PPC Pin Assignment Register: Section 11.13.5.2

Changed the reserved bit reset values from 0 to 1 in the PPC pin assignment register table. The second sentence in the second paragraph now reads:

Both control bits are cleared to one following a reset of the SA-1110, giving control of all GPIO pins to the system control module.

0h 9006 0008 PPC Pin Assignment Register: PPAR Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													SPR	Reserved					UPR	Reserved											
Reset	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1

(Sheet ? of ?)

109. PPC Sleep Mode Pin Direction Register: Section 11.13.6

Remove the word manager after the eighth sentence in the second paragraph.

110. PPC Pin Flag Register: Section 11.13.7

Changed reset values of reserved bits from 0 to 1.

0h 9006 0010 PPC Pin Flag Register: PPFR Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													SP4	SP3 RX	SP3 TX	SP2 RX	SP2 TX	SP1 RX	SP1 TX	Reserved											LCD
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

111. DC Operating Conditions: Section 12.2

These changes have been made in Table 12-2 (new table shown below):

- Rows Ioh and Iol have been removed

- Row ESD has had information added and 1 was removed from the Nominal column
- Changed the Minimum for Vihc from 0.8 X VDDX to 2.4
- Replaced note 5

Table 12-2. SA-1110 DC Operating Conditions

Symbol	Parameter	Minimum	Nominal	Maximum	Units	Notes
Vihc	IC input high voltage	2.4	—	VDDX	V	1, 2, 5
Vilc	IC input low voltage	0.0	—	0.2 × VDDX	V	1, 2
Vohc	OCZ output high voltage	0.8 × VDDX	—	VDDX	V	1, 3
Volc	OCZ output low voltage	0.0	—	0.2 × VDDX	V	1, 3
Iohc	High-level output current	—	—	– 2	mA	—
Iolc	Low-level output current	—	—	2	mA	—
Ta	Ambient operating temperature	0	—	70	°C	—
Iin	IC input leakage current	—	10	—	µA	—
Cin	Input capacitance	—	5	—	pF	4
ESD	HBM model ESD	—	—	**1000**	V	

NOTES:
1. Voltages measured with respect to VSS.
2. IC – CMOS-level inputs (includes IC and ICOCZ pin types).
3. OCZ – Output, CMOS levels, three state.
4. Parameter guaranteed by design.
5. Minimum not tested at this time

112. Power Supply Voltages and Currents: Section 12.3

Replaced Table 12-3 with the table below and the note has been modified.

Parameter	AC, AD (133 MHz)	BC, BD (206 MHz)
Maximum Run Mode Power	500 mW	1000mW
Typical Run Mode Power[1]	200 mW	350 mW
Maximum Idle Mode Power[2]	100 mW	200 mW
Typical Idle Mode Power[2]	75 mW	100 mW
Maximum Sleep Mode Current[2]	75 u A	75 u A
Typical Sleep Mode Current[2]	50 u A	50 uA
Vddi Max	1.63 V	2.10 V
Vddi Typ	1.55 V	1.75 V
Vddi Min	1.47 V	1.65 V
Vddx Max	3.60 V	3.60 V

Parameter	AC, AD (133 MHz)	BC, BD (206 MHz)
Vddx Typ	3.30 V	3.30 V
Vddx Min	3.00 V	3.00 V

NOTES:
1. Typical operation defined using the following parameters:
   320x240 LCD operating at 70 fps (passive color LCD,
   8-bit color depth, single panel (1 DMA unit); and
   UART3 transmitting and receiving 115.2 kbps (using 2 DMA units).
2. Room Temperature

Note: Only maximum values are guaranteed by manufacturing test screen. **Due to end-of-life status for B1 components, B-1 data has been eliminated from** Table 12-3**.**

113. Timing Parameters: Section 13.6

As indicated in bold, several parameters have changed in Table 13-3. Note 1 has been modified and Note 3 has been added to bottom of the table.

Table 13-3. SA-1110 AC Timing Specifications and Guidelines for SDRAM/SMROM

Pin Name	Symbol	Parameter	AC, AD (133 MHz max) BC, BD (206 MHz max)	SDCLK Frequency (MHz)	Non-Delayed or Delayed Latching on Read Data	Min	Unit	Note
Memory Bus								
A<25:0>, D<31:0>, nRAS/ nSDCS<3:0>, nCAS/ DQM<3:0>, nCS<3:0>, nSDRAS, nSDCAS, nWE, nOE, SDCKE<1:0>	Tsdos	SDRAM/ SMROM output setup time to SDCLK<2:0> rise	AC	28 - 66		**2.2**	ns	**3**
			BC	28 - 103		**2.2**	ns	**3**
A<25:0>, D<31:0>, nRAS/ nSDCS<3:0>, nCAS/ DQM<3:0>, nCS<3:0>, nSDRAS, nSDCAS, nWE, nOE, SDCKE<1:0>	Tsdoh	SDRAM/ SMROM output hold time from SDCLK<2:0> rise	AC	28 - 66		2.2	ns	
			BC	28 - 103		2.2	ns	
D<31:0>	Tsdis	SDRAM/ SMROM data input setup time to SDCLK<2:0> rise	AC	28 - **66**	Non-Delayed	**7.2**	ns	1
			BC	28 - 62	Non-Delayed	9.3	ns	1
				62 - 103	Delayed	2.7	ns	1
D<31:0>	Tsdih	SDRAM/ SMROM data input hold time from SDCLK<2:0> rise	AC	28 - **66**	Non-Delayed	2.7	ns	1
			BC	28 - 62	Non-Delayed	2.7	ns	1
				62 - 69	Delayed	**5.5**	ns	1, 2
				69 - 7**6**	Delayed	4.**7**	ns	1, 2
				7**6** - 84	Delayed	4.1	ns	1, 2
				84 - 91	Delayed	**3.6**	**ns**	**1, 2**
				91 - 98	**Delayed**	**3.1**	**ns**	**1, 2**
				98 - 103	Delayed	2.7	ns	1

NOTES:
1. Tsdis and Tsdih are specified for non-delayed read data latching on 133 MHz (AC, AD) and 206 MHz (BC, BD) devices, and for delayed read data latching at the maximum SDCLK frequency on AC and AD devices (103 MHz when using a 3.6864 MHz crystal). All other Tsdis and Tsdih values (i.e.- those for delayed read

data latching on BC and BD devices with SDCLK between 62 MHz and 98 MHz) should be considered as guidelines, and are not guaranteed for use under all operating conditions.
2. The larger Tsdih values can be achieved by intentionally adding delay to SDCLK (e.g., by using serpentine board routing). However, the system designer must carefully evaluate the resulting degradation to input setup time and output hold time: Tsdis and Tsdoh increase and decrease, respectively, from the corresponding table values.
3. **When SDRAM/SMROM is configured to run at one-half the memory clock frequency (e.g., MDREFR:K0DB2 = 1 for SMROM), the minimum output setup time is increased from Tsdos by approximately one memory clock period. This helps to accommodate SMROM, which typically requires both a lower frequency and larger setup times than SDRAM.**

114. Timing Parameters: Section 13.6

As indicated in Table 13-5, Trxds min is now 11 ns (was previously 0 ns) and Trxdh is 0 ns (was previously 4 ns).

Table 13-5 SA-1110 AC Timing Table: MCP Interface and LCD Controller

Pin Name	Symbol	Parameter	Min	Max	Unit	Note
MCP (CODEC) Interface						
SFRM_C	Tsfrmv	SCLK_C rise to SFRM_C driven valid	—	21	ns	—
RXD_C	Trxds	RXD_C valid to SCLK_C fall (input setup)	**11**	—	ns	—
	Trxdh	SCLK_C fall to RXD_C invalid (input hold)	**0**	—	ns	—
TXD_C	Ttxdv	SCLK_C rise to TXD_C valid	—	22	ns	—
LCD Controller						
L_LDD<7:0>	Tpclkdv	L_PCLK rise/fall to L_LDD<7:0> driven valid	—	14	ns	1
L_LCLK	Tpclklv	L_PCLK fall to L_LCLK driven valid	—	14	ns	2
L_FCLK	Tpclkfv	L_PCLK fall to L_LFCLK driven valid	—	14	ns	2
L_BIAS	Tpclkbv	L_PCLK rise to L_BIAS driven valid	—	14	ns	2

115. Package and Pinout: Section 14

Added Table 14-3 to show how to identify design Revision Number from the data marked on the SA-1110's package. Added B5 stepping information. Changed the paragraph in Section 14 to include references to Table 14-3. The paragraph now reads as:

This chapter describes package mechanical data, package pin-out data, and design Revision Number identification data. Figure 14-1 shows the SA-1110 256-pin mini-BGA mechanical drawing. Table 14-1 lists the SA-1110 pins in numeric order, showing the signal type for each pin. Table 14-2 lists the SA-1110 pins and their corresponding ball grid array (BGA) in alphabetic order, showing the signal type for each pin. Use Table 14-3 to identify the SA-1110 design revision number from physical marking on the SA-1110 package.

Table 14-3 Package Marking Versus Revision Number

Package Markings	Voltage (V)	Package Type	Speed (MHz)	Stepping[2]
SL3Z4 (MM#827856)[1]	1.55	256PBGA	133	B1
SL3Z5 (MM#827859)[1]	1.75	256PBGA	206	B1
GDS1110AB[1]	1.55	256PBGA	133	B2
GDS1110BB[1]	1.75	256PBGA	206	B2
GDS1110AC	1.55	256PBGA	133	B4
GDS1110BC	1.75	256PBGA	206	B4

Table 14-3 Package Marking Versus Revision Number

Package Markings	Voltage (V)	Package Type	Speed (MHz)	Stepping[2]
GDS1110AD	1.55	256PBGA	133	B5
GDS1110BD	1.75	256PBGA	206	B5

NOTES:
1. This device can no longer be ordered.
2. This value may be read from the ID register Register 0

116. Intel® StrongARM SA-1110 Device Identification (ID) Code Register: Section 16.6.2

The Stepping row of the table has had information for B5 added (as indicated in bold) and now appears as follows:

Stepping	Stepping revision of the SA-1110 0000 = A0 stepping 0100 = B0 stepping 0101 = B1 stepping 0110 = B2 stepping 1000 = B4 stepping **1001 = B5 stepping**

117. Boundary-Scan Interface Signals: Section 16.7

Removed the reference to note 8 in the last two rows of Table 16-1. The last two rows of this table now appear as follows:

Table 16-1. SA-1110 Boundary-Scan Interface Timing

Symbol	Parameter	Minimum	Typical	Maximum	Units	Notes
Tbsrs	**TMS** setup to TRr	10	—	—	ns	—
Tbsrh	**TMS** hold from TRr	10	—	—	ns	—

NOTES:
1. Assumes a 25-pF load on TDO. Output timing derates at 0.072 ns/pF of extra load applied.
2. TDO enable time applies when the TAP controller enters the Shift-DR or Shift-IR states.
3. TDO disable time applies when the TAP controller leaves the Shift-DR or Shift-IR states.
4. For correct data latching, the I/O signals (from the core and the pads) must be set up and held with respect to the rising edge of TCK in the CAPTURE-DR state of the SAMPLE/PRELOAD and EXTEST instructions.
5. Assumes that the data outputs are loaded with the ac test loads.
6. Data output enable time applies when the boundary-scan logic is used to enable the output drivers.
7. Data output disable time applies when the boundary scan is used to disable the output drivers.
8. TCK may be stopped indefinitely in either the low or high phase.

118. Boundary Scan Interface Signals: Section 16.7

Changed the introductory sentence for Table 16-1 to indicate that these are guidelines for timing signals. The updated sentence now appears as follows:

Table 16-1 shows the SA-1110 boundary-scan interface timing guidelines.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