

MITSUBISHI LSTTLs
M74LS92P

DIVIDE-BY-TWELVE COUNTER

DESCRIPTION

The M74LS92P is a semiconductor integrated circuit containing an asynchronous divide-by-twelve counter function with direct reset inputs.

FEATURES

- Direct reset input provided
- Usable independently as binary and divide-by-six counter
- High-speed counting ($f_{max} = 80\text{MHz}$ typical)
- Wide operating temperature range ($T_a = -20 \sim +75^\circ\text{C}$)

APPLICATION

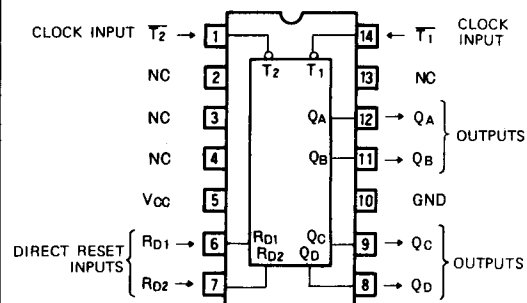
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

This device is composed of independent binary and divide-by-6 counters. Clock input \overline{T}_1 and output Q_A are employed for use as a binary counter while clock input \overline{T}_2 and Q_B , Q_C and Q_D are employed for use as a divide-by-6 counter. When employed as a divide-by-12 counter, Q_A and \overline{T}_2 are connected and by making \overline{T}_1 the input, the output appears in outputs Q_A , Q_B , Q_C and Q_D in accordance with the function table. The code appearing in the output is not pure binary code. Counting is performed when \overline{T}_1 and \overline{T}_2 are changed from high to low.

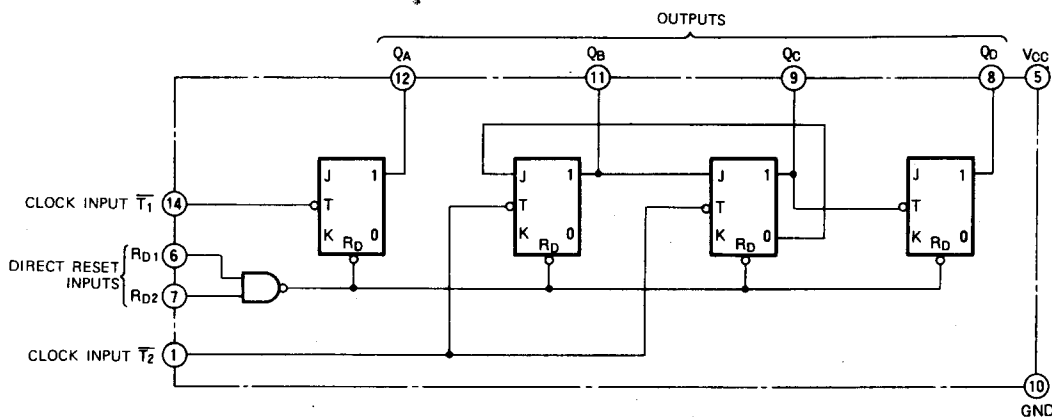
The binary and divide-by-6 counters can be reset simultaneously by setting direct reset inputs R_{D1} and R_{D2} high. For use as a counter, either R_{D1} or R_{D2} or both set low.

PIN CONFIGURATION (TOP VIEW)



Outline 14P4 NC : NO CONNECTION

BLOCK DIAGRAM



DIVIDE-BY-TWELVE COUNTER

FUNCTION TABLE (Note 1)

\bar{T}	R _{D1}	R _{D2}	Q _A	Q _B	Q _C	Q _D
X	H	H	L	L	L	L
↓	L	H	Count			
↓	H	L	Count			
↓	L	L	Count			

Note 1 ↓ : Transition from high to low
X : Irrelevant

Count number	Q _A	Q _B	Q _C	Q _D
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	L	L	H
7	H	L	L	H
8	L	H	L	H
9	H	H	L	H
10	L	L	H	H
11	H	L	H	H

ABSOLUTE MAXIMUM RATINGS

(T_a = -20 ~ +75°C, unless otherwise noted)

(1) Valid when Q_A and \bar{T}_2 are connected and \bar{T}_1 is made the input

Symbol	Parameter	Conditions	Limits	Unit
V _{CC}	Supply voltage		-0.5 ~ +7	V
V _I	Input voltage	Inputs \bar{T}_1, \bar{T}_2	-0.5 ~ +5.5	V
		Inputs R _{D1} , R _{D2}	-0.5 ~ +15	V
V _O	Output voltage	High-level state	-0.5 ~ V _{CC}	V
T _{opr}	Operating free-air ambient temperature range		-20 ~ +75	°C
T _{stg}	Storage temperature range		-65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = -20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V _{CC}	Supply voltage	4.75	5	5.25	V
I _{OH}	High-level output current	V _{OH} ≥ 2.7V	0	-400	μA
I _{OL}	Low-level output current	V _{OL} ≤ 0.4V	0	4	mA
		V _{OL} ≤ 0.5V	0	8	mA

ELECTRICAL CHARACTERISTICS (T_a = -20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ *	Max	
V _{IH}	High-level input voltage		2			V
V _{IL}	Low-level input voltage				0.8	V
V _{IC}	Input clamp voltage	V _{CC} = 4.75V, I _{IC} = -18mA			-1.5	V
V _{OH}	High-level output voltage	V _{CC} = 4.75V, V _I = 0.8V V _I = 2V, I _{OH} = -400μA	2.7	3.4		V
V _{OL}	Low-level output voltage	V _{CC} = 4.75V, I _{OL} = 4mA (Note 2)		0.25	0.4	V
		V _I = 0.8V, V _I = 2V, I _{OL} = 8mA (Note 2)		0.35	0.5	V
I _{IH}	High-level input current	R _{D1} , R _{D2}			20	μA
		\bar{T}_1	V _{CC} = 5.25V, V _I = 2.7V		40	
		\bar{T}_2			80	
		\bar{T}_1	V _{CC} = 5.25V, V _I = 5.5V		0.2	mA
\bar{T}_2			0.4			
I _{IL}	Low-level input current	R _{D1} , R _{D2}	V _{CC} = 5.25V, V _I = 10V		0.1	mA
		R _{D1} , R _{D2}	V _{CC} = 5.25V, V _I = 0.4V		-0.4	
		\bar{T}_1			-2.4	
		\bar{T}_2			-3.2	
I _{OS}	Short-circuit output current (Note 3)	V _{CC} = 5.25V, V _O = 0V	-20		-100	mA
I _{CC}	Supply current	V _{CC} = 5.25V (Note 4)		9	15	mA

* : All typical values are at V_{CC} = 5V, T_a = 25°C.

Note 2: Testing of output Q_A should be conducted with input \bar{T}_2 connected to output Q_A.

Note 3: All measurements should be done quickly and not more than one output should be shorted at a time.

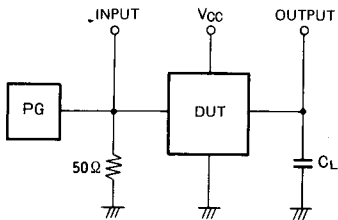
Note 4: I_{CC} is measured with \bar{T}_1 and \bar{T}_2 at 0V after R_{D1} and R_{D2} have been set to 0V from 4.5V.

DIVIDE-BY-TWELVE COUNTER

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^\circ C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock frequency, from input \overline{T}_1 to output Q_A	$C_L = 15\text{ pF}$ (Note 4)	32	80		MHz
f_{max}	Maximum clock frequency, from input \overline{T}_2 to output Q_B		16	30		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input \overline{T}_1 to output Q_A			7	16	ns
t_{PHL}	High-to-low-level, high-to-low-level output propagation time, from input \overline{T}_1 to output Q_A			8	18	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input \overline{T}_1 to output Q_D			25	48	ns
t_{PHL}	High-to-low-level, high-to-low-level output propagation time, from input \overline{T}_1 to output Q_D			25	50	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input \overline{T}_2 to output Q_B			7	16	ns
t_{PHL}	High-to-low-level, high-to-low-level output propagation time, from input \overline{T}_2 to output Q_B			8	21	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input \overline{T}_2 to output Q_C			8	16	ns
t_{PHL}	High-to-low-level, high-to-low-level output propagation time, from input \overline{T}_2 to output Q_C			10	21	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input \overline{T}_2 to output Q_D			15	32	ns
t_{PHL}	High-to-low-level, high-to-low-level output propagation time, from input \overline{T}_2 to output Q_D			15	35	ns
t_{PHL}	High-to-low-level output propagation time, from inputs R_{D1} , R_{D2} to outputs Q_A , Q_B , Q_C , Q_D			17	40	ns

Note 4: Measurement circuit

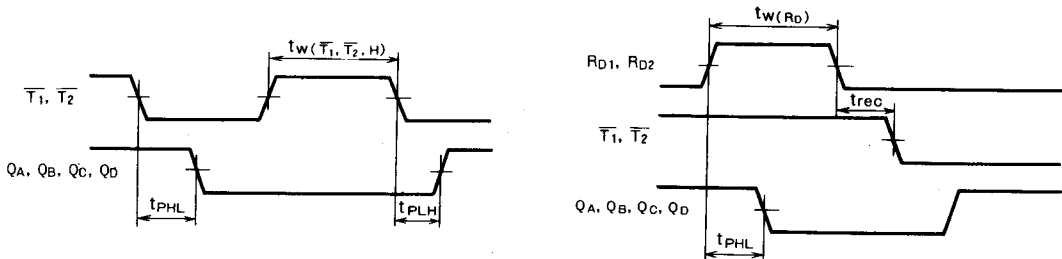


- (1) The pulse generator (PG) has the following characteristics:
 $PRR = 1\text{ MNz}$, $t_r = 6\text{ ns}$, $t_f = 6\text{ ns}$, $t_w = 500\text{ ns}$,
 $V_p = 3V_{p.p.}$, $Z_o = 50\Omega$.
- (2) C_L includes probe and jig capacitance

TIMING REQUIREMENTS ($V_{CC}=5V$, $T_a=25^\circ C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(\overline{T}_1H)}$	Clock input \overline{T}_1 high pulse width		15	6		ns
$t_{W(\overline{T}_2H)}$	Clock input \overline{T}_2 high pulse width		30	17		ns
$t_{W(R_D)}$	Direct reset R_{D1} , R_{D2} pulse width		15	5		ns
t_r	Clock pulse rise time			500	100	ns
t_f	Clock pulse fall time			200	100	ns
$t_{rec(R_D)}$	Recovery time R_{D1} , R_{D2} to \overline{T}_1 , \overline{T}_2		25	8		ns

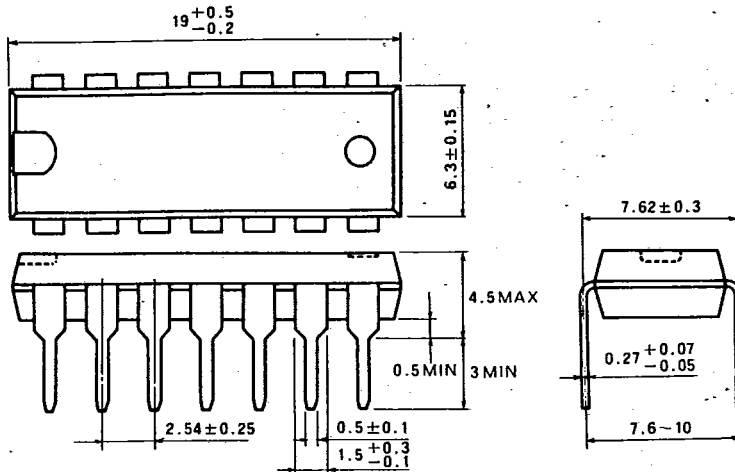
TIMING DIAGRAM (Reference level = 1.3V)



T-90-20

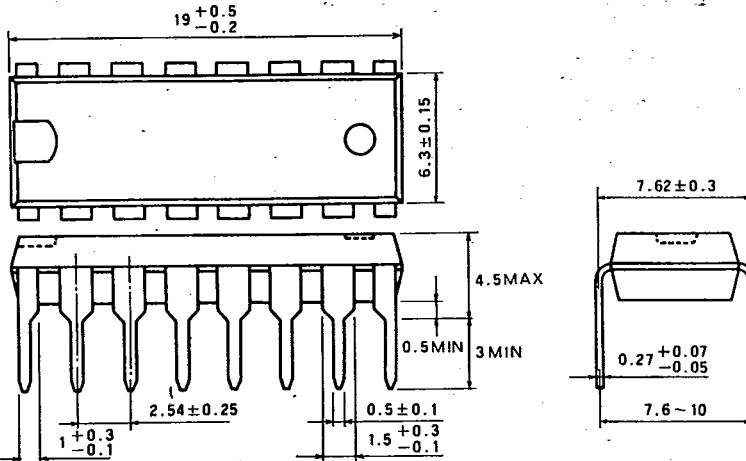
TYPE 14P4 14-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 20P4 20-PIN MOLDED PLASTIC DIL

Dimension in mm

