M74LS190P

SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER WITH MODE CONTROL

DESCRIPTION

The M74LS190P is a semiconductor integrated circuit containing a decade up/down counter function with up/down control and preset inputs.

FEATURES

- Up/down switching with up/down control input
- Asynchronous preset input provided
- Enable input provided
- Easy cascade connection possible
- High-speed counting (f_{max}= 38MHz typical)
- Wide operating temperature range (T_a= −20~+75°C)

APPLICATION

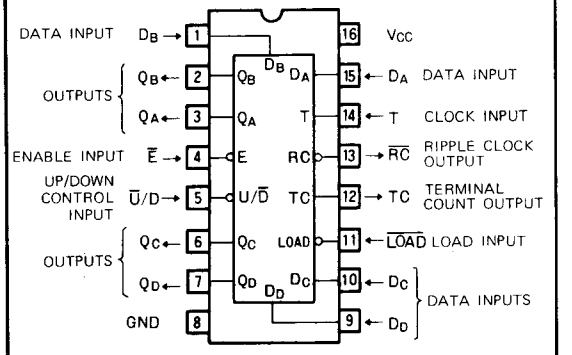
General purpose, for use in industrial and consumer equipment.

FUNCTIONAL DESCRIPTION

When enable input $\overline{E}$ is low, load input $\overline{LOAD}$ is high and the count pulses are applied to clock input T, the number of count pulses appear as a BCD code in the outputs Q_A, Q_B, Q_C and Q_D in synchronization with the count pulses. When the up/down control input $\overline{U}/D$ is made low, count-up begins and when made high, count-down begins. Counting is performed when T changes from low to high.

Presetting is performed regardless of the count pulses and by applying the data to data inputs D_A, D_B, D_C and D_D and by setting $\overline{LOAD}$ low, the D_A, D_B, D_C and D_D signals appear in outputs Q_A, Q_B, Q_C and Q_D irrespective of the status of the other inputs and the count can be preset. Counting proceeds as per the status transition diagram with presetting to a numerical value of 10_2 or higher.

PIN CONFIGURATION (TOP VIEW)

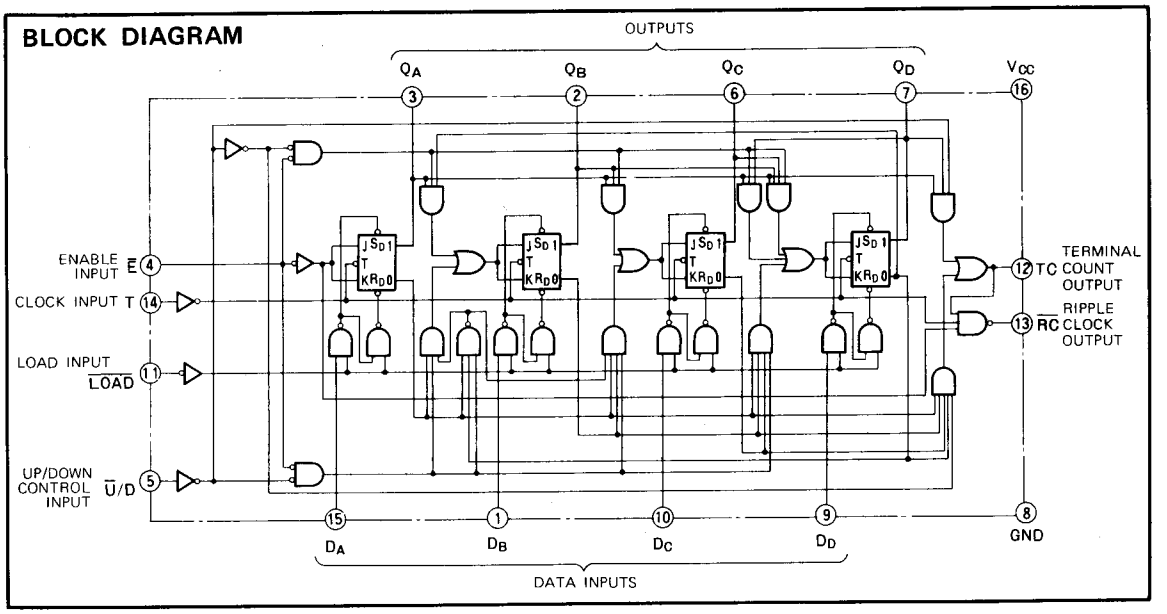


Outline 16P4

High appears in the terminal count output TC during count-up while 9_2 appears in Q_A, Q_B, Q_C and Q_D and during count-down while 0_2 appears. Low appears in the ripple clock output $\overline{RC}$ only when $\overline{E}$ and T are low and 9_2 appears in outputs Q_A, Q_B, Q_C and Q_D during count-up or 0_2 appears in the outputs during count-down. $\overline{E}$, TC and $\overline{RC}$ are used when cascade-connecting the counter. (Refer to application examples.)

$\overline{E}$ can be changed from high to low irrespective of the status of T but when changed from low to high, T must be high. Perform the change for $\overline{U}/D$ when T is high.

BLOCK DIAGRAM



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FUNCTION TABLE (Note 1)

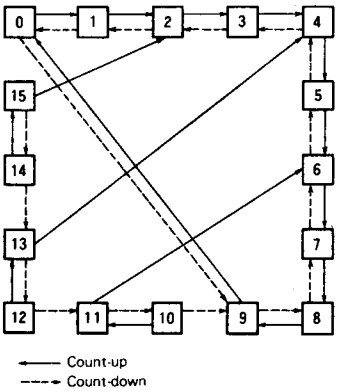
$\overline{LOAD}$	$\overline{E}$	$\overline{U}/D$	T	Q_A	Q_B	Q_C	Q_D
L	X	X	X	D_A	D_B	D_C	D_D
H	L	L	↑	Count-up			
H	L	H	↑	Count-down			
H	H	X	X	Inhibit			

Note 1. ↑ : Transition from low to high
X : Irrelevant

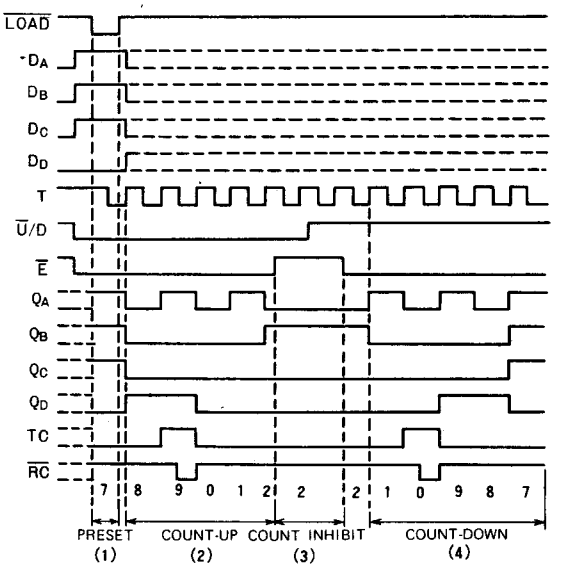
$\overline{E}$	TC(1)	T	$\overline{RC}$
L	H	L	L
L	H	H	H
H	X	X	H
X	L	X	H

TC is the output but the signal generated internally by the following logical expression.
$TC = Q_A \cdot Q_D \cdot (\overline{U/D})$ ..... Count-up
$TC = \overline{Q_A} \cdot \overline{Q_B} \cdot \overline{Q_C} \cdot \overline{Q_D} \cdot (\overline{U}/D)$ ..... Count-down

STATE DIAGRAM



OPERATION TIMING DIAGRAM



Details of timing diagram
(1) Preset to 13
(2) Count-up 8, 9, 0, 1, 2
(3) Count inhibit
(4) Count-down 1, 0, 9, 8, 7

ABSOLUTE MAXIMUM RATINGS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		−0.5 ~ +7	V
V_I	Input voltage		−0.5 ~ +15	V
V_O	Output voltage	High-level state	−0.5 ~ V_{CC}	V
Topr	Operating free-air ambient temperature range		−20 ~ +75	°C
Tstg	Storage temperature range		−65 ~ +150	°C

RECOMMENDED OPERATING CONDITIONS (T_a = −20 ~ +75°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{OH}	High-level output current	$V_{OH} \geqq 2.7V$	0		−400	μA
I_{OL}	Low-level output current	$V_{OL} \leqq 0.4V$	0		4	mA
		$V_{OL} \leqq 0.5V$	0		8	mA

SYNCHRONOUS PRESETTABLE UP/DOWN DECADE COUNTER WITH MODE CONTROL

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75°C$, unless otherwise noted)

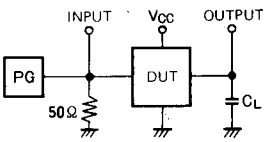
Symbol	Parameter		Test conditions		Limits			Unit
					Min	Typ *	Max	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IC}	Input clamp voltage		$V_{CC}=4.75V$, $I_{IC}=-18mA$				−1.5	V
V_{OH}	High-level output voltage		$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$, $I_{OH}=-400\mu A$		2.7	3.4		V
V_{OL}	Low-level output voltage		$V_{CC}=4.75V$, $V_I=0.8V$, $V_I=2V$	$I_{OL}=4mA$		0.25	0.4	V
				$I_{OL}=8mA$		0.35	0.5	V
I_{IH}	High-level input current	$T, \overline{LOAD}, U/\overline{D}, D_A \sim D_D$	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
		$\overline{E}$					60	
		$T, \overline{LOAD}, U/\overline{D}, D_A \sim D_D$	$V_{CC}=5.25V$, $V_I=10V$				0.1	mA
		$\overline{E}$					0.3	
I_{IL}	Low-level input current	$T, \overline{LOAD}, U/\overline{D}, D_A \sim D_D$	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
		$\overline{E}$					−1.2	
I_{OS}	Short-circuit output current (Note 2)		$V_{CC}=5.25V$, $V_O=0V$		−20		−100	mA
I_{CC}	Supply current		$V_{CC}=5.25V$ (Note 3)			20	35	mA

* : All typical values are at V_{CC} = 5V, Ta = 25°C.
Note 2. All measurements should be done quickly and not more than one output should be shorted at a time.
Note 3. I_{CC} is measured with all the inputs at 0V.

SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
f_{max}	Maximum clock freqency	$C_L=15pF$ (Note 4)	20	40		MHz
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, input $\overline{LOAD}$ to outputs Q_A, Q_B, Q_C, Q_D			19	33	ns
t_{PHL}				25	50	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from inputs D_A, D_B, D_C, D_D to outputs Q_A, Q_B, Q_C, Q_D			11	32	ns
t_{PHL}				25	40	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T to output $\overline{RC}$			11	20	ns
t_{PHL}				11	24	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T to outputs Q_A, Q_B, Q_C, Q_D			12	24	ns
t_{PHL}				14	36	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input T to output TC			20	42	ns
t_{PHL}				24	52	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $U/\overline{D}$ to output $\overline{RC}$			22	45	ns
t_{PHL}				20	45	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $U/\overline{D}$ to output TC			15	33	ns
t_{PHL}				15	33	ns
t_{PLH}	Low-to-high-level, high-to-low-level output propagation time, from input $\overline{E}$ to output $\overline{RC}$			10	33	ns
t_{PHL}				11	33	ns

Note 4: Measurement circuit



(1) The pulse generator (PG) has the following characteristics:
PRR = 1MHz, t_r = 6ns, t_f = 6ns, t_W = 500ns,
$V_P = 3V_{P\text{-}P}$, $Z_O = 50\Omega$
(2) C_L includes probe and jig capacitance

TIMING REQUIREMENTS ($V_{CC}=5V$, $T_a=25°C$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{W(TL)}$	Clock input T low pulse width		25	9		ns
$t_{W(\overline{LOAD})}$	Load $\overline{LOAD}$ pulse width		35	10		ns
tr	Clock pulse rise time			2000	100	ns
$t_{SU(D)}$	Setup time $D_A \sim D_D$ to $\overline{LOAD}$		20	9		ns
$t_{SU(\overline{EL})}$	Setup time $\overline{E}$ low to T		40	24		ns
$t_{h(D)}$	Hold time $D_A \sim D_D$ to $\overline{LOAD}$		5	0		ns
$t_{h(\overline{EL})}$	Hold time $\overline{E}$ low to T		5	2		ns
$t_{rec(\overline{LOAD})}$	Recovery time $\overline{LOAD}$ to T		20	16		ns

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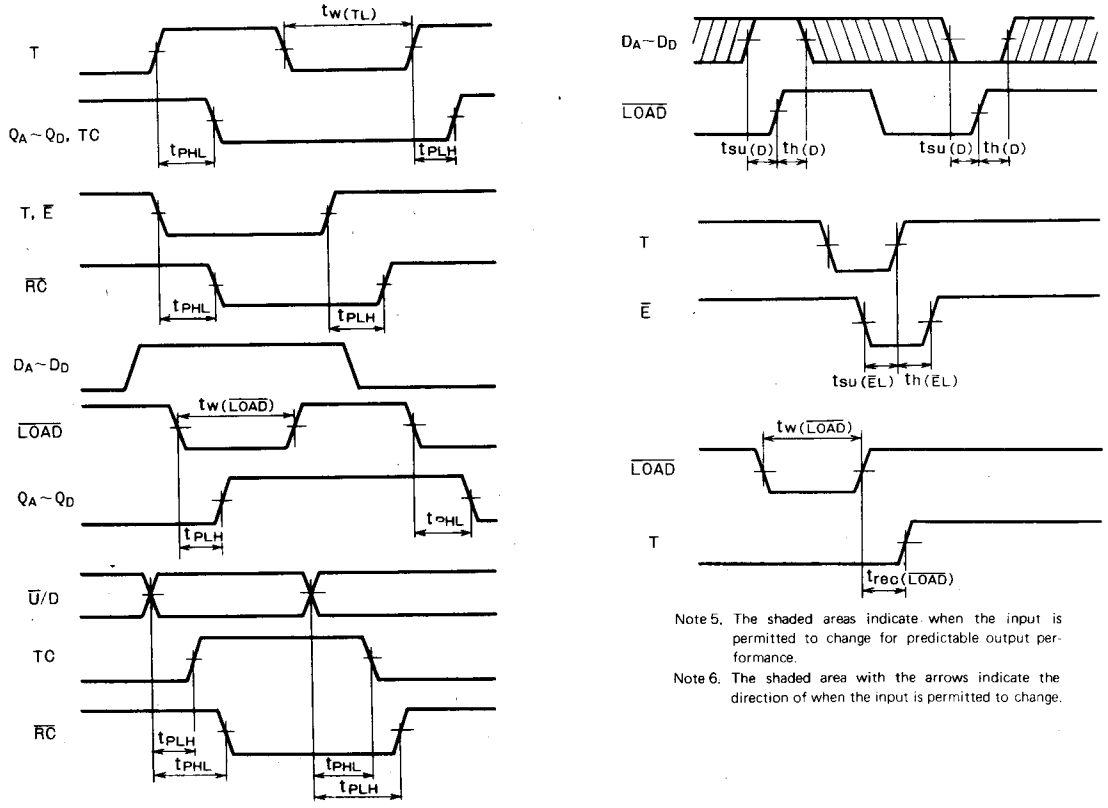
TIMING DIAGRAM (Reference level = 1.3V)

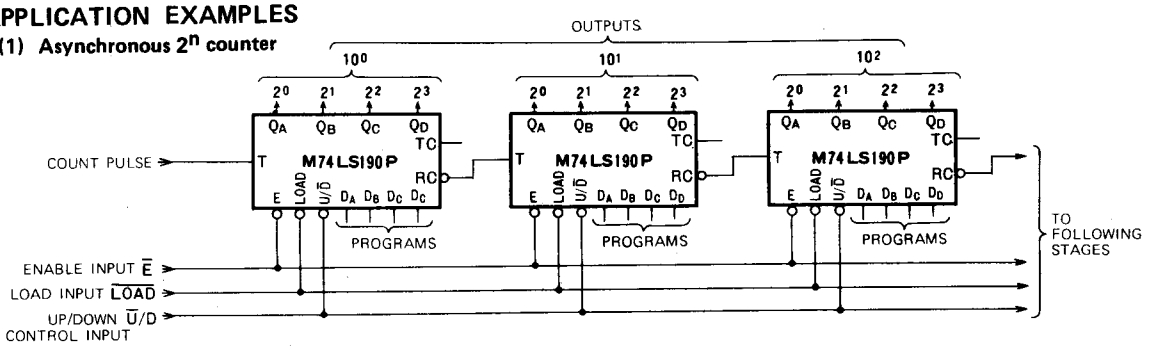


Note 5. The shaded areas indicate when the input is permitted to change for predictable output performance.

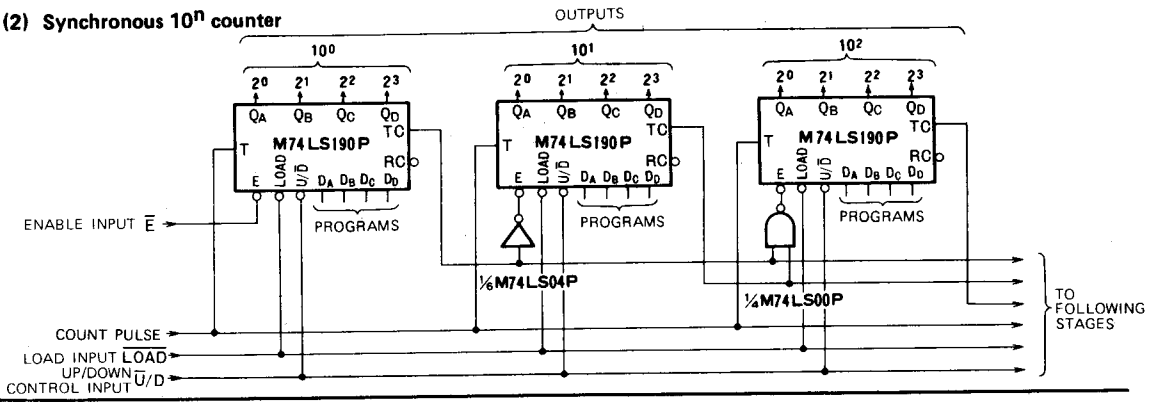
Note 6. The shaded area with the arrows indicate the direction of when the input is permitted to change.

APPLICATION EXAMPLES

(1) Asynchronous 2^n counter



(2) Synchronous 10^n counter



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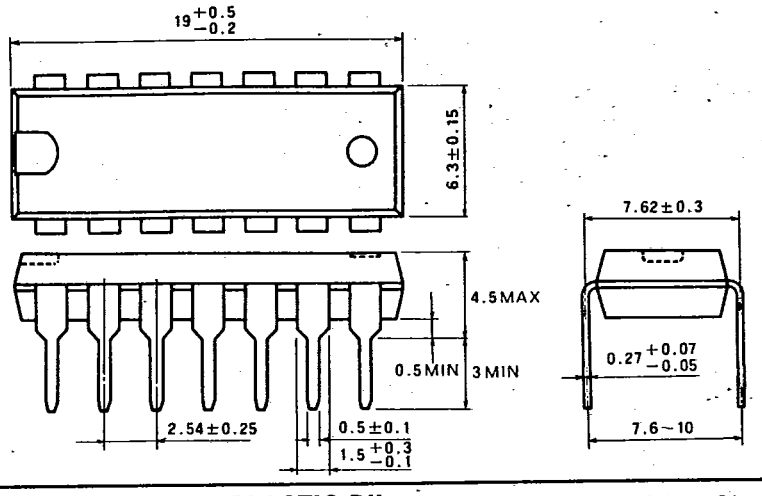
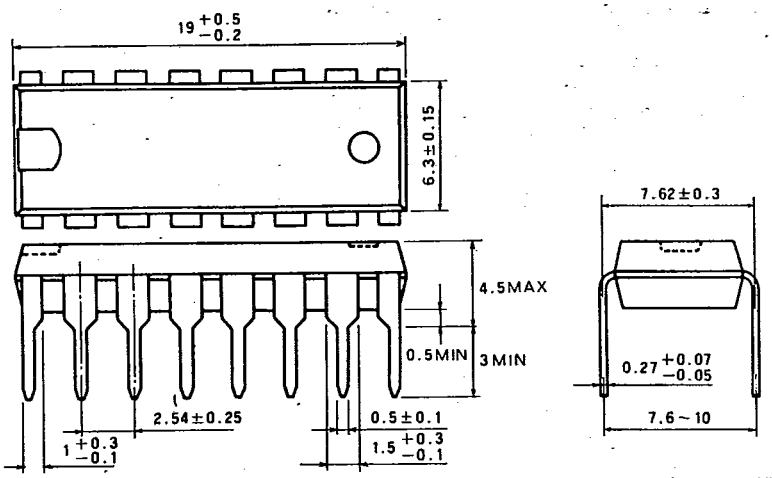
TYPE 14P4 14-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 16P4 16-PIN MOLDED PLASTIC DIL

Dimension in mm



TYPE 20P4 20-PIN MOLDED PLASTIC DIL

Dimension in mm