ISSUE 3 January 1993

Features

- Timeslot interchange circuit for digital switch applications
- 16 bit wide data bus I/O
- 2048 x 16 bit wide byte capacity
- Dual addressing capability; internal counter and external address bus
- Variable clock and frame rates
- Microprocessor interface
- CMOS

Applications

- Building block for digital switching matrices used in PBXs, CO equipment, data switching, etc.
- Programmable delay lines

Ordering Information

MT9080AP 84 Pin PLCC

-40°C to 70°C

Description

The MT9080 is a flexible memory module suitable for use as a basic building block in the construction of large digital switching matrices. It can be configured as either a Data Memory or a Connection Memory. Interface to the device is via 16 bit wide data and address busses. The MT9080 can operate with variable clock rates up to 16.7 MHz.

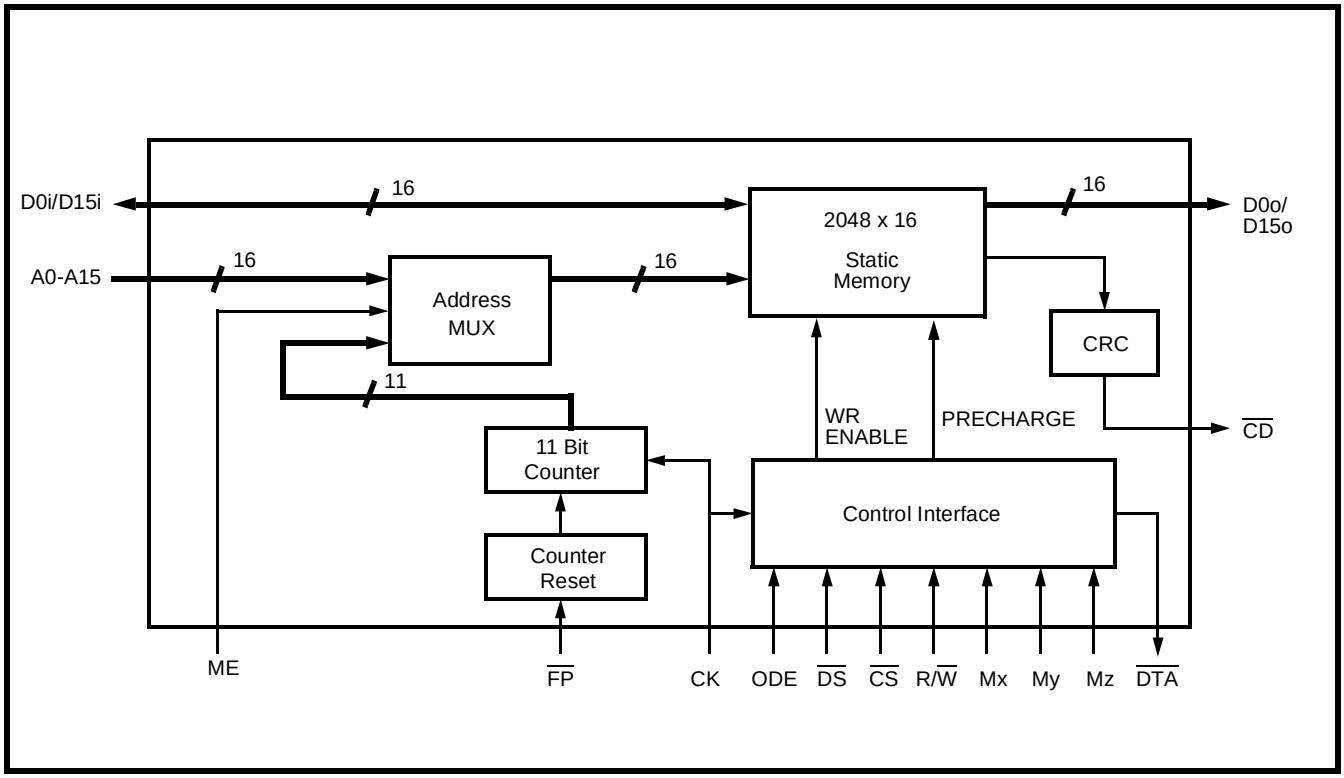


Figure 1 - Functional Block Diagram

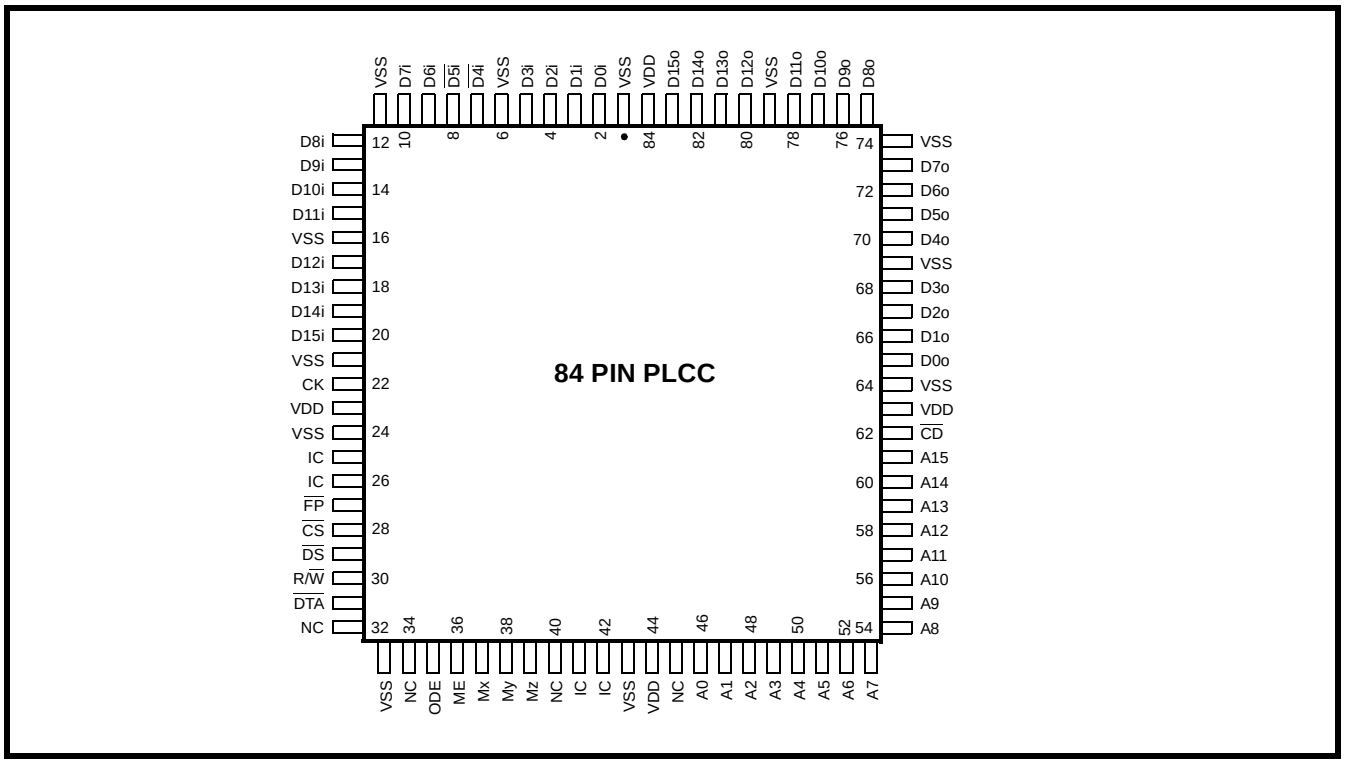


Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
1	**V_{SS}**	Ground.
2-5	**D0i-D3i**	**Input/Microport Data Bus.** This is part of a 16 bit data bus. The data bus is bidirectional in Connect Memory mode where it is typically interfaced to a microprocessor. In all other modes the data bus is an input. Data to be switched through the device is clocked in at this port.
6	**V_{SS}**	Ground.
7-10	**D4i-D7i**	**Input/Microport Data Bus.** See description for pins 2-5 above.
11	**V_{SS}**	Ground.
12-15	**D8i-D11i**	**Input/Microport Data Bus.** See description for pins 2-5 above.
16	**V_{SS}**	Ground.
17-20	**D12i-D15i**	**Input/Microport Data Bus.** See description for pins 2-5 above.
21	**V_{SS}**	Ground.
22	**CK**	**Clock.** Master clock input which is used to clock data into and out of the device. It also clocks the internal 11 bit counter.
23	**V_{DD}**	+5V supply input .
24	**V_{SS}**	Ground.
25,26	**IC**	**Internal Connection.** Should be tied to V_{SS} for normal operation.
27	**$\overline{FP}$**	**Frame Pulse.** An active low signal that serves as a synchronous clear for the internal 11 bit counter in all modes except Shift Register mode. The counter is cleared on a rising edge of CK. In the Shift Register mode, $\overline{FP}$ serves to align channel boundaries.

Pin Description

Pin #	Name	Description
28	$\overline{CS}$	**Chip Select.** Active Low input. Selects the device for microport access in connect memory, data memory, external and shift register modes. Tying $\overline{CS}$ high will disable output data drivers (D0-D15o) in all modes except connect memory and shift register modes.
29	$\overline{DS}$	**Data Strobe.** Active low input. Indicates to the SMX that valid data is present on the microport data bus during a write operation or that the SMX must output data on a read operation. In Connect Memory modes, a low level applied to this input during a write operation indicates to the SMX that valid data is present on the microport data bus. During a read operation the low going signal indicates to the SMX that it must output data on the microport data bus. In Data Memory and External modes, when $\overline{DS}$ is high, the output data bus D0o-D15o will be disabled. The input data bus D0i-D15i is not affected. The $\overline{DS}$ input has no effect on the input and output busses in Counter or Shift Register modes.
30	R/$\overline{W}$	**Read/Write Enable.** Data is written into the device when R/$\overline{W}$ is low and read from it when it is high. This control input is disabled in data memory and shift register modes. It should be tied to V_{SS} or V_{DD} in these modes. In counter and external modes, the state of R/$\overline{W}$ pin is clocked in with the rising edge of CK. The actual read or write operation will be implemented on the next rising clock edge.
31	$\overline{DTA}$	**Data Transfer Acknowledge.** Open drain output which is pulled low to acknowledge completion of microport data transfer. On a read of the SMX, $\overline{DTA}$ low indicates that the SMX has put valid data on the data bus. On a write, $\overline{DTA}$ low indicates that the SMX has completed latching the data in.
32	NC	**No Connection.**
33	V_{SS}	Ground.
34	NC	**No Connection.**
35	ODE	**Output Data Enable.** Control input which enables the output data bus. Pulling this input low will place the data bus in a high impedance state. The level on this pin is latched by a rising edge of CK. The output drivers will be enabled or disabled with the rising edge in the next timeslot (see Fig. 24 for applicable timing in different modes).
36	ME	**Message Enable.** When tied high the data latched in on the address bus is clocked out on D0o-D15o. When ME is tied low, the contents of the addressed memory location will be output on the bus. The level on this pin is latched in with the rising edge of the clock. The actual mode change is implemented on the rising edge in the next timeslot. Refer to Figures 25 and 26 for more timing information.
37	Mx	**Mode X.** One of three inputs which permit the selection of different operating modes for the device. Refer to Table 1 for description of various modes.
38	My	**Mode Y.** See description for pin 37.
39	Mz	**Mode Z.** See description for pin 37.
40	NC	**No Connection.**
41, 42	IC	**Internal Connection.** Leave open for normal operation.
43	V_{SS}	Ground.
44	V_{DD}	Supply Voltage. +5V .
45	NC	**No Connection.**

Pin Description

Pin #	Name	Description
46-61	**A0-A15**	**Address Bus.** These inputs have three different functions. Inputs A0-A10 are used to address internal memory locations during read or write operations in all modes except Shift Register mode. In Shift Register mode, the levels latched in on A0-A10 program the delay through the device. When the ME pin is tied high, the data latched in on A0-A15 is clocked out on to the data bus (D0o-D15o).
62	**$\overline{CD}$**	**Change Detect.** Open drain output which is pulled low when a change in the memory contents from one frame to the next is detected by a Cyclic Redundancy Check ($\overline{CRC}$). Changes in memory contents resulting from microprocessor access do not cause $\overline{CD}$ to go low. The output is reset to its normal high impedance state when the $\overline{DS}$ input is strobed, while the device has been selected ($\overline{CS}$ is low).
63	**V_{DD}**	Supply Voltage. +5V .
64	**V_{SS}**	Ground.
65-68	**D0o-D3o**	**Output Data Bus.** These three state outputs are part of a 16 bit data bus which is used to clock out data from the device. Data is clocked out with the rising edge of the clock. See Figures 24 to 26 for timing information. The bus is actively driven when ODE is tied high. It is disabled when ODE is tied low. Tying $\overline{CS}$ high will also disable the output data bus in all modes except Connect Memory and Shift Register Modes.
69	**V_{SS}**	Ground.
70-73	**D4o-D7o**	**Output Data Bus.** See description for pins 65-68.
74	**V_{SS}**	Ground.
75-78	**D8o-D11o**	**Output Data Bus.** See description for pins 65-68.
79	**V_{SS}**	Ground.
80-83	**D12o-D15o**	**Output Data Bus.** See description for pins 65-68.
84	**V_{DD}**	Supply Voltage. +5V .

Functional Description

The SMX is a flexible memory module suitable for use in the construction of timeslot interchange circuits used in PCM voice or data switches. The device can be configured as a data memory or a connection memory.

The SMX has separate 16 bit input and output data busses. A 16 bit address bus and a full microprocessor interface is also provided.

Data is clocked into and out of the device with the signal applied at the CK (clock) input. Depending on the mode of operation, the memory locations for the read or write operation can be addressed sequentially by the internal counter or randomly via the external address bus. A messaging sub-mode, which permits the data latched in on the address bus to be multiplexed on to the output data bus, is also available (see ME pin description).

The SMX ensures integrity of the stored data by performing a Cyclic Redundancy Check (CRC) on a per frame basis. When a change in the memory contents is detected from one frame to the next, the Change Detect ($\overline{CD}$) pin is pulled low. The output will be reset to its normal high impedance state when $\overline{DS}$ input is strobed while $\overline{CS}$ is low (i.e., while the device has been selected for microprocessor access). The $\overline{CD}$ output is not pulled low when the memory contents have been modified by a processor access to the device.

Modes Of Operation

The SMX can be programmed to operate in one of eight modes as summarized in Table 1. The different modes are used to realize specific switch implementations. For example, to implement a 1024 channel switch, two SMXs are required. One is operated in Data Memory mode, while the second is operated in Connect Memory mode. A 2048 channel switch can be realized using three SMXs. Two of the devices are operated, alternatively, in Counter and External modes, the third serves as the Connection Memory. A detailed description of the implementation is presented in the Applications section of this data sheet. An outline of the device functionality in each mode is presented below.

Mode	M_X	M_Y	M_Z	Name	Abbr.
1	0	0	0	Data Memory - 1	DM-1
2	0	0	1	Data Memory - 2	DM-2
3	0	1	0	Connect Memory - 1	CM-1
4	0	1	1	Connect Memory - 2	CM-2
5	1	0	0	Counter Mode	CNT
6	1	0	1	External Mode	EXT
7	1	1	0	Shift Register Mode	SR
8	1	1	1	Data Memory - 3	DM-3

Table 1. SMX Modes of Operation

Data Memory Mode-1

Data Memory Mode-1 is designed for use in the construction of a 1024 Channel Switch Matrix. Data on the D0-D15 input bus is clocked into the SMX and stored in memory locations addressed by the internal 11 bit counter. Data is clocked out according to the addresses asserted on the address bus. The pin configuration of the device in this mode is illustrated in Fig .3

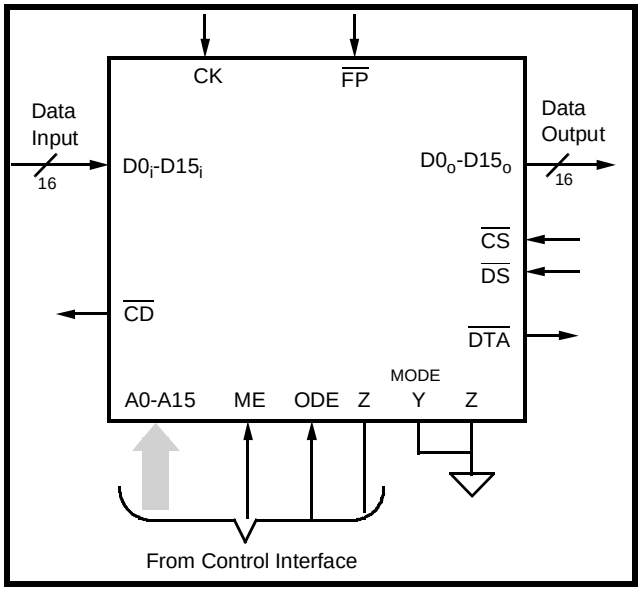
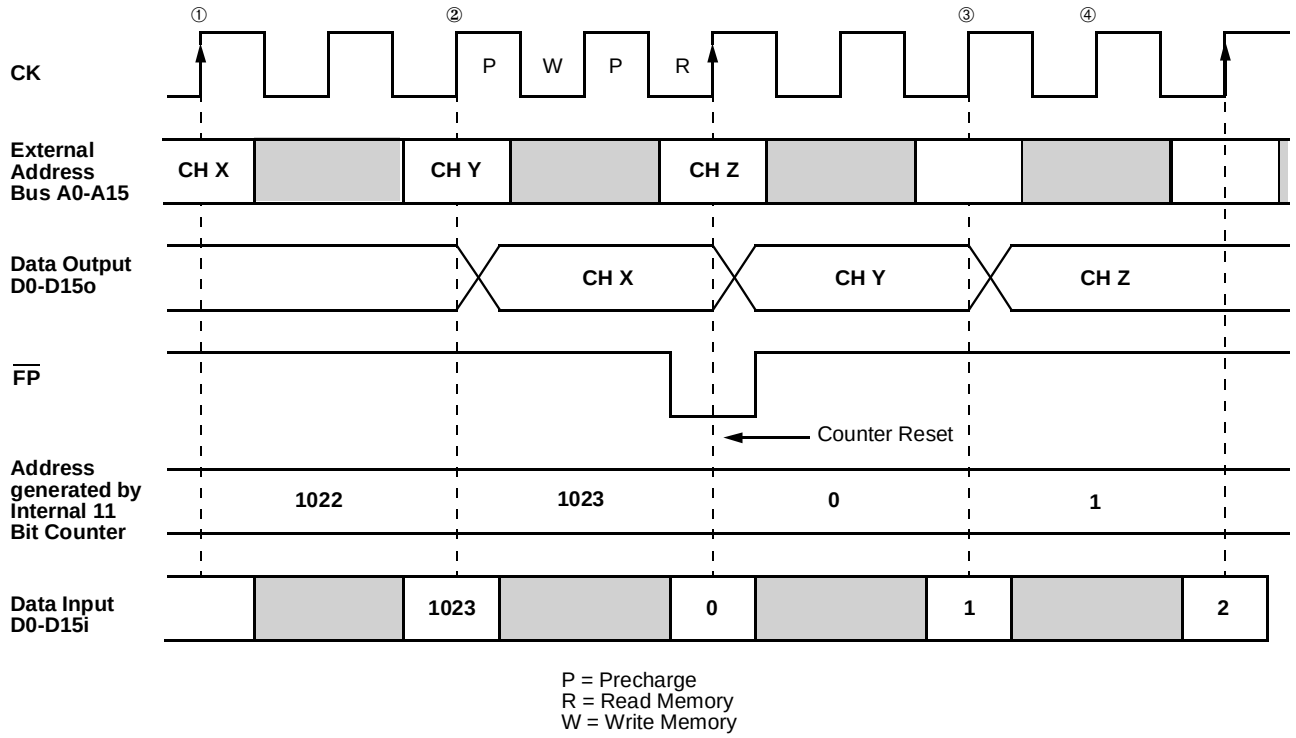


Fig. 3 - Data Memory Modes 1 and 2 Pinout

The timing for the read and write operation is illustrated in Fig. 4. The first half of each clock period is used for precharging the internal bus. Data is latched in and out of the device with rising edge of the CK clock. Correct operation of the device in this mode requires 2048 clock cycles in a single frame defined by the frame pulse. Consequently, for switching of 64 kbit/s PCM voice channels, the clock frequency must be 16.384 Mbit/s with a frame rate of 8 kHz.

The address supplied on the address bus is latched in with the first positive clock edge in a channel timeslot. The contents of the memory location addressed will be clocked out on D0-D15o with the first positive clock edge in the next timeslot (see Fig. 4).

In Data Memory Mode-1, the delay through the switch depends on the number of channel timeslots between the input channel and the output channel. If the time difference between the input channel and output channel is less than two channels, data clocked into the device in the current frame will be clocked out in the next frame. If the difference is greater than or equal to two channels, data will be clocked out in the same frame. This concept is further illustrated in Fig. 5.

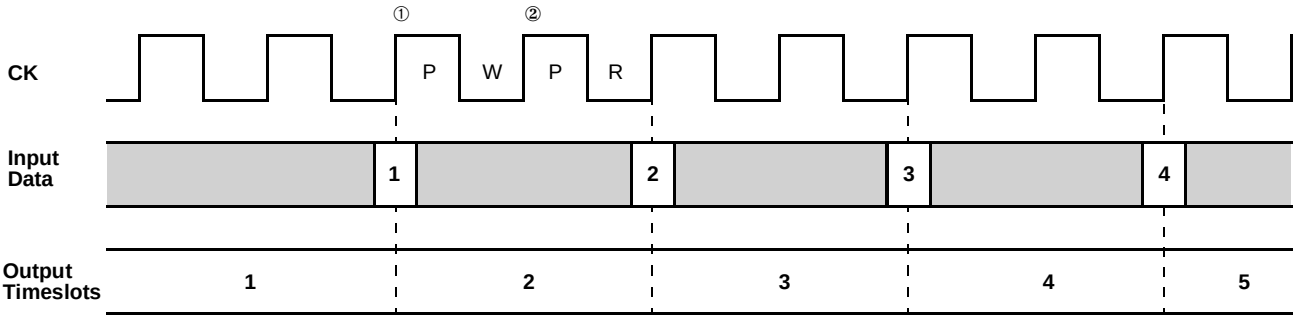


P = Precharge
R = Read Memory
W = Write Memory

Data is clocked out of the memory location addressed by external address bus. The address is latched in with CK edge marked ①. Data is clocked out with CK edge marked ②.

Data is latched into the device with the last rising edge of CK in the timeslot (e.g., edge ③ in diagram). It is stored in the memory location address by the internal 11 bit counter with the next rising clock edge (edge ④ in diagram).

Figure 4 - Data Memory Mode Functional Timing



P = Precharge
R = Read Memory
W = Write Memory

Data on the input bus of the SMX is latched into the device with last rising edge of the clock within a timeslot. It is written into the internal memory with the following positive edge.

Data is clocked out of the memory location and latched onto the output data bus with first positive clock edge in the timeslot.

Switching channel 1 to channel 1 or channel 2 will result in one frame delay. Note that channel 2 is clocked out by CK edge labelled ① while channel 1 is written into the memory with edge ②. However, if channel 1 is switched to channel 3, there will be only one channel delay.

Figure 5 - Throughput Delay in Data Memory Mode-1

This mode provides minimum delay through the SMX for any switching configuration.

Data Memory Mode-2

Data Memory Mode-2 is designed for use in constructing a 1024 by 1024 channel double buffered switch. This mode is similar in most respects to Data Memory Mode-1. The double buffering is achieved by dividing the internal 2048 memory into two equal blocks. In a single frame, data is written into the first block and read from the second. In the next frame, the data will be written into the second and read from the first (see Figure 6). Frame sequence integrity of the data will be maintained for all switching configurations if the output frame is delayed by one channel with respect to the input frame. In this case, data clocked into the device during any of the channels in the current frame will be clocked out in the next frame. However, if the input and output frames are aligned, then data switched from any input channel to output channels 0 or 1 will be clocked out one frame after the next - consequently frame sequence integrity is not maintained for channels 0 or 1. Frame sequence integrity will be maintained for data switched to any of the other output channels. (See SMX/PAC Application Note, MSAN-135, for more information.)

It is possible to switch between Data Memory Mode-1 and Mode-2 on a per timeslot basis.

Data Memory Mode-3

This mode is similar to Data Memory Mode-1. However, there is no restriction on the minimum acceptable clock frequency or frame rate. In this mode, the size of the switching matrix depends on the clock and frame rates provided as per the following relationship:

$$S = \frac{F_{CK}}{2 X F_{FP}}$$

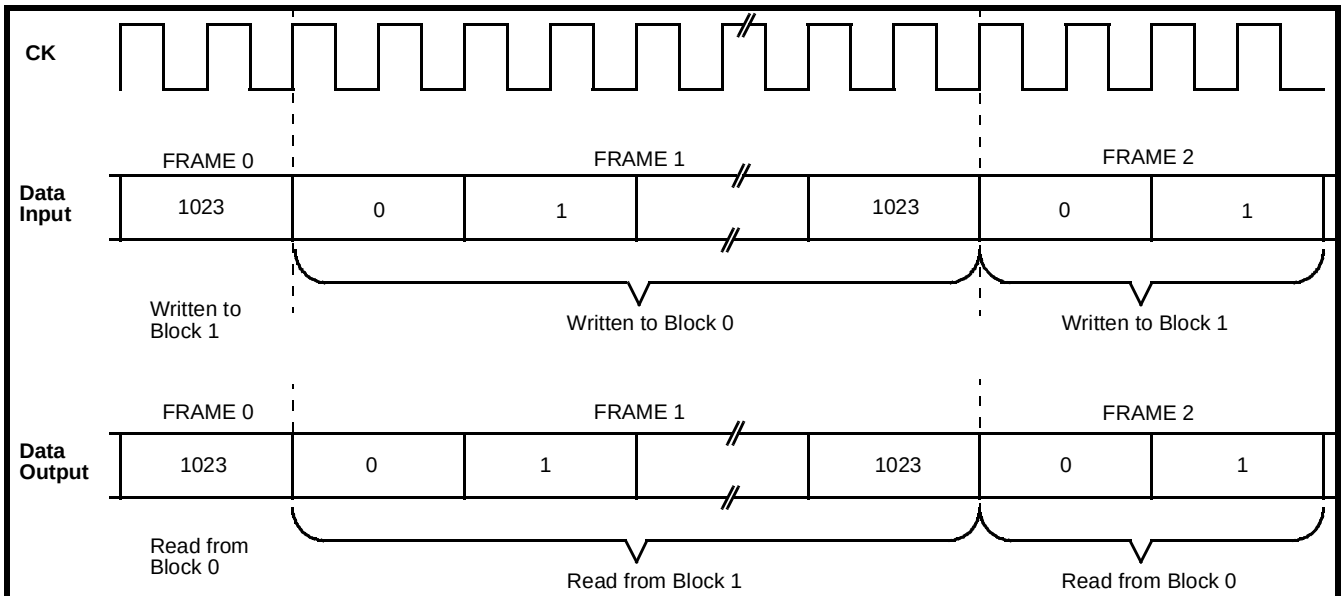
where S is the number of channels in the switching matrix F_{FP} is the frame pulse frequency in Hz, and F_{CK} is the clock frequency in Hz. The following table shows how the size of a switching matrix can be varied by selecting a suitable combination of clock and frame rates.

CK (kHz)	$\overline{FP}$ (kHz)	Number of channels in the switching matrix
16.384	4	2,048
16.384	8	1,024
16.384	16	512
12.288	4	1,536
12.288	8	768
8.192	4	1,024
8.192	8	512

It is not possible to switch between Data Memory Mode-3 and other modes on per-timeslot basis.

Connect Memory Mode -1

In Connect Memory Mode-1, the input data bus is bidirectional. Internal memory locations can be randomly accessed via the microprocessor bus. The pinout of the device in this mode is illustrated in Figure 7.



Note: No input and output channel alignment is implied in the example shown above. It is assumed that the frame pulse for the connection memory used to generate adresses for the read operation has a specific phase relationship with respect to the Data Memory frame pulse.

Figure 6 - Data Memory Mode-2 Functional Timing

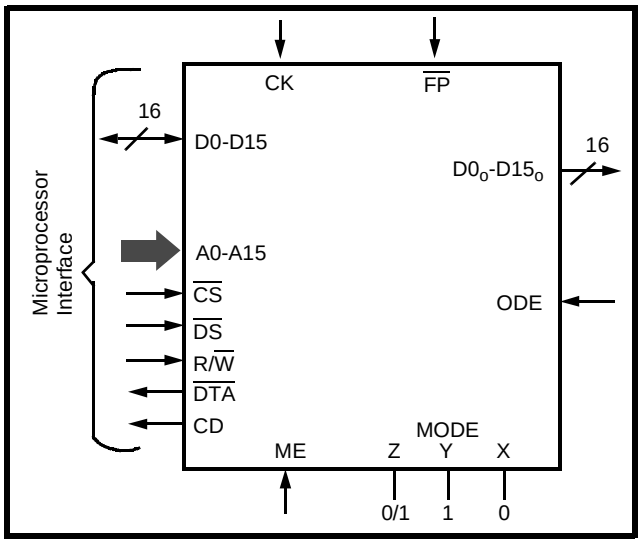


Fig. 7 - Connect Memory Modes Pinout

Data is clocked out on $D0_o$-$D15_o$ from memory locations addressed sequentially by the internal counter. This counter is incremented every second clock period and is reset with FP. The frequency of the clock signal used should be twice the data rate.

A timing diagram showing the relationship between the data output and the clock signal is presented in Fig. 8. With a clock rate of 16.384 MHz, the maximum number of addresses that can be generated in an 8 kHz frame period is 1024.

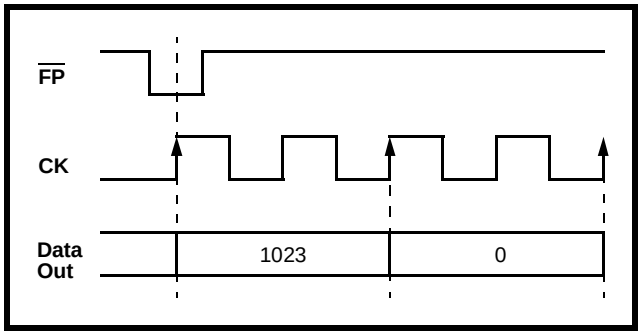


Fig. 8 - Connect Memory Mode-1 Functional Timing

Microprocessor access timing is shown in Figures 28 and 29. During a microprocessor read cycle, DS low indicates to the SMX that the processor is ready to receive data. The SMX responds by pulling DTA low when there is valid data present on the bus. The processor latches the data in and sets DS high. The SMX completes the bus cycle by disabling the DTA. DS should be kept low until after DTA is issued by the SMX. CS, R/W and the address lines should also be asserted for the duration of the access. A MPU write cycle is similar to the read cycle. Data will be latched into the device approximately three clock (CK) cycles after DS goes low. When the device has latched the data in, it will pull DTA low. DS can subsequently be set high.

Connect Memory Mode-2

Connect Memory Mode-2 is designed specifically for 2048 channel switching applications. Data is clocked out on $D0_o$-$D15_o$ with every rising clock edge from memory locations addressed sequentially by the internal counter (see Figure 9). This counter is incremented with each clock period and is reset with FP or when a count of 2047 is reached.

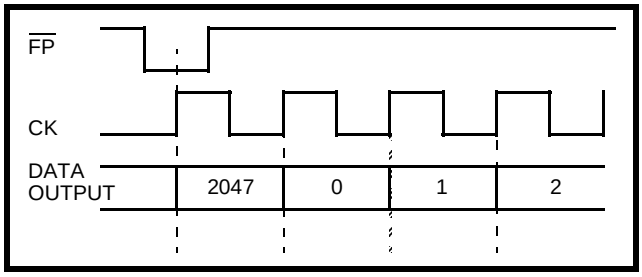


Fig. 9 - Connect Memory Mode-2 Functional Timing

The clock frequency should be 16.384 MHz for a connection memory designed to support a 2048 channel switch.

Microprocessor access is similar to Connect Memory Mode-1.

Counter Mode

This mode is designed for 2048 channel switching applications. In the counter mode all read and write addresses are generated sequentially by the internal 11 bit counter. The 11 bit counter is incremented with each clock pulse. It will wrap around when it reaches a count of binary 2047 or when it is reset by FP. The active input/output pins in this mode are illustrated in Fig. 10.

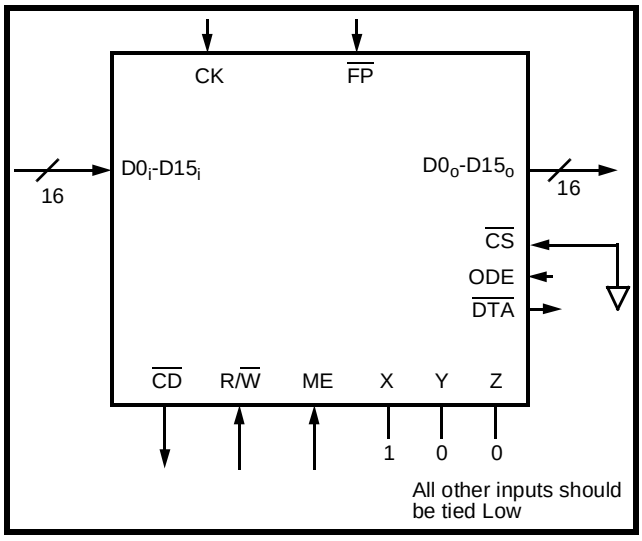


Fig. 10 - Counter Mode Pinout

The device can perform either a read or a write, depending on the level asserted at the R/$\overline{W}$ pin. When R/$\overline{W}$ is high, the contents of the memory addressed by the internal counter will be clocked out on to the output data bus. Setting R/$\overline{W}$ low will enable data on the input data bus to be written into the device. During a write operation, the output bus is actively driven by the data latched out in the previous read operation.

Data is clocked in or out of the device on the positive edge of the clock. See Fig. 11.

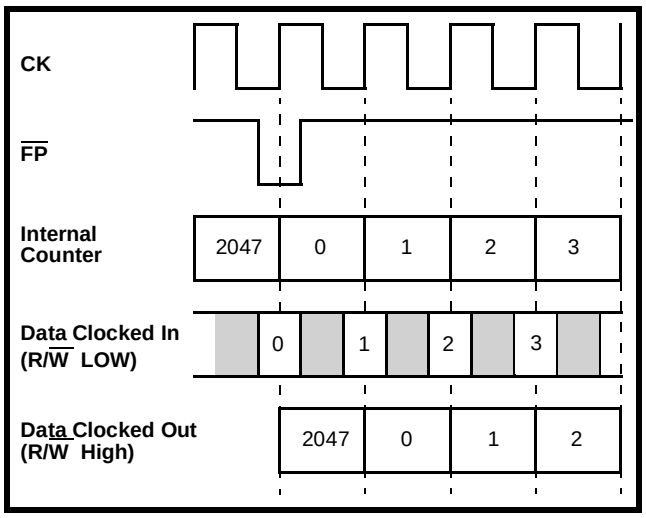


Fig. 11 - Counter Mode Functional Timing

External Mode

The external mode, which is designed for use in 2048 switching applications, permits random access to the memory both for input and output operations. The pinout for external mode is shown in Fig. 12. The address asserted on the external address bus is used to specify the memory location to be accessed for the read or write operation. The level asserted on R/$\overline{W}$ during a specific clock period determines whether the addressed memory is written to or read from. During a write operation, the output data bus is actively driven with data latched out in the previous read operation.

Data is clocked into or out of the device on the positive edges of the clock as shown in Fig. 13.

Shift Register Mode

In this mode, data clocked into the SMX is delayed by a number of clock cycles before being clocked out of the device. The delay introduced (in number of clock cycles) is equal to two times the binary value of the address latched into the device plus 2. For example, if the address asserted is Hex 02, the delay through the switch is equal to six clock cycles.

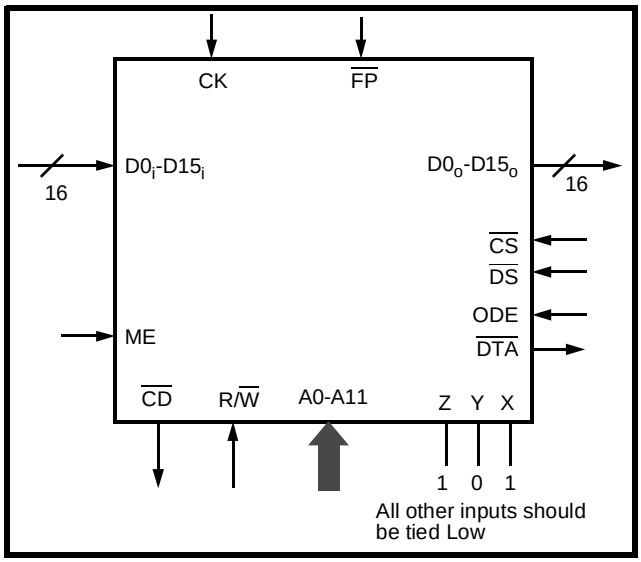


Figure 12 - External Mode Pinout

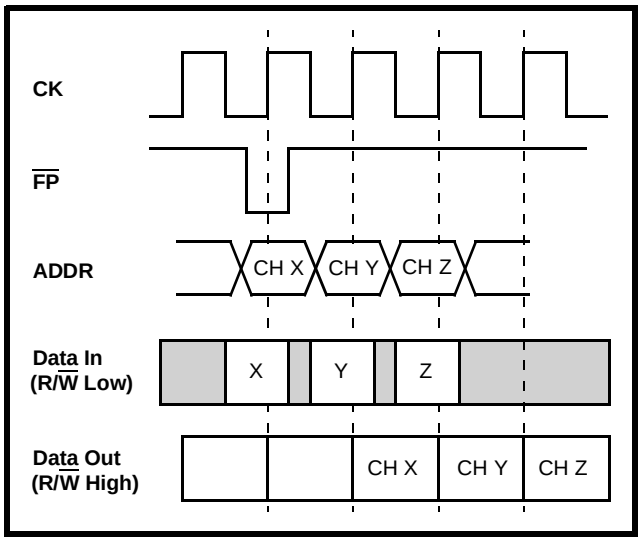


Figure 13 - External Mode Functional Timing

Maximum permissible delay is equal to 4096 clock cycles.

The pertinent timing parameters are illustrated in Fig. 14. Data is clocked in and out of the device with rising edge of the clock.

The address is latched in with the negative edge of $\overline{DS}$ while the $\overline{CS}$ is low.

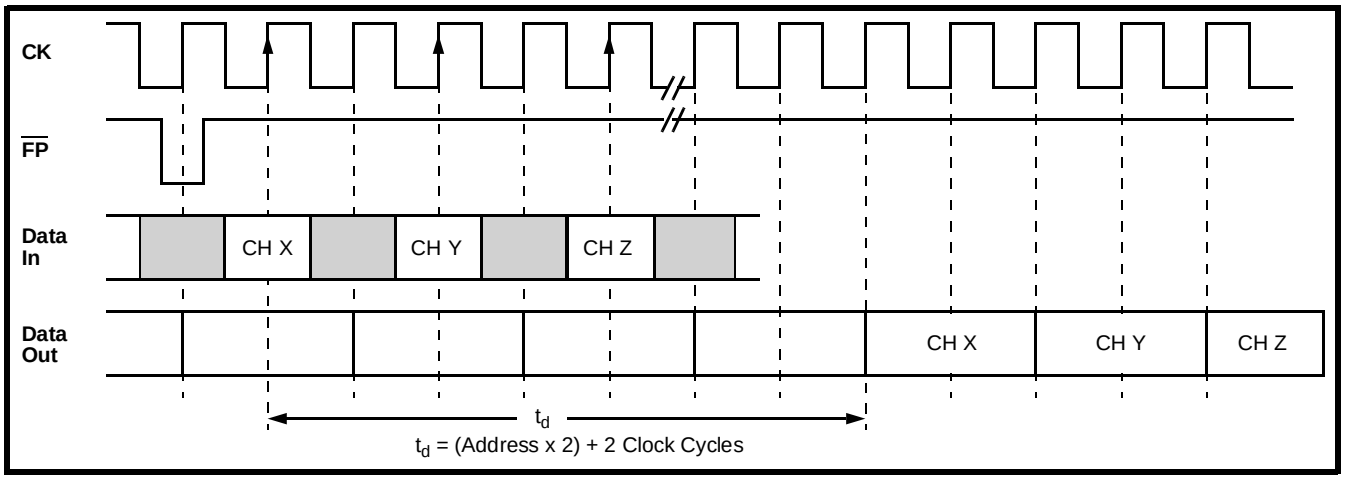


Figure 14 - Shift Register Mode Data Input/Output Timing

Applications

1024 Channel Switch Matrix

A 1024 channel, non-blocking, timeslot interchange switch can be constructed using two SMX devices (refer to Figure 15). One SMX is operated in the Data Memory mode, while the second device is operated in Connect Memory Mode-1.

Data to be switched is clocked into the data memory via the 16 bit input data bus and stored sequentially in memory locations addressed by the internal 11 bit counter. The data is read out of the Data Memory (SMX#1) according to the external address supplied by the Connection Memory (SMX#2). The Connection memory clocks out contents of the memory according to the addresses supplied by the internal counter.

The clock applied at the CK input of both the devices has a frequency of 16.384 MHz. There are two clock periods in each channel timeslot (see Figure 16). A framing signal ($\overline{FP}$) with a frequency of 8 kHz is used to delinate frames with 1024 channels each. The $\overline{FP}$ input to the Data Memory is delayed by seven clock periods from the Connection Memory frame pulse. This phase delay synchronizes the internal counters of the two SMXs such that the Connection Memory clocks out addresses one channel ahead of the affected timelsot.

Using the connections illustrated in Figure 15, the Data Memory address and control functions can be mapped onto specific bits of the Connect Memory to form a 16 bit control word, as shown in Figure 17.

The 16 bit control word is written into the Connection Memory by the processor. Subsequently, when the memory location is addressed by the internal counter, this word will be clocked out of the memory on to the data bus ($D0_o$-$D15_o$).

The output on the Connect Memory data bus ($D0_o$-$D9_o$) is used to specify the Data Memory location to be read out during any particular timeslot. The Connection Memory is programmed in a manner that permits specific addresses to be output in certain timeslots. The Data Memory will clock out data from internal memory locations according to the address asserted on its address bus. As mentioned earlier, this address is latched into Data Memory with a positive edge of the clock. The contents of the appropriate addressed memory location will be clocked out of the device at the beginning of the next channel timeslot.

Connection Memory bit 10 controls the level on the ODE input. The ODE pin is used to enable the output drivers of the Data Memory. The capability to selectively enable or disable the output drivers during specific channel timeslots is required when constructing larger switches using the 1024 channel switch as a building block.

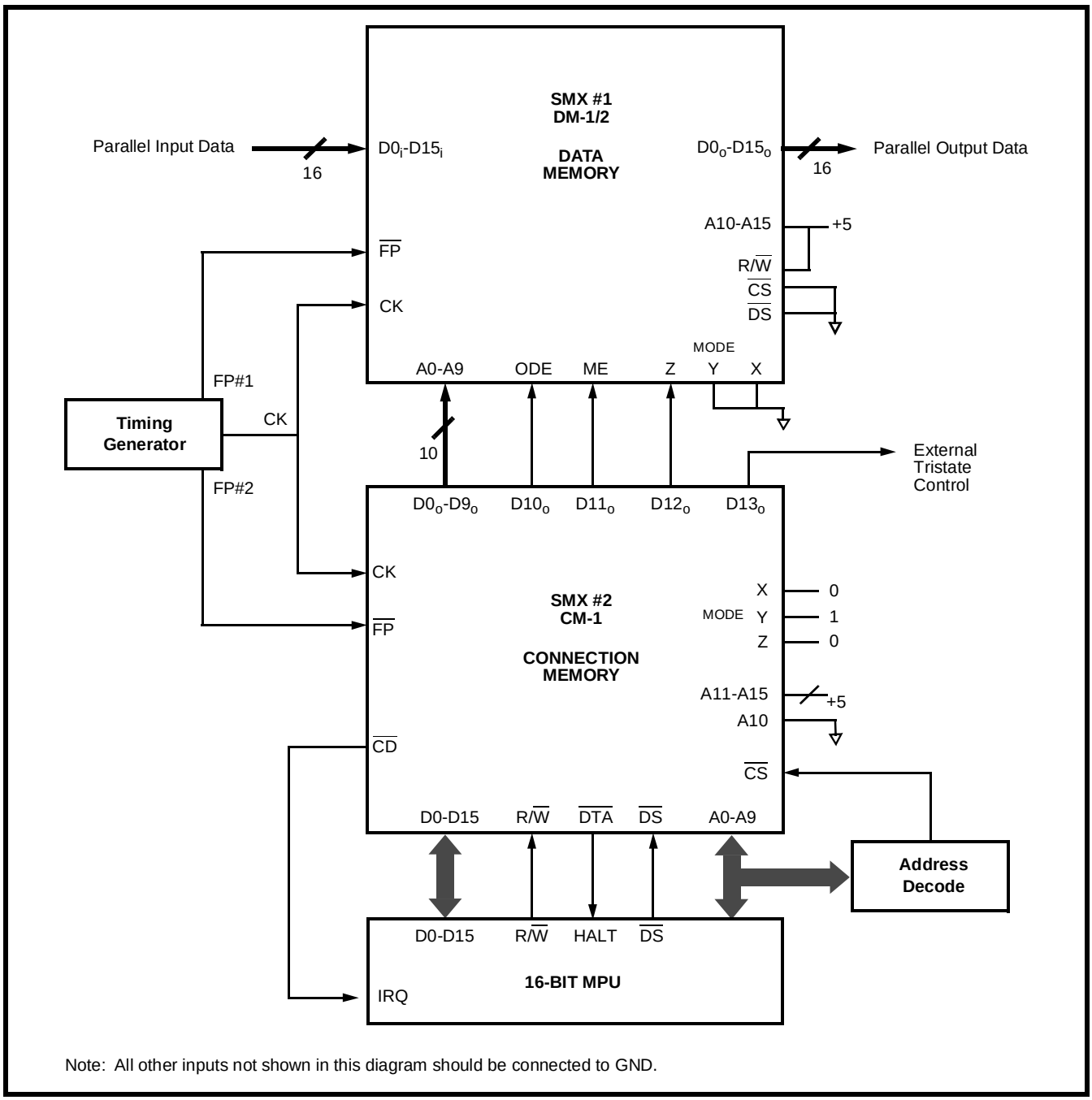
The Message Enable (ME) input of the Data Memory is controlled by D11. Setting this particular bit high will result in the data latched into the address bus being clocked out on to the Data Memory output bus. Note that only 10 of the 16 address inputs are actually connected to the data bus of the Connection Memory. Consequently, only 10 of the 16 data output bits on the Data Memory can be dynamically controlled through the Connection Memory. In other applications, all 16 of the address bits may be connected to the data output bus of the Connection Memory.

The mode of operation of the Data Memory can be changed from Data Memory Mode-1 to Data Memory Mode-2 by setting or resetting D12 in the connection

memory. The delay through the matrix can be optimized for specific applications by selectively enabling one of the two modes. Data Memory-1 (DM-1) is designed for voice switching applications where it is generally desirable to minimize delay through the switch. As mentioned earlier in the DM-1 description, the delay through the switch depends upon the difference between the input channel timeslot and the output channel timeslot. Consecutive output channels switched from non-contiguous input channels will not always originate from the same input frame. For example, if channels 3, 6 and 8 are to be switched to channels 5, 6 and 7; output channel 5 will contain data input in the current frame, while channels 6 and 7 will contain data clocked in one frame earlier. Data Memory-2 (DM-2) is designed for data switching applications where concatenation of a number of channels is often necessary. Data clocked out of the device will originate from the previous frame, regardless of the input/output time difference. There is one exception, when channel 1023 is switched to channel 0, the contents of Channel 0 will not originate from the previous frame but rather from the frame before it.

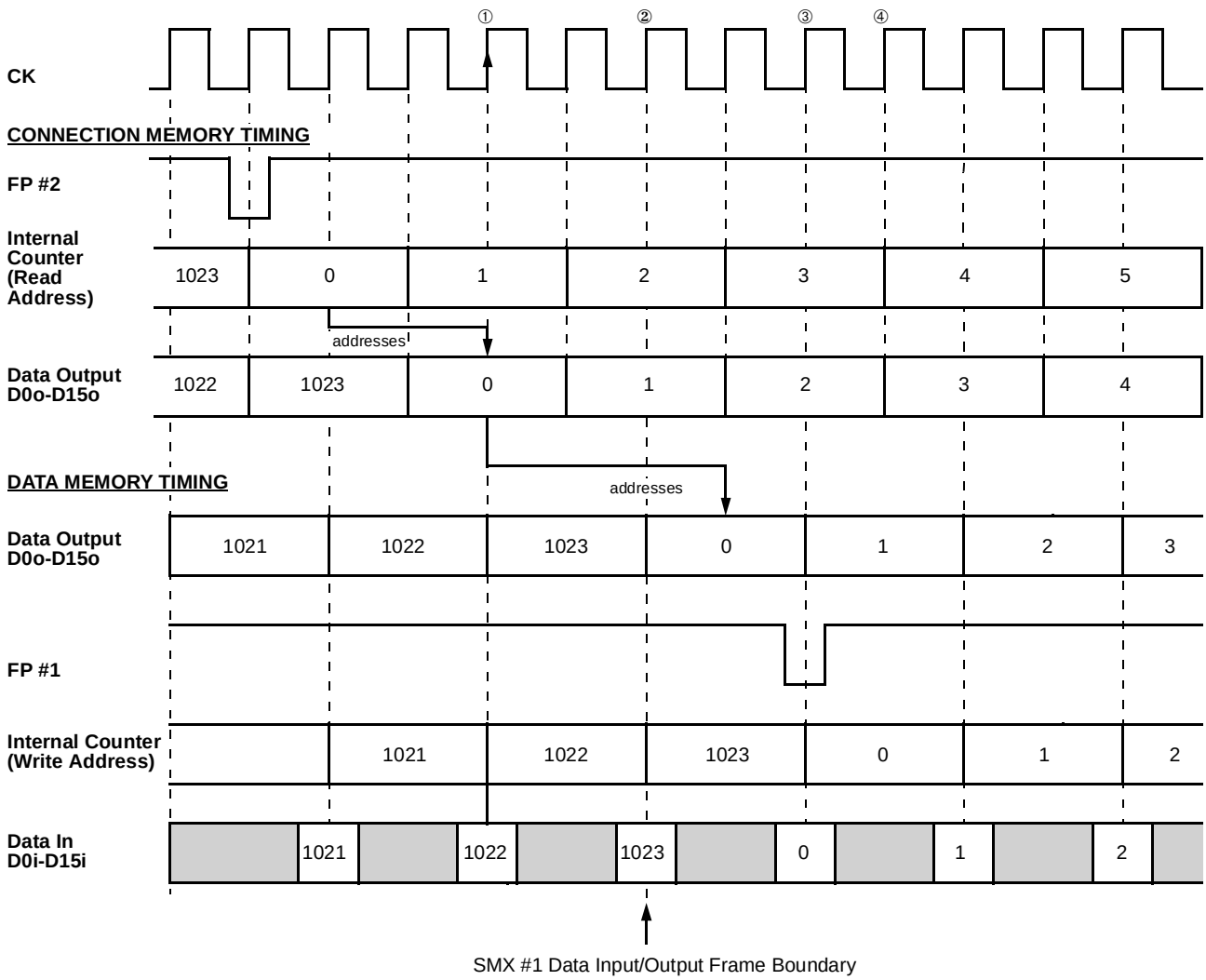
The capability to selectively change between DM-1 and DM-2 allows a single switch to handle both voice and data effectively.

External bus drivers can be controlled with D13 of the Connection Memory data bus. This bit will be output along with the remaining bits one channel



Note: All other inputs not shown in this diagram should be connected to GND.

Figure 15 - 1024 Channel Switch Matrix



Note 1: Address is latched into the Data Memory by the first positive clock edge in a timeslot (edge ① for Ch. 0). Data will be clocked out by the first positive clock edge in the next timeslot (edge ② for Ch. 0).

Note 2: Data is latched into the Data Memory by the first rising edge in a timeslot (edge ③ for Ch. 0) and is written into the memory location addressed by the internal counter with the next rising edge (edge ④ for Ch. 0).

Figure 16 - 1024 Channel Switch Timing

ahead of time; i.e., one channel before the addressed data is clocked out of the Data Memory. It may be necessary to provide an external bus enable one channel ahead of time in applications where precharging of the external data bus is required. In other applications where no precharge is required, control bit from the next channel may be used in order to ensure that the external bus is enabled at the same time as the channel is being clocked out of the device.

The Change Detect ($\overline{CD}$) output of the Connection Memory is used to interrupt the MPU. As mentioned in the Pin and Functional descriptions, $\overline{CD}$ goes low when the internal CRC performed by the device indicates a change in memory contents. This feature is particularly useful in switching applications where the Connection Memory is configured once and is not modified for long periods of time, e.g., in network digital access crossconnect systems. Any inadvertent corruption of the memory contents will cause $\overline{CD}$ to interrupt the processor.

D15 - D14 Unused	**D13** External Driver Enable	**D12** DM-1 or DM-2 Select	**D11** Message Enable	**D10** ODE Control	**D9 - D0** Source Channel Address

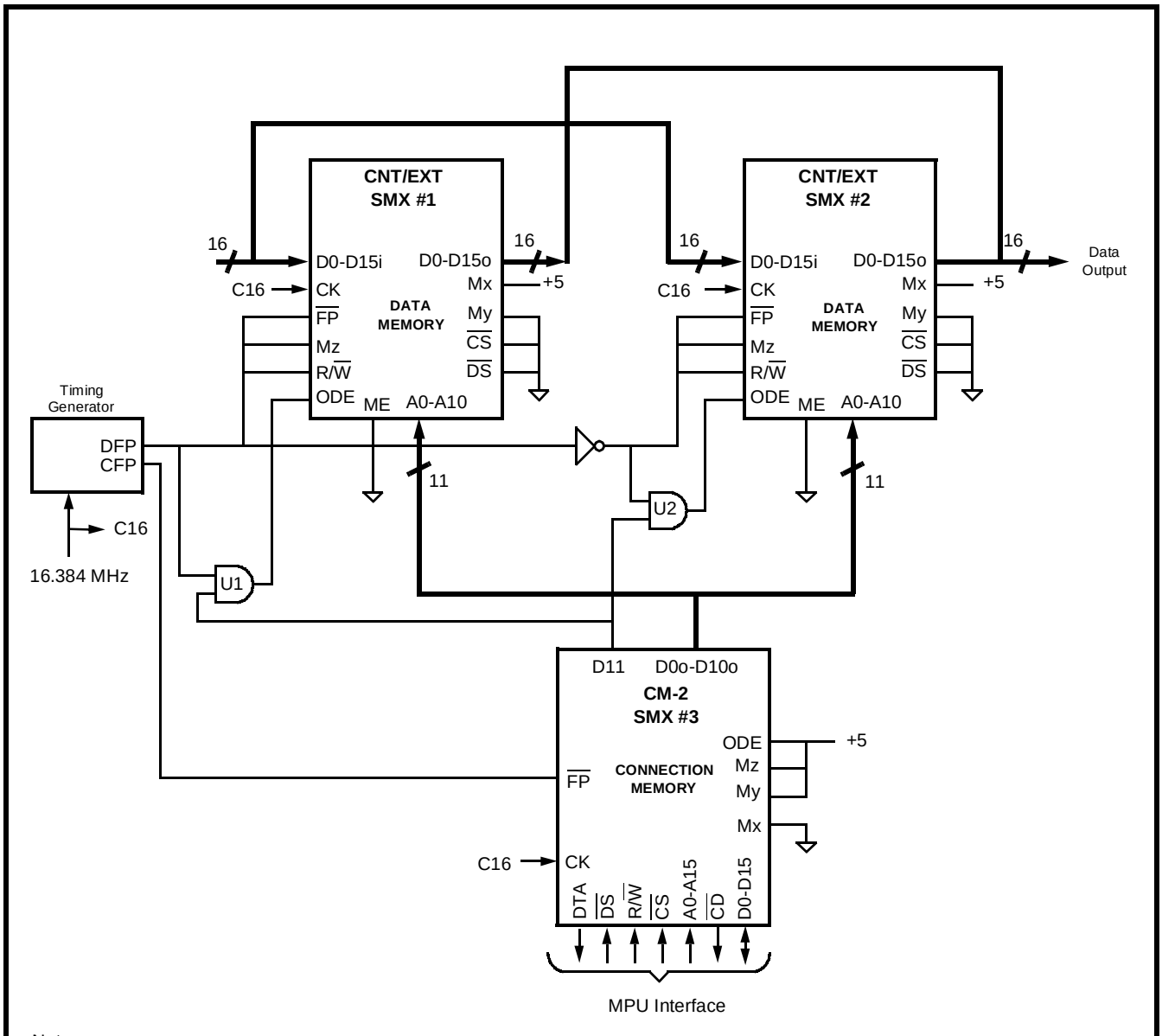
Figure 17 - Mapping of Address and Control Signals onto Connect Memory Data Bits

Switching any input channel to an output channel timeslot is possible by merely writing the address of the input channel in the Connection Memory location corresponding to the output channel timeslot. For example, to switch channel 1 to output channel 5 and enable output drivers during channel 5, the Connection Memory location corresponding to channel 5 should be loaded with Hex 2001. This word will be clocked out of the Connection Memory during timeslot 4 and will cause the Data Memory to clock out contents of the memory corresponding to channel 1 during the channel 5 timeslot. The 16 bit word clocked out by the Connection Memory will also enable Data Memory output drivers, and, external drivers.

2048 Channel Switch Matrix

A 2048 channel, double buffered timeslot interchange switch can be constructed with three SMXs as shown in Figure 18. SMX#1 and SMX#2 are used to store data and switch it in time, while the third SMX functions as a Connection Memory.

SMX#1 and 2 are operated in the Counter Mode and External Mode alternatively in consecutive frames. In any specific frame, one of the two is in Counter mode while the other is in External mode. The functions are reversed in the successive frame. The SMX in counter mode is programmed to write data



Notes:
1) U1 and U2 are required if the data output bus is to be enabled/disabled via the microprocessor interface.
2) All inputs not shown should be connected to Ground (V_{SS}).

Figure 18 - 2048 Channel Timeslot Interchange Circuit

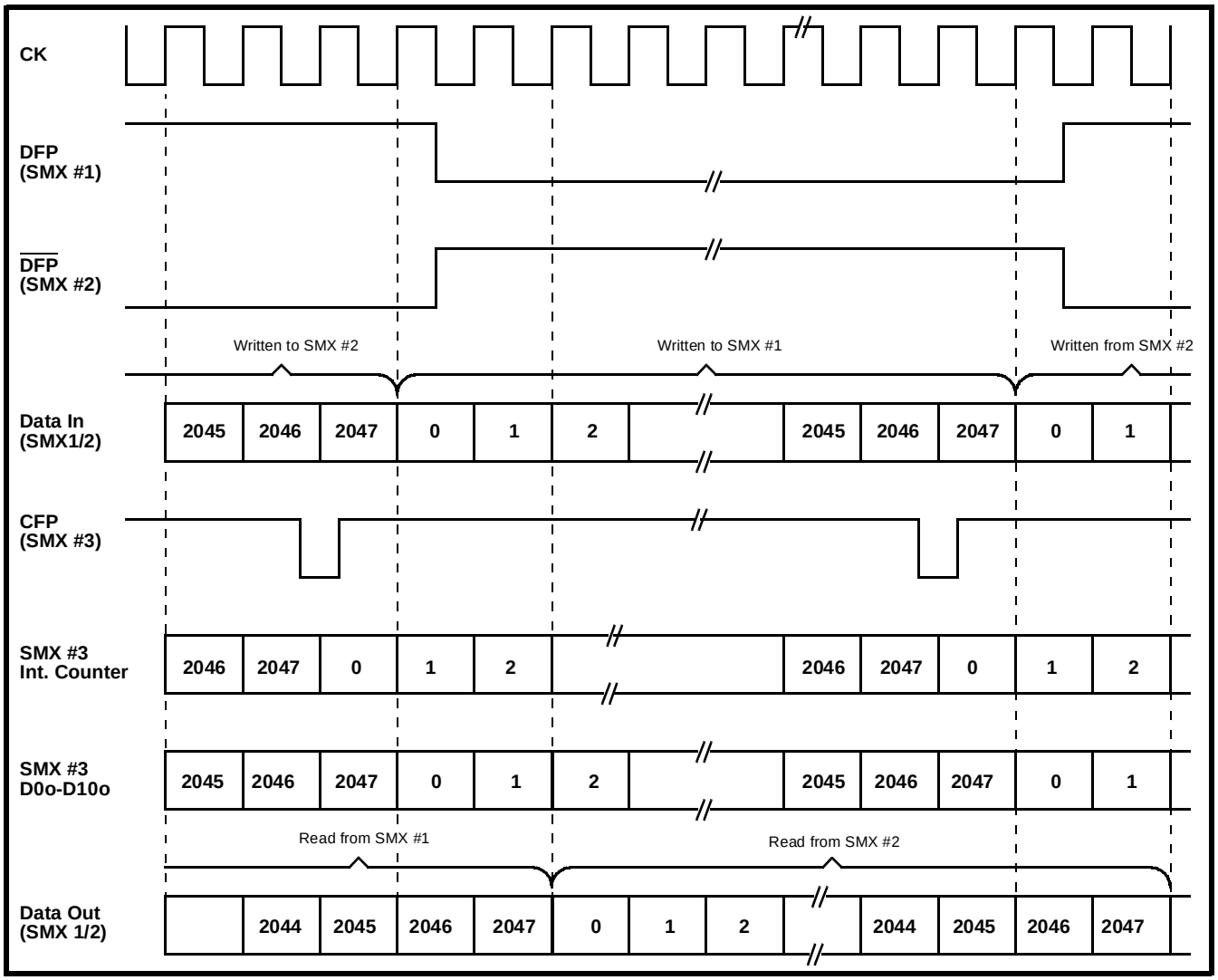


Figure 19 - 2048 Channel Switch Timing

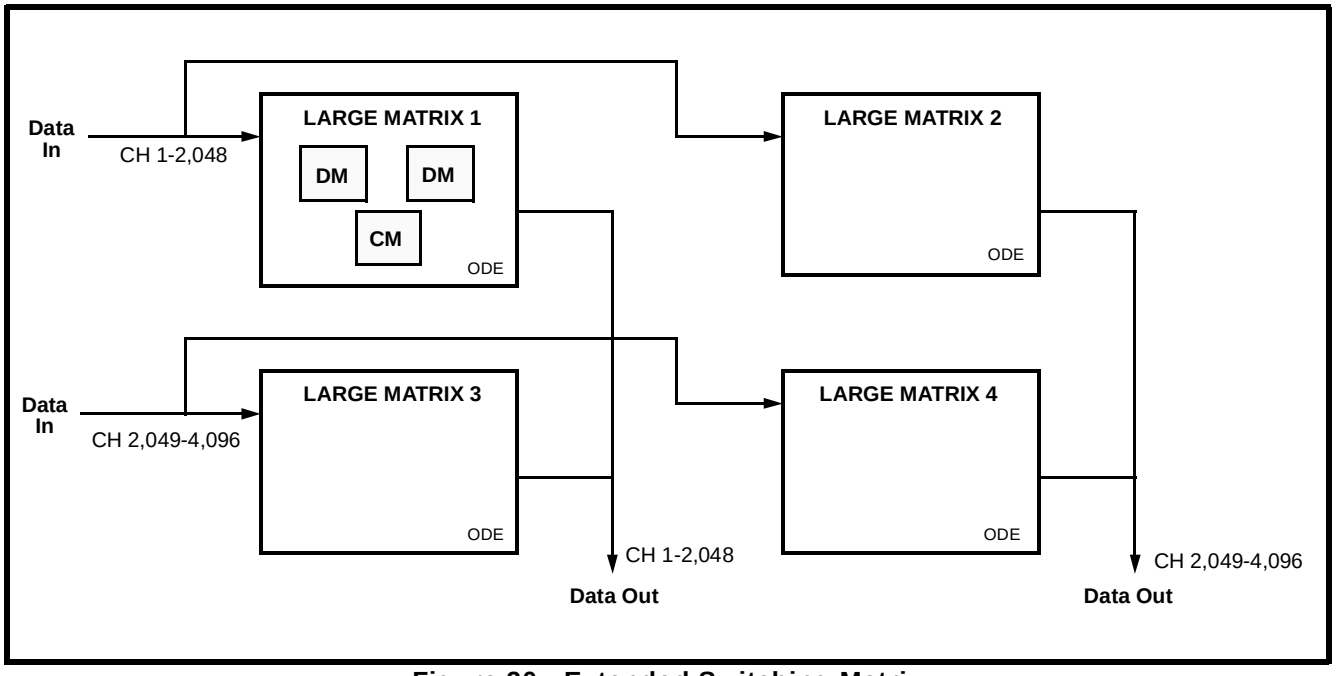


Figure 20 - Extended Switching Matrix

into its memories addressed by the internal counter. The SMX in the external mode reads data out from memory locations addressed by the Connection memory. In this manner, incoming data is continually written into one memory block while it is being read out of the other block. The device in counter mode has its output drivers disabled.

This configuration results in a maximum throughput delay of two frames. Data clocked into the device in the current frame is clocked out in the next frame. The appropriate timing parameters are illustrated in Figure 19. The clock signal applied to all three SMXs has the same frequency.

SMX#3 is operated in Connect Memory Mode-2. In this mode, data is clocked out of the device at the same rate as the clock, i.e., at 16.384 Mbps.

Extended Switching Matrix

Larger extended switch matrices can be created using the 1024/2048 channel switch as a building block. As shown in Figure 20, a 4096 channel matrix would require four smaller 2048 channel building blocks.

Construction of matrices larger than 4K may require external drivers to accommodate the greater capacitive loading on the outputs.

Using the SMX for Messaging

In some system architectures the PCM voice signals and system status information is transmitted and received over a common backplane. To facilitate microprocessor access to the backplane, the SMX can be used to read incoming data or write to a channel on the output data bus.

Data clocked into the SMX can be read from the device by a microprocessor interfaced to the output data bus and the address bus (see Figure 21). Data can be written to a specific timeslot on the output data bus directly by the microprocessor using the messaging feature (enabled by tying the ME pin high) .

A 1024 Switch Matrix with messaging capability can be constructed with three SMXs as shown in Figure 22. The first SMX is used for performing the actual switching function. The second SMX is configured as the connection memory. As discussed in the 1024 switch application, by enabling the messaging feature, data clocked out of the connection memory and latched into the data memory address bus will be clocked out on to the data bus directly. Incoming data is read by the microprocessor using the third

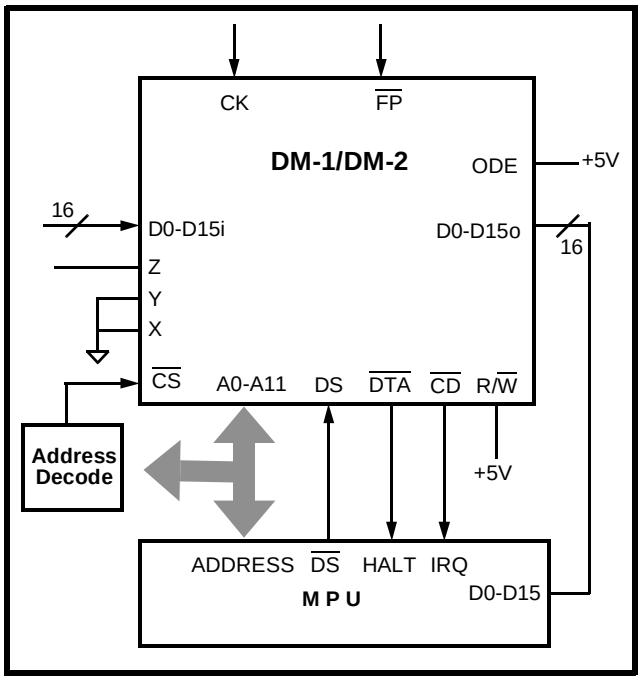


Figure 21 - Reading the Data Memory with a Microprocessor

SMX. The data output bus of the third SMX is connected to the data bus of the MPU.

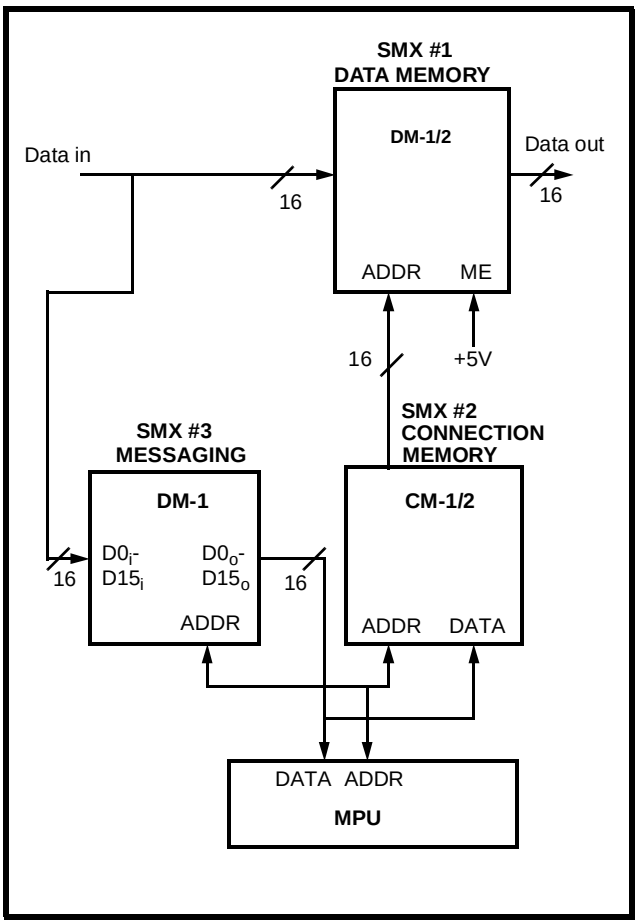


Figure 22 - A 1024 Channel Switch Matrix with Message Capability

Parallel-to-Serial Conversion

The SMX can be used in systems which employ serial architectures by converting the parallel I/O into a serial format. The Mitel MT9085 Parallel Access Circuit (PAC) is designed to interface to the parallel busses of the SMX. A single PAC can convert the output of a1024 channel switch into 2.048 Mbit/s or 4.096 Mbit/s serial format. A second PAC can be configured to implement serial to parallel conversion (see Figure 23).

The PAC generates all framing signals required to implement a 1024 or 2048 channel matrix. Refer to the MT9085 data sheet for more information on operation of the PAC.

For more information, see Mitel's Application Note MSAN-135 *"Design of Large Digital Switching Matrices using the SMX/PAC"*.

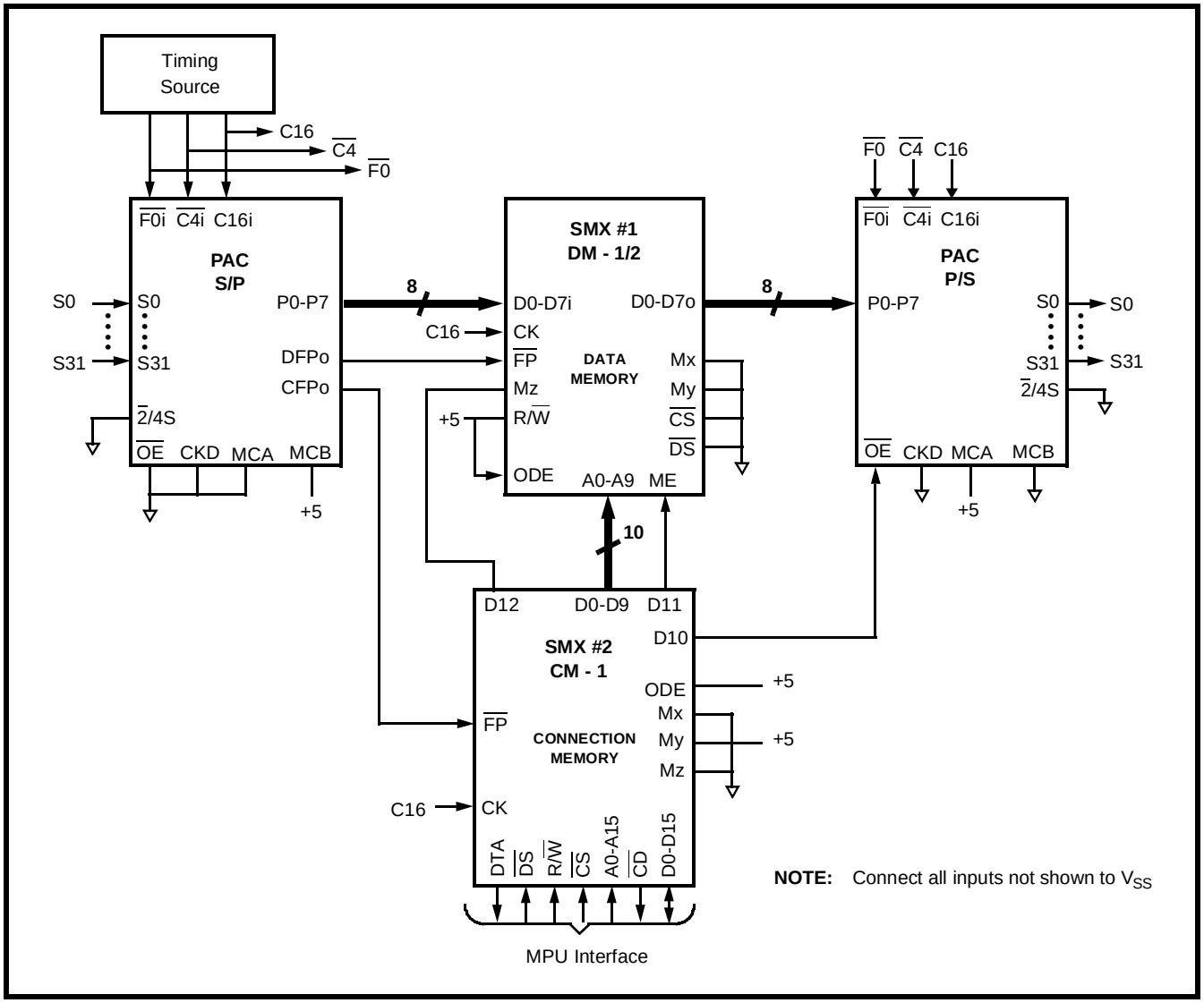


Figure 23 - 1024 Channel Serial Switch Matrix Using the PAC and SMX

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage V_{DD}-V_{SS}	V_{DD}	-0.3	7	V
2	All Input Voltages	V_i	V_{SS}-0.3	V_{DD} +0.3	V
3	All Output Voltages	V_o	V_{SS}-0.3	V_{DD} +0.3	V
4	Storage Temperature Range	T_S	-40	125	°C
5	Current at Digital Outputs	I_O		150	mA
6	Continuous Power Dissipation	P_D		2	W

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to Ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Supply Voltage	V_{DD}	4.75	5.0	5.75	V	
2	Operating Temperature	T_{OP}	-40		70	°C	
3	Input High Voltage	V_{IH}	$0.7V_{DD}$			V	
4	Input low Voltage	V_{IL}	0		$0.3V_{DD}$	V	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - Voltages are with respect to Ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Supply Current	I_{DD}		120	200	mA	Outputs unloaded
2	Input High Voltage	V_{IH}	$0.7V_{DD}$			V	
3	Input Low Voltage	V_{IL}	0		$0.3V_{DD}$	V	
4	Input Leakage Current	I_{IL}			±10	µA	
5	Output High Current (all outputs except D0i-D15i)	I_{OH}	8			mA	V_{OH}=0.7 V_{DD}
6	Output Low Current (all outputs except $\overline{DTA}$, $\overline{CD}$ and D0i-D15i)	I_{OL}	8			mA	V_{OL}=0.3 V_{DD}
7	Output High Current D0i-D15i	I_{OH}	2			mA	V_{OH}=0.7 V_{DD}
8	Output Low Current $\overline{DTA}$ & $\overline{CD}$	I_{OL}	2			mA	V_{OL}=0.3 V_{DD}
9	Input Capacitance	C_i			10	pF	
10	Output Pin Capacitance	C_o		10		pF	V_{DD}=5.0V±10%.
11	High Impedance Leakage	I_{OZ}			10	µA	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - Output Drive Enable Timing (see Fig. 24) - Voltages are with respect to Ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	ODE Setup	t_{OS}	0			ns	
2	ODE Hold	t_{OH}	20			ns	
3	Data Output High Z to Active	t_{DZA}			35	ns	C_L=30pF
4	Data Output Active to High Z	t_{DAZ}			30	ns	

† Timing is over recommended temperature and power supply voltages.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

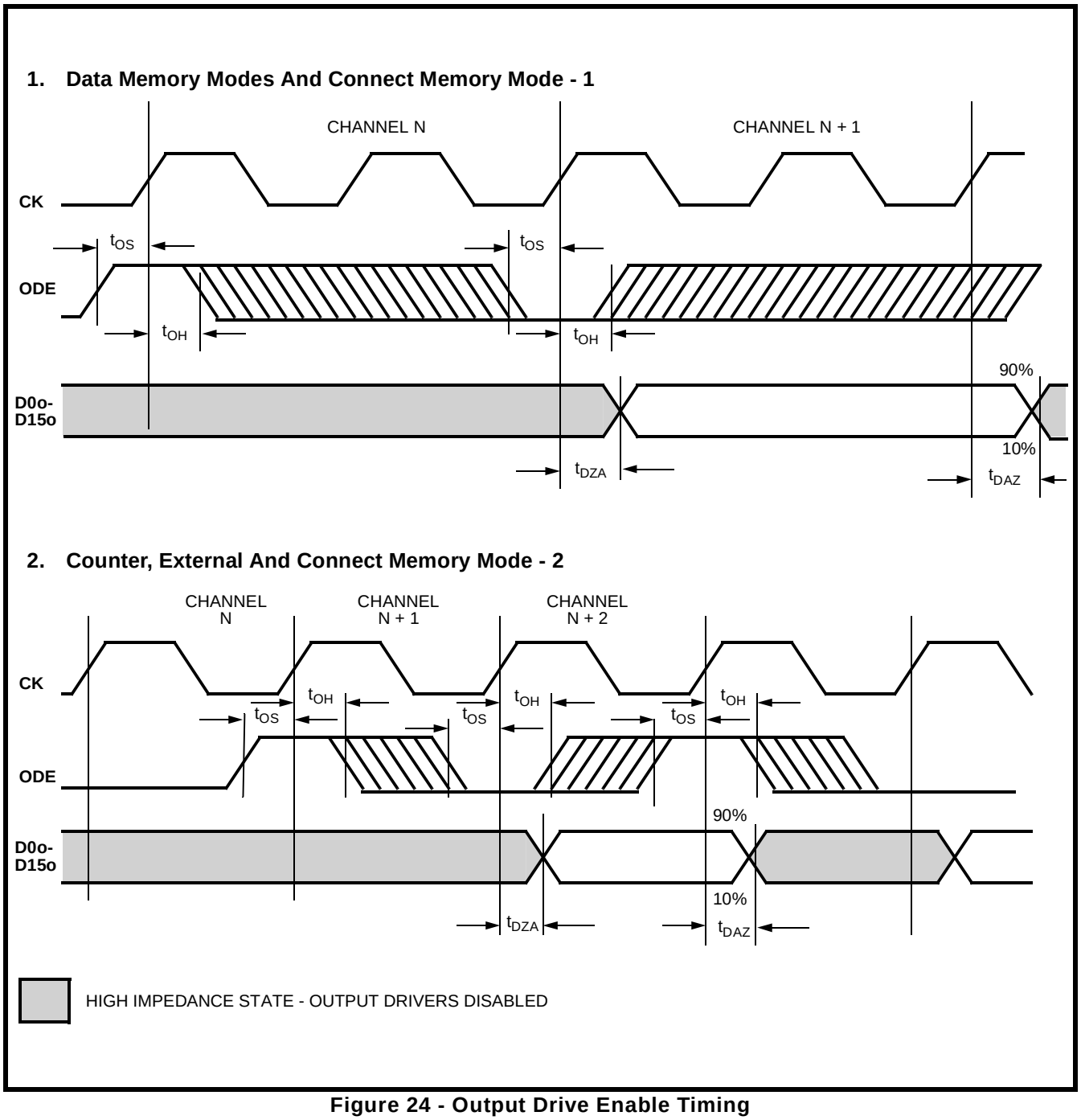


Figure 24 - Output Drive Enable Timing

AC Electrical Characteristics† - Data Memory, Connect Memory-1 and Shift Register Mode Timing (See Fig. 25) - Voltages are with respect to Ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Address Setup	t_{AS}	0			ns	
2	Address Hold	t_{AH}	18			ns	
3	Data Output Delay	t_{DD}		9	34	ns	C_L = 30 pF
4	Data Input Setup	t_{DS}	0			ns	
5	Data Input Hold	t_{DH}	4			ns	
6	ME, Mx, My, Mz Setup	t_{MES}	0			ns	
7	ME, Mx, My, Mz Hold	t_{MEH}	26			ns	
8	CK Clock Period	t_{PCK}	60			ns	

† Timing is over recommended temperature and power supply voltages.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

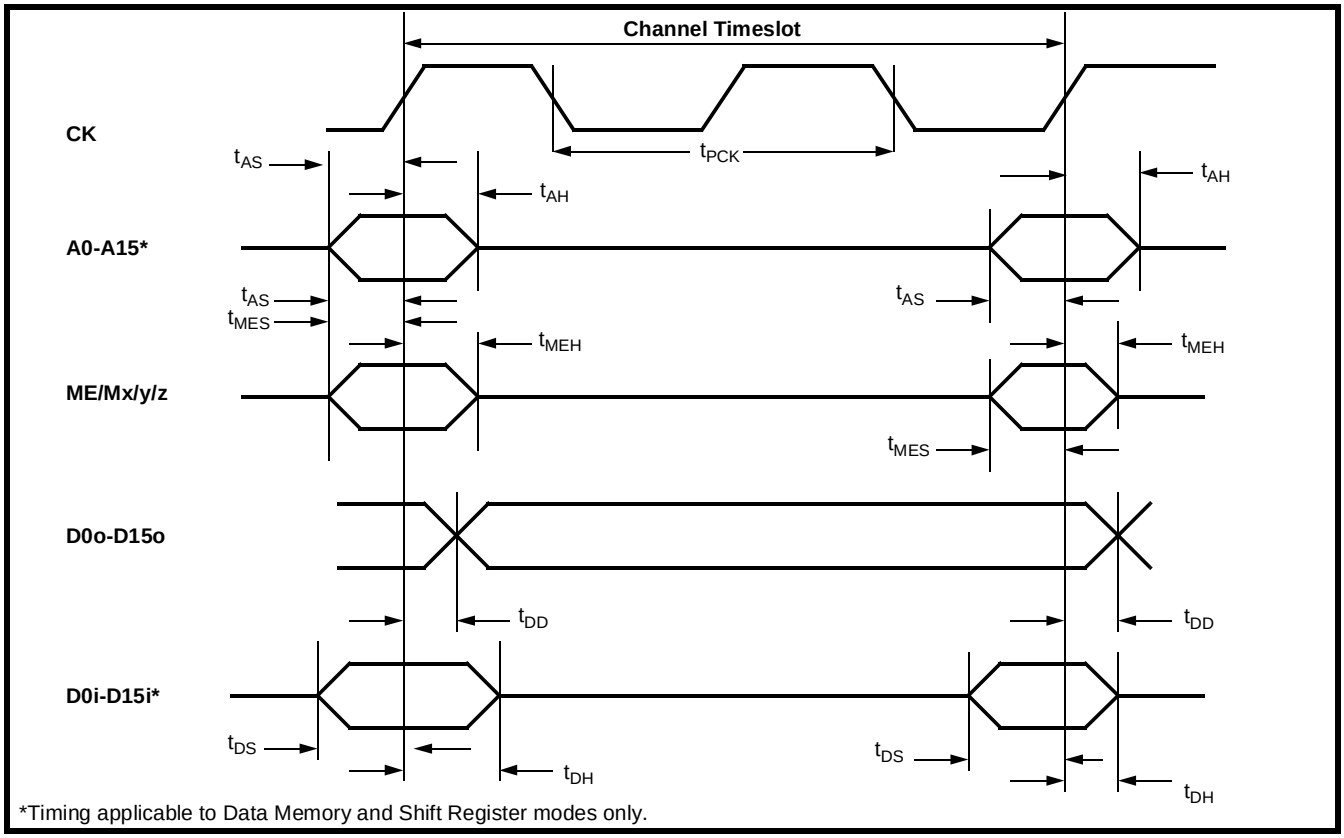


Figure 25 - Data Memory, Connect Memory-1 and Shift Register Mode Timing

AC Electrical Characteristics† - External, Connect Memory-2 and Counter Mode Timing (See Fig. 26) - Voltages are with respect to Ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	ADDR, R/$\overline{W}$ Hold Time	t_{WEH}	10			ns	
2	ADDR,R/$\overline{W}$ Setup Time	t_{WES}	2			ns	
3	Data Setup	t_{DS}	0			ns	
4	Data Hold	t_{DH}	4			ns	
5	Data Output Delay	t_{DD}		9	34	ns	C_L = 30 pF
6	ME, Mx, My, Mz Setup	t_{MES}	0			ns	
7	ME, Mx, My, Mz Hold	t_{MEH}	26			ns	

† Timing is over recommended temperature and power supply voltages.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

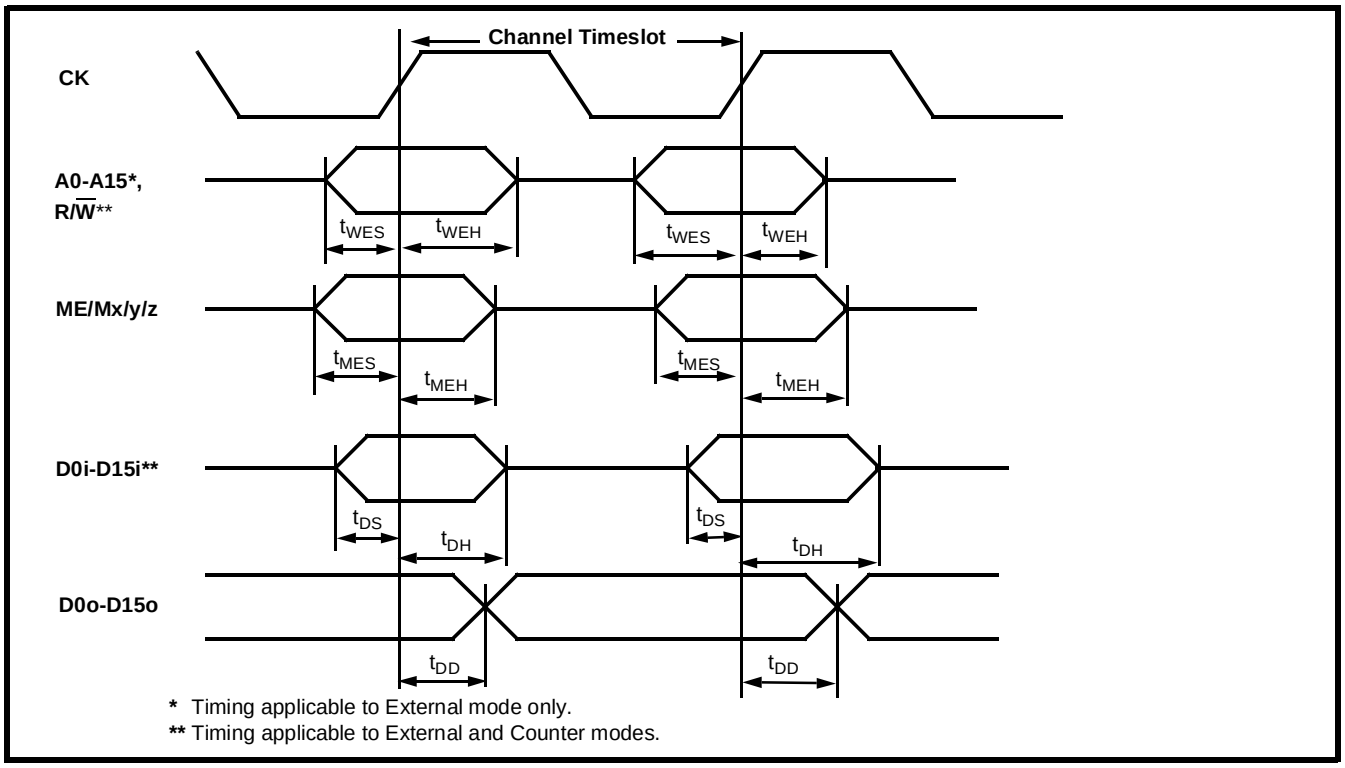


Figure 26 - External, Connect Memory-2 and Counter Mode Timing

AC Electrical Characteristics† - Address Bus Timing In Shift Register Mode (See Fig. 27) -

Voltages are with respect to Ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Address Setup	t_{AS}	0			ns	
2	Address Hold	t_{AH}	12			ns	
3	Chip Select Setup	t_{CSS}	0			ns	
4	Chip Select Hold	t_{CSH}	0			ns	

† Timing is over recommended temperature and power supply voltages.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

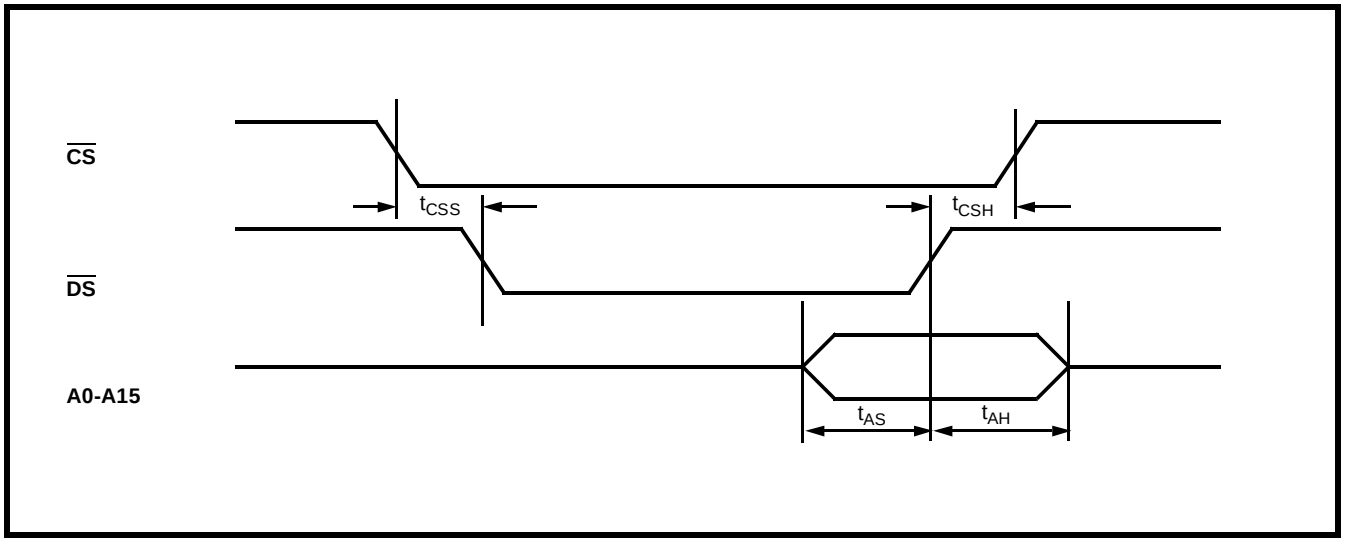
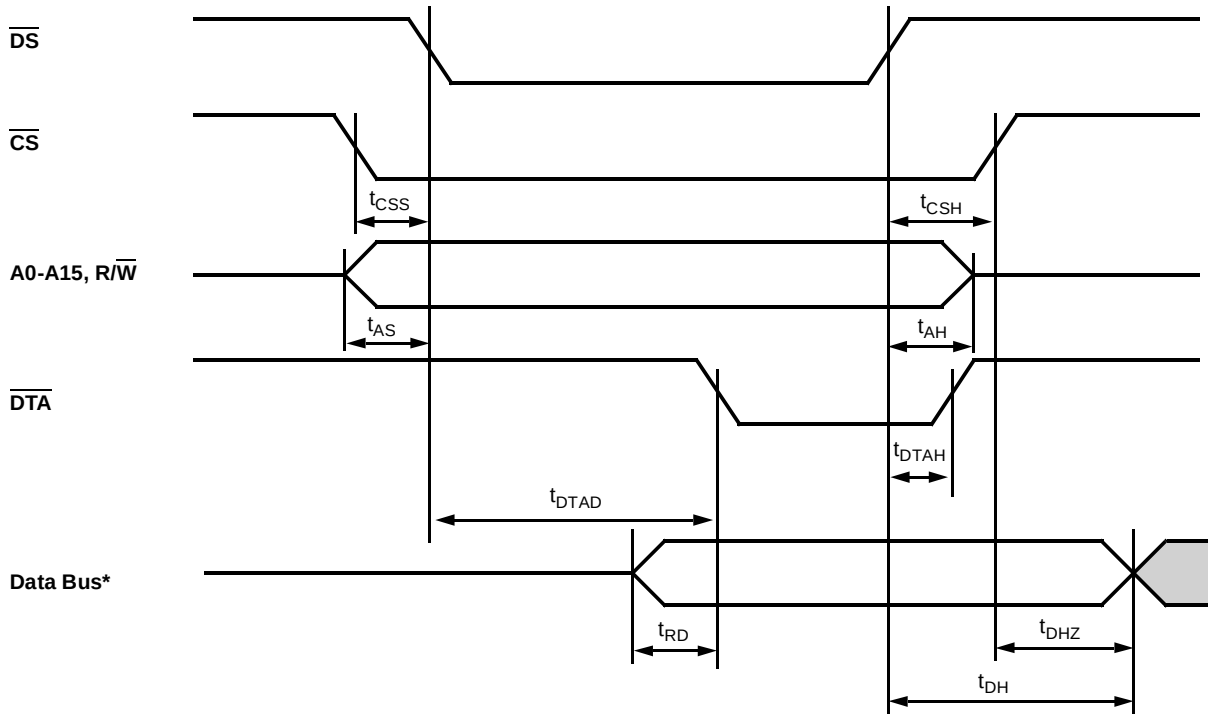


Figure 27 - Address Bus Timing in Shift Register Mode

AC Electrical Characteristics† - Microprocessor Read Timing for Connect Memory, Data Memory & External Modes (See Fig. 28) - Voltages are with respect to Ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Chip Select Setup	t_{CSS}	0			ns	
2	Chip Select Hold	t_{CSH}	0			ns	
3	ADDR, R/$\overline{W}$ Setup	t_{AS}	0			ns	
4	ADDR, R/$\overline{W}$ Hold	t_{AH}	0			ns	
5	$\overline{DTA}$ Delay	t_{DTAD}	4.5		9	T_{CK}*	
6	$\overline{DTA}$ Hold	t_{DTAH}	0			ns	
7	Valid Data Out to DTA Low	t_{RD}	3			T_{CK}*	
8	$\overline{DS}$ High to Data Invalid	t_{DH}	0		27	ns	
9	Output Data Active to High Z	t_{DHZ}			31	ns	

* T_{CK}= Clock (CK) Period
† Timing is over recommended temperature and power supply voltages.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.



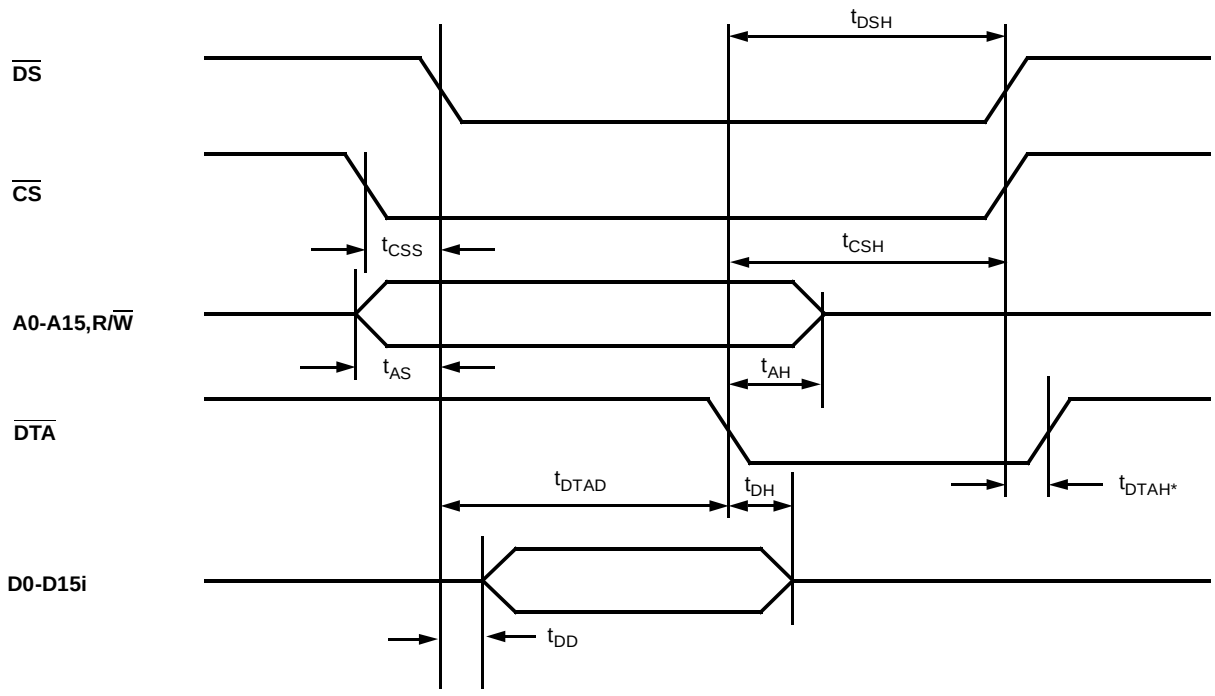
* In Data Memory Mode and External Mode, data is clocked out on D0o-D15o; in Connect Memory Mode data is clocked out on D0i-D15i (bidirectional).

Figure 28 - Microprocessor Read Timing for Connect Memory Mode, Data Memory Mode and External Mode

AC Electrical Characteristics† - Microprocessor Write Timing for Connect Memory Mode (See Fig. 29) - Voltages are with respect to Ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Chip Select Setup	t_{CSS}	0			ns	
2	Chip Select Hold	t_{CSH}	0			ns	
3	ADDR, R/$\overline{W}$ Setup	t_{AS}	0			ns	
4	ADDR, R/$\overline{W}$ Hold	t_{AH}	0			ns	
5	$\overline{DTA}$ Delay	t_{DTAD}	4.5		7.5	T_{CK}*	
6	$\overline{DTA}$ Hold	t_{DTAH}	0			ns	
7	$\overline{DS}$ Low to Data in Delay	t_{DD}			4.5	T_{CK}*	
8	$\overline{DTA}$ Low to Data in Hold	t_{DH}	0			ns	
9	$\overline{DS}$ Hold Time	t_{DSH}	0			ns	

* T_{CK}= Clock (CK) Period
† Timing is over recommended temperature and power supply voltages.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.



* This parameter is specified with respect to the rising edge of $\overline{DS}$ or $\overline{CS}$ depending on which signal goes high first.

Figure 29 - Microprocessor Write Timing for Connect Memory Mode

AC Electrical Characteristics† - Frame Pulse, Clock and Change Detect Timing (See Fig. 30) - Voltages are with respect to Ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Frame Pulse Setup	t_{FPS}	6			ns	
2	Frame Pulse Hold	t_{FPH}	3			ns	
3	Change Detect Delay	t_{CDD}			38	ns	
4	Change Detect Reset Delay	t_{CDRD}	0		13	ns	

† Timing is over recommended temperature and power supply voltages.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

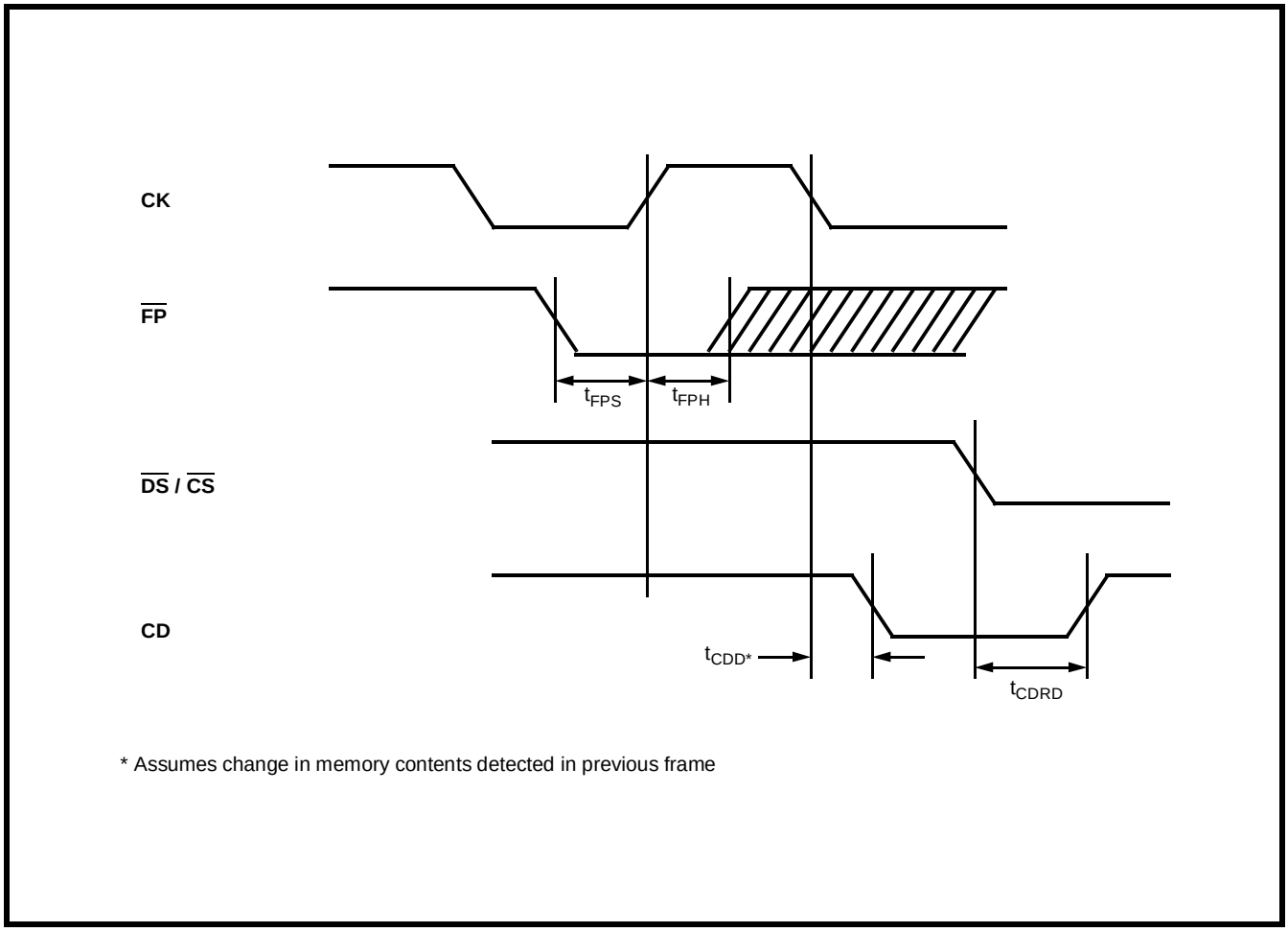


Figure 30 - Frame Pulse and Change Detect Timing

NOTES: