MINDSPEED™
A CONEXANT BUSINESS

Traffic Stream™ Processor

MXT4400

Complete Programmable Traffic Management and Internetworking Solution

The MXT4400 Traffic Stream Processor (TSP) platform is the industry's first programmable traffic management and internetworking engine to offer wire-speed performance for gigabit-scale cell and packet network equipment. This innovative integrated circuit adapts the protocol and traffic flow of up to 64K input traffic streams to managed traffic streams in an output data path. Defining traffic streams as cells or packets enables the MXT4400 to excel in a wide range of ATM and Packet-over-SONET applications. The MXT4400 is the first member of the TSP product family, which will span the performance spectrum from OC-3 to OC-48.

To shorten time to market, Mindspeed Technologies™ offers off-the-shelf PortMaker software for the MXT4400. PortMaker is a family of complete applications for AAL5 SARing (PortMaker-SAR) and ATM traffic shaping, policing and OAM cell processing (PortMaker-Cell Traffic Manager). The source code for these applications can also be licensed to customers who want to develop value-added features or additional services.

Mindspeed Technologies also supplies extensive system-development tools with both the binary and source-code versions of PortMaker. TSP Board Development Kit provides a chip model, test bench and diagnostic code for hardware design verifications. The TSP Design Toolkit is a powerful development environment for customers modifying PortMaker source code or developing custom applications.

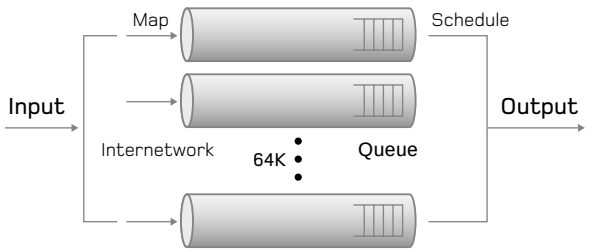
KEY FEATURES

- Programmable QoS and internetworking
- Wire-speed performance/ firmware flexibility
- Supports up to 64K traffic streams
- Standard interfaces with complete tools suite
- Integrated memory subsystems and buffer management
- Scales to OC-12
- Complete off-the-shelf software applications are available

Traffic Stream Processing Services

Traffic Stream Processors act as intelligent agents in a network data path. They discriminate between packet or cell traffic streams within highly channelized data paths by mapping them to software processes. These processes service each traffic stream with internetworking algorithms designated for that channel. The Octave™ processor's proximity to the flow of data gives it an unmatched ability to examine and manipulate network headers. The TSP's hardware engines accelerate more laborious tasks, such as ensuring data integrity.

Many services require queuing for elastic data storage. TSPs integrate this critical function. Per-stream queues draw upon autonomously-managed TSP buffer resources. Service-specific software algorithms inject feedback into traffic streams to avoid congestion and reserve resources to protect loss-sensitive streams from buffer starvation. The MXT4400 supports up to 64K queues. TSPs also allot output-port bandwidth among many traffic streams and enforce service-level agreements on a per-stream basis. Traffic-shaping and queue-scheduling functions apportion each traffic stream its fair share of the output port within a bandwidth floor and ceiling. Streams may be grouped in arbitrary hierarchies to control their aggregate output. Policing functions control input streams by limiting their bandwidth consumption — a vital function in service-provider networks.



Statistics-gathering functions monitor service-fulfillment goals for billing, network management and fault isolation. Alarms elevate unexpected conditions to management software as asynchronous indications of trouble.

Flexible Communications Processing Power

The Octave processor is a RISC processor, optimized to meet the demands of traffic stream processing.

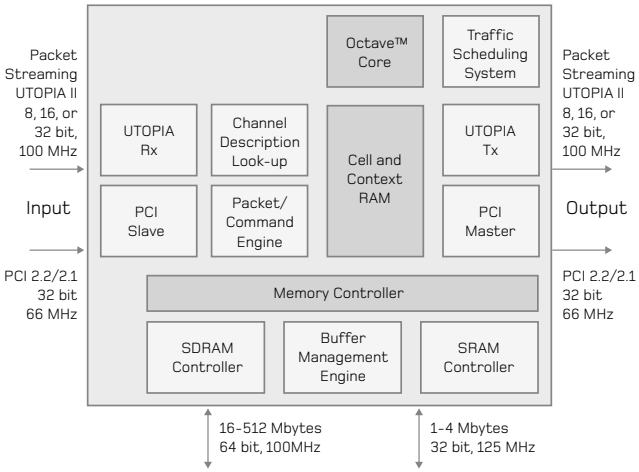
The MXT4400 minimizes context-switching overhead by erforming switching as a background process. This preserves processor cycles for system control and internetworking functions.

Tightly coupled to surrounding hardware and the data path through its register and instruction sets, the Octave processor efficiently dispatches parallel hardware operations while performing traffic-stream processing functions. The Octave processor extends the familiar RISC instruction set (ALU, Branch, Load/Store) with specialized instructions for internetworking and traffic management. Enhancing a traditional instruction set shortens the learning curve of TSP programmers and allows Mindspeed Technologies to leverage standard code-generation tools.

Hardware–Accelerated Architecture

Multiple hardware machines are integrated on-chip with the Octave processor to achieve optical wire-speed erformance. The input data path streams into the MXT4400 through its UTOPIA receiver port or FIFO ports within its PCI address space. The Channel Descriptor Look-Up engine and the Packet/Command Engine map each traffic stream to an Octave software process by examining header fields and converting the traffic stream into an internal cell format.

All traffic streams flow through the Cell and Context RAM. The Octave processor has very low-latency access to this memory and it is here that inter networking functions inspect and modify the traffic stream. Per-stream context, or state, also resides in this memory as the stream is processed.



If the application requires queuing, the Octave processor uses the buffer-management engine to manage memory allocation. The TSP supports two memory interfaces: one for low-cost synchronous DRAM and the other for low-latency synchronous SRAM. Four independent DMA engines work concurrently to sustain high throughput of stream data and context through an internal high-speed crossbar memory controller. The TSP feeds each output port with a prioritized, wire-speed stream of data.
The MXT4400's Traffic Scheduling System makes bandwidth reservations and resolves scheduling conflicts based on per-stream as well as network path and tunnel parameters.

Off-the-Shelf Software Applications

PortMaker is a family of software applications for the TSP product family. Mindspeed Technologies speeds time to market by providing off-the-shelf services such as ATM AAL5 SARing and ATM traffic shaping, policing and OAM cell processing. PortMaker product briefs provide additional details about these services.

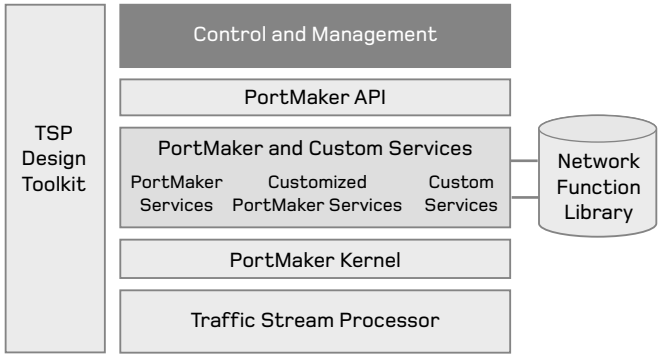
TSP Board Development Kit (BDK)

The TSP BDK is a tool available to customers who use an off-the-shelf PortMaker application. It includes tools needed for system simulation, board development and host code development. The TSP BDK provides a complete reference design for system simulation. This includes a Verilog netlist with instantiations of the TSP along with the instantiations of the required peripheral device models. This reference board-level simulation can be modified to reflect the actual TSP board used in the customer design. A test bench, with example test cases, is provided to simulate the virtual TSP board. The SWIFT encrypted simulation model for the TSP has bus loggers attached to it. Log files can be viewed with the graphical post processor, GSIM.

Customizable Software Applications

In addition to production-ready binary code, Mindspeed Technologies also licenses PortMaker applications in source-code format for the development of value-added services.

Modifications and extensions to existing PortMaker applications are facilitated by PortMaker's modular architecture.



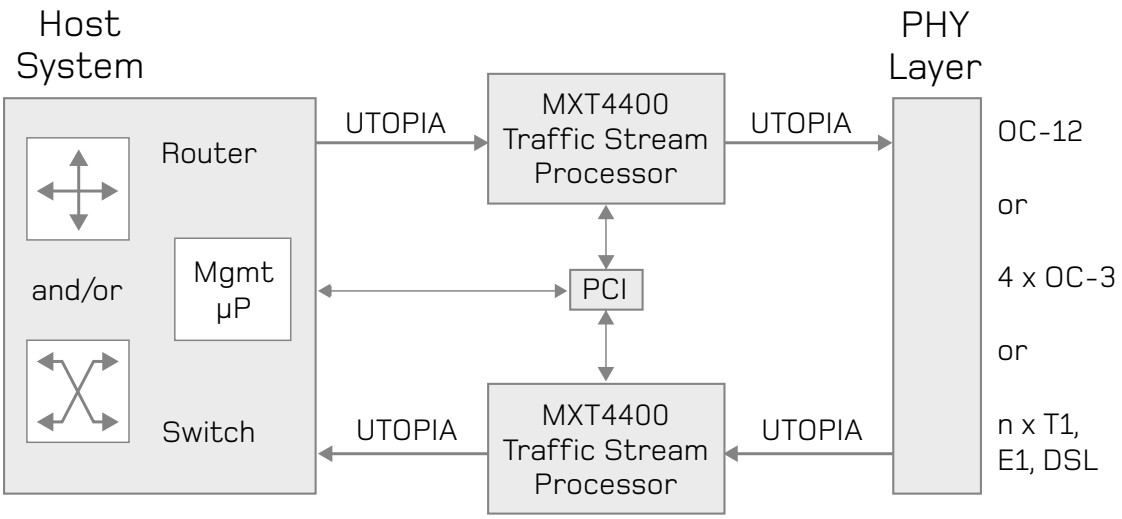
The PortMaker kernel provides the basic infrastructure or "shell" of a TSP application. The system management task spawned by the kernel communicates with external host processors, dispatches commands to services, and performs background task scheduling. PortMaker software libraries put common software routines at the disposal of service developers. By using these fully tested routines for common operations, developers can concentrate their efforts on value-added functions.

TSP Source Design Kit (SDK)

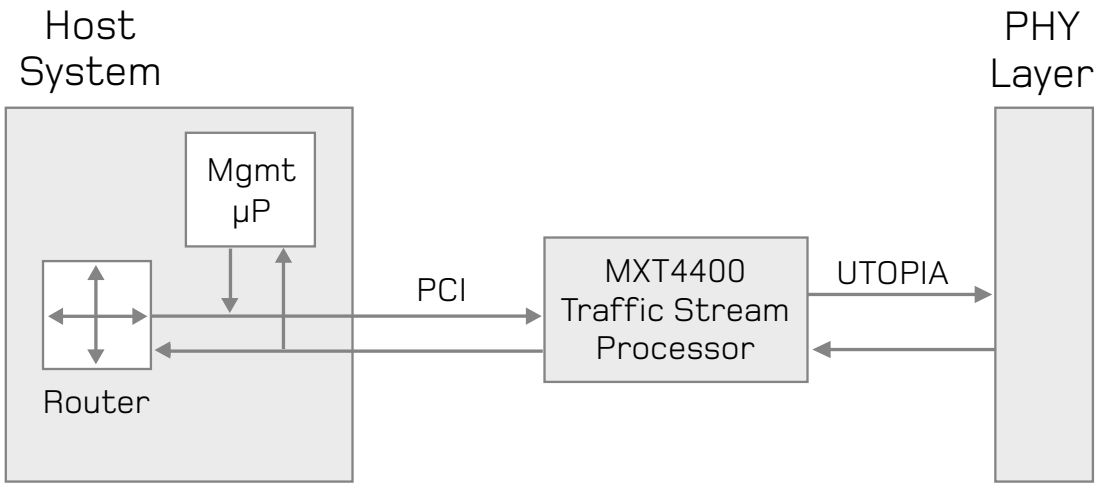
The TSP SDK is provided to source-code customers. It includes all the contents of the TSP BDK kit, as well as the code-generation tool chain and a hardware/software co-simulator. Source-code customers use the foundation of "production-ready," fully tested PortMaker services and modify or extend the functionality using the code-generation, simulation, and debugging tools provided with the TSP SDK.

Collaborative Engineering

A Collaborative Engineering program can unite Mindspeed Technologies' expertise in high-performance traffic-stream processing applications with our customers' architectural design team. Mindspeed Technologies also offers hands-on training courses with comprehensive labs and a focus on your specific design needs. With this joint commitment, system architects can capitalize on the advanced capabilities of the TSP to create high-performance traffic-stream processing applications.



High-performance switched system



Low-cost shared memory system

Applications

The MXT4400 fits within a variety of system architectures. High-performance systems exchange data with the TSP over its FIFO-like streaming interfaces. The MXT4400 also supports shared memory models for system designs optimized for low cost. Any system requiring traffic management and internetworking can take advantage of the MXT4400's flexible architecture.

Product Features

TSP Applications

- Internetworking
  - ATM SARing
  - VC/stream merging
  - Encapsulation
  - LANE
  - MPOA
  - Data forwarding
  - Multicast replication
- Buffer Management
  - 64K per-stream queues
  - Early packet discard (EPD)
  - Class-based resource isolation
- Congestion Control/Avoidance
  - Random early detection (RED, WRED)
  - Frame Relay BECN and FECN
  - ABR, VS/VD
- Bandwidth Management
  - Multilevel shaping
  - Per class
  - Per stream
  - Per tunnel/path
  - TM 4.-1-compliant
  - Dual leaky bucket shaping
  - SLA policing
  - Shaping within minimum/maximum limits
  - Class and flow WFQ
- Statistics and Alarms
- CRC and FCS error checking

Off-the-Shelf Software Applications

- PortMaker AAL5 segmentation and reassembly
- PortMaker Cell Traffic Manager

Octave Processor

- 32-bit optimized instruction set
- Background context switching
- 4K instruction cache
- 8 KB zero-latency scratchpad memory
- Interrupt, halt and trap support

Parallel Hardware Engines

- Channel Descriptor Look-Up Engine
  - Associates arriving data with one of 64K streams
  - CAM-like search
- Buffer Management Engine
  - Programmable buffer size
  - Two physical buffer pools
  - 16 logical buffer classes
  - Per-class accounting
  - Hardware buffer reclamation
- DMA Engines
  - Direct buffer reclamation
  - Buffer chaining
  - CRC-32
- Traffic Scheduling System
  - 1-32 physical ports
  - Per-stream shaping
  - 1-4 CoS priorities
  - Generic Cell Rate Algorithm (GCRA) scheduling

Physical Interfaces

- UTOPIA
  - Level I/II
  - Master or slave mode
  - 8-, 16- or 32-bit Tx/Rx
  - Cell or packet mode
  - Independently clocked to 100MHz
- PCI
  - Revision 2.2/2.1-compliant
  - 32-bit bus
  - Independently clocked to 66MHz
  - PCI master and target

External Memory

- SDRAM
  - 16 to 512 MBytes
  - 64-bit
  - 100 MHz
- SRAM
  - 1 to 4 MBytes
  - 32-bit
  - Core speed

Device Information

- Power supply: 3.3 V, 2.5 V
- I/O voltage levels: 3.3 V
- Typical Power dissipation: 3.85 W
- Package: 474 CBGA
- Body size: 32.5x25x5mm
- Ball pitch: 1.27mm
- Operation temperature: -40°C to +85°C

Development Tools

- TSP BDK – Simulation models and test benches for binary-code customers
- TSP SDK – Hardware/software development tools for source-code customers

Ordering Information

- MXT4400: CX27440-I3

www.mindspeed.com
General Information:
U.S. and Canada: (800) 854-8099
International: (949) 483-6996
Headquarters – Newport Beach
4000 MacArthur Blvd., East Tower
Newport Beach, CA 92660
Order# 500024B M01-0537

© 2001 Mindspeed Technologies™, a Conexant business. All rights reserved. Mindspeed and the Mindspeed logo are trademarks of Mindspeed Technologies. All other trademarks are the property of their respective owners. Although Mindspeed Technologies strives for accuracy in all its publications, this material may contain errors or omissions and is subject to change without notice. **This material is provided as is and without any express or implied warranties, including merchantability, fitness for a particular purpose and non-infringement.** Mindspeed Technologies shall not be liable for any special, indirect, incidental or consequential damages as a result of its use.

MINDSPEED™
A CONEXANT BUSINESS