MICROCHIP TC4426A/TC4427A/TC4428A

1.5A Dual High-Speed Power MOSFET Drivers

Features

- High Peak Output Current 1.5A
- · Wide Input Supply Voltage Operating Range:
 - 4.5V to 18V
- High Capacitive Load Drive Capability 1000 pF in 25 nsec (typ.)
- Short Delay Times 30 nsec (typ.)
- · Matched Rise, Fall and Delay Times
- · Low Supply Current:
 - With Logic '1' Input 1 mA (typ.)
 - With Logic '0' Input 100 μA (typ.)
- Low Output Impedance 7Ω (typ.)
- Latch-Up Protected: Will Withstand 0.5A Reverse Current
- Input Will Withstand Negative Inputs Up to 5V
- · ESD Protected 4 kV
- Pinouts the same as TC426/TC427/TC428 and TC4426/TC4427/TC4428
- · Space-saving 8-Pin MSOP Package

Applications

- · Switch Mode Power Supplies
- · Line Drivers
- · Pulse Transformer Drive

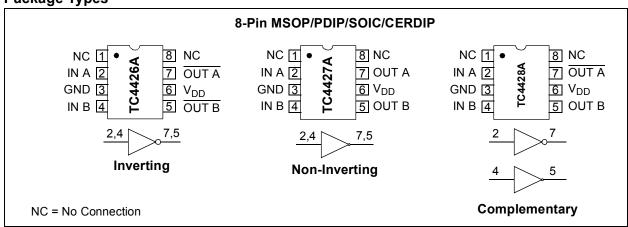
General Description

The TC4426A/TC4427A/TC4428A are improved versions of the earlier TC4426/TC4427/TC4428 family of MOSFET drivers. In addition to matched rise and fall times, the TC4426A/TC4427A/TC4428A devices have matched leading and falling edge propagation delay times.

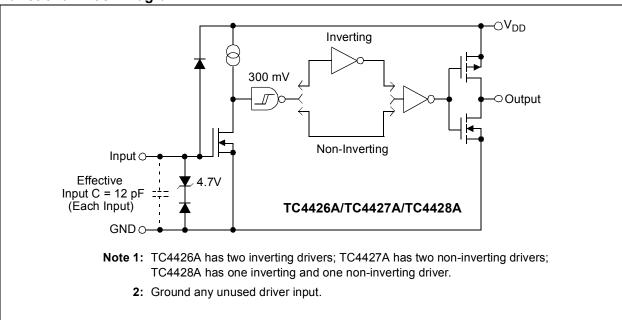
These devices are highly latch-up resistant under any conditions within their power and voltage ratings. They are not subject to damage when up to 5V of noise spiking (of either polarity) occurs on the ground pin. They can accept, without damage or logic upset, up to 500 mA of reverse current (of either polarity) being forced back into their outputs. All terminals are fully protected against electrostatic discharge up to 4 kV.

The TC4426A/TC4427A/TC4428A MOSFET drivers can easily charge/discharge 1000 pF gate capacitances in under 30 nsec and provide low enough impedances in both the 'ON' and 'OFF' states to ensure the MOSFET's intended state will not be affected, even by large transients.

Package Types



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage+22V
Input Voltage, IN A or IN B
(V _{DD} + 0.3V) to (GND – 5V
Package Power Dissipation (T _A ≤ 70°C)
PDIP730 mW
CERDIP800 mW
SOIC470 mW
MSOP 340 mW

† **Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Parameters	Sym	Min	Тур	Max	Units	Conditions
Input						
Logic '1', High Input Voltage	V _{IH}	2.4	_		V	
Logic '0', Low Input Voltage	V _{IL}	_	_	0.8	V	
Input Current	I _{IN}	-1.0 -10	_	+1.0 +10	μA	$0V \le V_{IN} \le V_{DD}$
Output						
High Output Voltage	V _{OH}	V _{DD} – 0.025	_	_	V	DC Test
Low Output Voltage	V _{OL}	_	_	0.025	V	DC Test
Output Resistance	R _O	_ _ _ _	7 7 8 8	9 10 11 12	Ω	I_{OUT} = 10 mA, V_{DD} = 18V, T_A = +25°C 0°C $\leq T_A \leq$ +70°C -40 °C $\leq T_A \leq$ +85°C -40 °C $\leq T_A \leq$ +125°C
Peak Output Current	I _{PK}	_	1.5	_	Α	V _{DD} = 18V
Latch-Up Protection Withstand Reverse Current	I _{REV}	_	>0.5	_	Α	Duty cycle \leq 2%, t \leq 300 µsec V_{DD} = 18V
Switching Time (Note 1)						
Rise Time	t _R		25 27 29 30	35 40 40 40	nsec	T_A = +25°C 0°C \leq T_A \leq +70°C -40°C \leq T_A \leq +85°C -40°C \leq T_A \leq +125°C, Figure 4-1
Fall Time	t _F	_ _ _ _	25 27 29 30	35 40 40 40	nsec	
Delay Time	t _{D1}	_ _ _ _	30 33 35 38	35 40 45 50	nsec	$T_A = +25^{\circ}C$ $0^{\circ}C \le T_A \le +70^{\circ}C$ $-40^{\circ}C \le T_A \le +85^{\circ}C$ $-40^{\circ}C \le T_A \le +125^{\circ}C$, Figure 4-1
Delay Time	t _{D2}	_ _ _ _	30 33 35 38	35 40 45 50	nsec	

Note 1: Switching times ensured by design.

DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, over operating temperature range with $4.5V \le V_{DD} \le 18V$.									
Parameters Sym Min Typ Max Units Conditions									
Power Supply									
Power Supply Current	I _S		1.0 0.1	2.0 0.2		V_{IN} = 3V (Both inputs) V_{IN} = 0V (Both inputs), V_{DD} = 18V			

Note 1: Switching times ensured by design.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless of	therwise	noted, all	paramete	rs apply wit	h 4.5V ≤	V _{DD} ≤ 18V.
Parameters	Sym	Min	Тур	Max	Units	Conditions
Temperature Ranges						
Specified Temperature Range (C)	T _A	0	_	+70	°C	
Specified Temperature Range (E)	T _A	-40	_	+85	°C	
Specified Temperature Range (M)	T _A	-55	_	+125	°C	
Specified Temperature Range (V)	T _A	-40	_	+125	°C	
Maximum Junction Temperature	TJ	_	_	+150	°C	
Storage Temperature Range	T _A	-65	_	+150	°C	
Package Thermal Resistances						
Thermal Resistance, 8L-MSOP	θ_{JA}	_	206	_	°C/W	
Thermal Resistance, 8L-PDIP	θ_{JA}	_	125	_	°C/W	
Thermal Resistance, 8L-CERDIP	θ_{JA}	_	150	_	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	_	155	_	°C/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, over operating temperature range with 4.5V \leq V_{DD} \leq 18V.

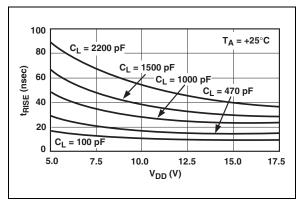


FIGURE 2-1: Rise Time vs. Supply Voltage.

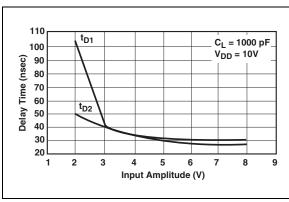


FIGURE 2-2: Delay Time vs. Input Amplitude.

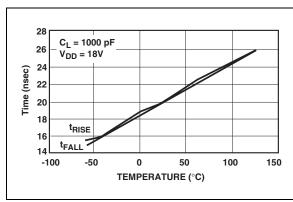


FIGURE 2-3: Rise and Fall Times vs. Temperature.

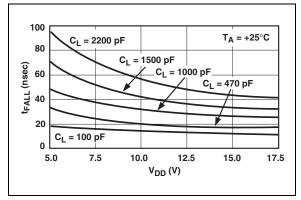


FIGURE 2-4: Fall Time vs. Supply Voltage.

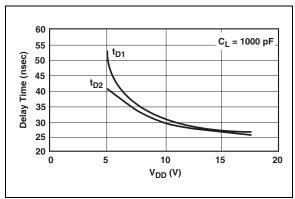


FIGURE 2-5: Propagation Delay Time vs. Supply Voltage.

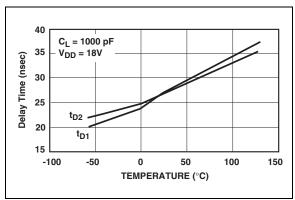


FIGURE 2-6: Propagation Delay Time vs. Temperature.

Note: Unless otherwise indicated, over operating temperature range with $4.5V \le V_{DD} \le 18V$.

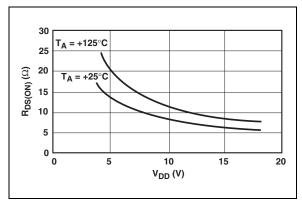


FIGURE 2-7: Resistance.

High-State Output

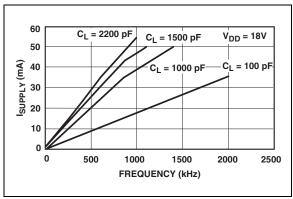


FIGURE 2-8: Frequency.

Supply Current vs.

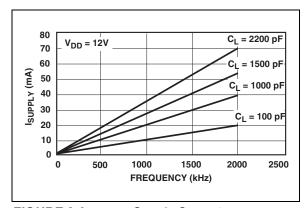


FIGURE 2-9: Frequency.

Supply Current vs.

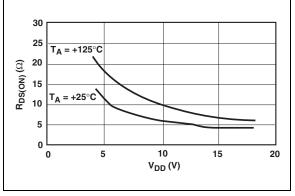


FIGURE 2-10: Resistance.

2-10: Low State Output

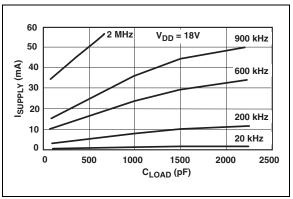


FIGURE 2-11: Capacitive Load.

Supply Current vs.

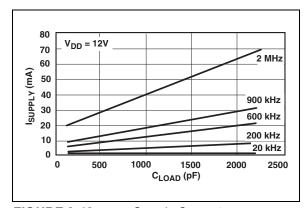


FIGURE 2-12: Capacitive Load.

Supply Current vs.

Note: Unless otherwise indicated, over operating temperature range with $4.5V \le V_{DD} \le 18V$.

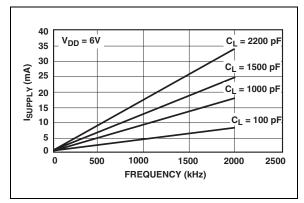


FIGURE 2-13: Supply Current vs. Frequency.

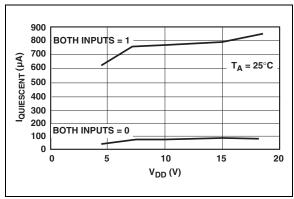


FIGURE 2-14: Quiescent Supply Current vs. Voltage.

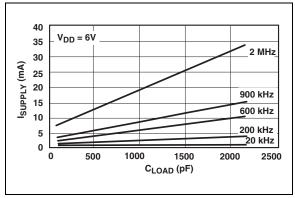


FIGURE 2-15: Supply Current vs. Capacitive Load.

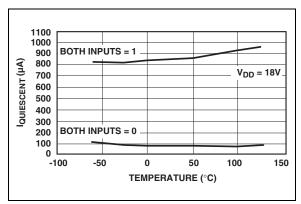


FIGURE 2-16: Quiescent Supply Current vs. Temperature.

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin No. (8-Pin MSOP, PDIP, SOIC, CERDIP)	Symbol	Description
1	NC	No connection
2	IN A	Input A
3	GND	Ground
4	IN B	Input B
5	OUT B	Output B
6	V_{DD}	Supply Input
7	OUT A	Output A
8	NC	No connection

3.1 Inputs A & B

MOSFET driver inputs A & B are high-impedance, TTL/CMOS-compatible inputs. These inputs also have 300 mV of hysteresis between the high and low thresholds, which prevents output glitching even when the rise and fall time of the input signal is very slow.

3.2 Ground (GND)

The ground pin is the return path for both the bias current and the high peak current that discharges the external load capacitance. The ground pin should be tied into a ground plane or have a very short trace to the bias supply source return.

3.3 Output A & B

MOSFET driver outputs A & B are low-impedance, CMOS push-pull style outputs. The pull-down and pull-up devices are equal strength, making the rise and fall times equivalent.

3.4 Supply Input (V_{DD})

The V_{DD} input is the bias supply for the MOSFET driver and is rated for 4.5V to 18V, with respect to the ground pin. The V_{DD} input should be bypassed with local ceramic capacitors. The value of these capacitors should be chosen based on the capacitive load that is being driven.

4.0 APPLICATIONS INFORMATION

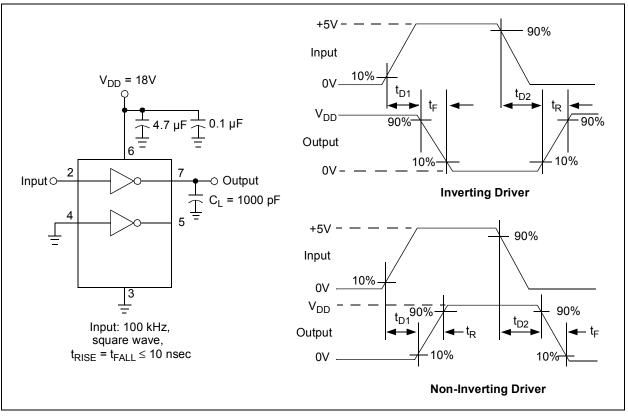
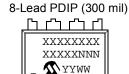


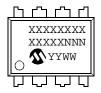
FIGURE 4-1: Switching Time Test Circuit.

5.0 PACKAGING INFORMATION

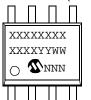
5.1 Package Marking Information



8-Lead CERDIP (300 mil)



8-Lead SOIC (150 mil)



8-Lead MSOP



Example:



Example:



Example:



Example:



Legend: XX...X Customer specific information*

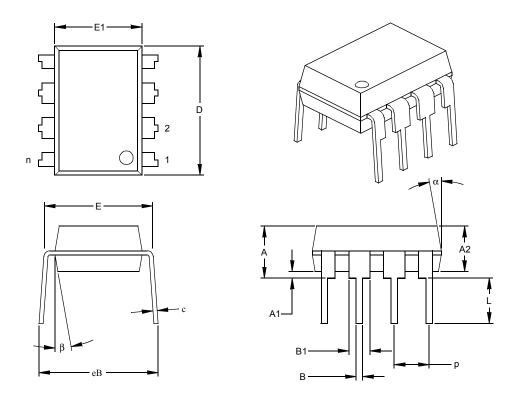
YY Year code (last 2 digits of calendar year)
WW Week code (week of January 1 is week '01')

NNN Alphanumeric traceability code

bte: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

* Standard marking consists of Microchip part number, year code, week code, traceability code (facility code, mask rev#, and assembly code).

8-Lead Plastic Dual In-line (PA) - 300 mil (PDIP)



	Units		INCHES*			MILLIMETERS		
Dimensi	ion Limits	MIN	NOM	MAX	MIN	NOM	MAX	
Number of Pins	n		8			8		
Pitch	р		.100			2.54		
Top to Seating Plane	Α	.140	.155	.170	3.56	3.94	4.32	
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68	
Base to Seating Plane	A1	.015			0.38			
Shoulder to Shoulder Width	Е	.300	.313	.325	7.62	7.94	8.26	
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60	
Overall Length	D	.360	.373	.385	9.14	9.46	9.78	
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43	
Lead Thickness	С	.008	.012	.015	0.20	0.29	0.38	
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78	
Lower Lead Width	В	.014	.018	.022	0.36	0.46	0.56	
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92	
Mold Draft Angle Top	α	5	10	15	5	10	15	
Mold Draft Angle Bottom	β	5	10	15	5	10	15	

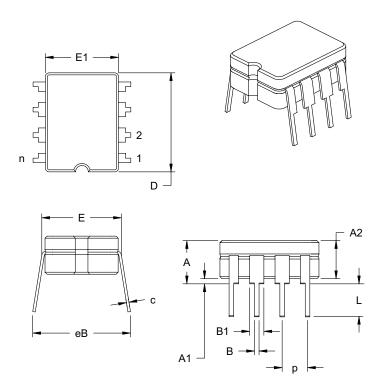
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed

.010" (0.254mm) per side. JEDEC Equivalent: MS-001

Drawing No. C04-018

^{*} Controlling Parameter § Significant Characteristic

8-Lead Ceramic Dual In-line – 300 mil (CERDIP)

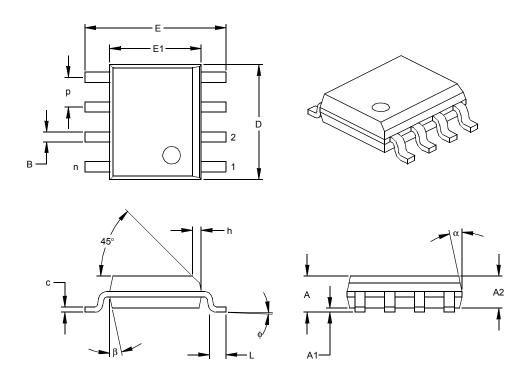


	Units	INCHES*			N	;	
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	р		.100			2.54	
Top to Seating Plane	Α	.160	.180	.200	4.06	4.57	5.08
Standoff §	A1	.020	.030	.040	0.51	0.77	1.02
Shoulder to Shoulder Width	E	.290	.305	.320	7.37	7.75	8.13
Ceramic Pkg. Width	E1	.230	.265	.300	5.84	6.73	7.62
Overall Length	D	.370	.385	.400	9.40	9.78	10.16
Tip to Seating Plane	L	.125	.163	.200	3.18	4.13	5.08
Lead Thickness	С	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.055	.065	1.14	1.40	1.65
Lower Lead Width	В	.016	.018	.020	0.41	0.46	0.51
Overall Row Spacing	eВ	.320	.360	.400	8.13	9.15	10.16

*Controlling Parameter
JEDEC Equivalent: MS-030

Drawing No. C04-010

8-Lead Plastic Small Outline (OA) - Narrow, 150 mil (SOIC)



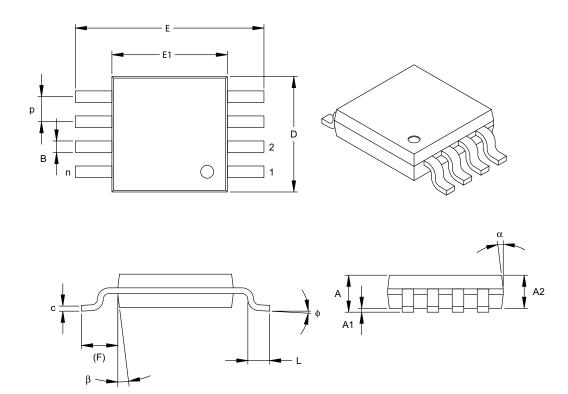
	Units	INCHES*			MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	р		.050			1.27	
Overall Height	Α	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	Е	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	ф	0	4	8	0	4	8
Lead Thickness	С	.008	.009	.010	0.20	0.23	0.25
Lead Width	В	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

^{*} Controlling Parameter § Significant Characteristic

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed

.010" (0.254mm) per side. JEDEC Equivalent: MS-012 Drawing No. C04-057

8-Lead Plastic Micro Small Outline Package (UA) (MSOP)



	Units	INCHES			М	*	
Dimension Lin	nits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	р		.026 BSC			0.65 BSC	
Overall Height	Α	-	-	.043	-	-	1.10
Molded Package Thickness	A2	.030	.033	.037	0.75	0.85	0.95
Standoff	A1	.000	-	.006	0.00	-	0.15
Overall Width	E		.193 TYP.		4.90 BSC		
Molded Package Width	E1		.118 BSC		3.00 BSC		
Overall Length	D		.118 BSC		3.00 BSC		
Foot Length	L	.016	.024	.031	0.40	0.60	0.80
Footprint (Reference)	F		.037 REF		0.95 REF		
Foot Angle	ф	0°	-	8°	0°	-	8°
Lead Thickness	С	.003	.006	.009	0.08	-	0.23
Lead Width	В	.009	.012	.016	0.22	-	0.40
Mold Draft Angle Top	α	5°	-	15°	5°	-	15°
Mold Draft Angle Bottom	β	5°	ı	15°	5°	-	15°

^{*}Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MO-187

Drawing No. C04-111

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	<u>X</u> / <u>XX</u>	Examples:				
Device 1	Femperature Package Range	a)	TC4426ACOA:	1.5A Dual MOSFET driver, SOIC package, 0°C to +70°C.		
Device:	TC4426A: 1.5A Dual MOSFET Driver, Inverting TC4427A: 1.5A Dual MOSFET Driver, Non-Inverting	b)	TC4426AEOA:	1.5A Dual MOSFET driver, SOIC package, -40°C to +85°C.		
Temperature Range:	TC4428A: 1.5A Dual MOSFET Driver, Complimentary C = 0°C to +70°C (PDIP & SOIC Only)	a)	TC4427ACPA:	1.5A Dual MOSFET driver, PDIP package, 0°C to +70°C.		
	E = -40°C to +85°C V = -40°C to +125°C M = -55°C to +125°C (CERDIP only)	b)	TC4427AEPA:	1.5A Dual MOSFET driver, PDIP package, -40°C to +85°C.		
Package:	JA = Ceramic Dual In-line (300 mil Body), 8-lead OA = Plastic SOIC, (150 mil Body), 8-lead OA713 = Plastic SOIC, (150 mil Body), 8-lead	a)	TC4428AMJA:	1.5A Dual MOSFET driver, CDIP package, -55°C to +125°C.		
	(Tape and Reel) PA = Plastic DIP (300 mil Body), 8-lead UA = Plastic Micro Small Outline (MSOP), 8-lead UA713 = Plastic Micro Small Outline (MSOP), 8-lead (Tape and Reel)	b)	TC4428ACOA713:	1.5A Dual MOSFET driver, Tape and Reel, SOIC package, 0°C to +70°C.		

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

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- 2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
- 3. The Microchip Worldwide Site (www.microchip.com)

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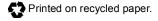
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WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office

2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tel: 480-792-7200

Fax: 480-792-7277 Technical Support: 480-792-7627 Web Address: http://www.microchip.com

Atlanta

3780 Mansell Road, Suite 130 Alpharetta, GA 30022 Tel: 770-640-0034 Fax: 770-640-0307

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ASIA/PACIFIC

Australia

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Fax: 61-2-9868-6755

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Tel: 86-532-5027355 Fax: 86-532-5027205

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82-2-558-5934

Singapore 200 Middle Road #07-02 Prime Centre Singapore, 188980

Tel: 65-6334-8870 Fax: 65-6334-8850

Taiwan

Kaohsiung Branch 30F - 1 No. 8 Min Chuan 2nd Road Kaohsiung 806, Taiwan Tel: 886-7-536-4818 Fax: 886-7-536-4803

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Steinheilstrasse 10 D-85737 Ismaning, Germany Tel: 49-89-627-144-0 Fax: 49-89-627-144-44

Italy

Via Quasimodo, 12 20025 Legnano (MI) Milan, Italy Tel: 39-0331-742611 Fax: 39-0331-466781

Fax: 33-1-69-30-90-79

Netherlands

P. A. De Biesbosch 14 NL-5152 SC Drunen, Netherlands Tel: 31-416-690399

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Berkshire, England RG41 5TU Tel: 44-118-921-5869 Fax: 44-118-921-5820

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