REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add packages T and W. Add vendor CAGE 60395 as source of supply. Increase data retention to 20 years, minimum. Redrawn with changes.	93-06-29	M. A. Frye
B	Changes in accordance with NOR 5962-R139-94.	94-03-29	M. A. Frye
C	Changes in accordance with NOR 5962-R278-94.	94-09-19	M. A. Frye
D	Changes in accordance with NOR 5962-R163-96.	96-06-27	M. A. Frye
E	Updated boilerplate. Added device types 16-18 and packages M and N to drawing along with vendor CAGE 0EU86 as supplier. Removed figures 9, 10 and 11 software data protect algorithms. Removed vendor 61395 as supplier. - glg	98-07-22	Raymond Monnin
F	Corrected dimensions for packages "M" and "N". - glg	99-10-06	Raymond Monnin
G	Added device 19, packages 6 and 7, and updated boilerplate. ksr	01-10-05	Raymond Monnin
H	5 year review, updated boilerplate paragraphs. ksr	06-05-15	Raymond Monnin

The original first page has been replaced.

REV	H	H																		
SHEET	35	36																		
REV	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS	REV	H	H	H	H	H	H	H	H	H	H	H	H	H
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Kenneth Rice

CHECKED BY
Charles Reusing

APPROVED BY
Charlie Besore

DRAWING APPROVAL DATE
91-07-12

REVISION LEVEL
H

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE
FOR USE BY ALL DEPARTMENTS
AND AGENCIES OF THE
DEPARTMENT OF DEFENSE
AMSC N/A

DEFENSE SUPPLY CENTER COLUMBUS

COLUMBUS, OHIO 43218-3990

http://www.dscc.dla.mil

MICROCIRCUIT, MEMORY, DIGITAL, CMOS 128K x 8 BIT EEPROM, MONOLITHIC SILICON

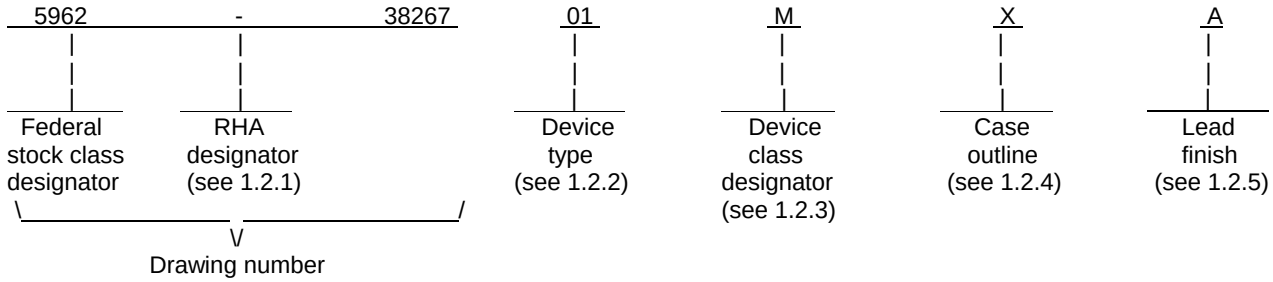
SIZE	CAGE CODE	
A	**67268**	**5962-38267**

SHEET 1 OF 36

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time	Write speed	Write mode	Endurance	Software data protect
01,16	1/	128K x 8 EEPROM	250 ns	10 ms	Byte/Page	10,000 cycle	yes
02		128K x 8 EEPROM	250 ns	5 ms	Byte/Page	10,000 cycle	yes
03,17		128K x 8 EEPROM	200 ns	10 ms	Byte/Page	10,000 cycle	yes
04		128K x 8 EEPROM	200 ns	5 ms	Byte/Page	10,000 cycle	yes
05,18		128K x 8 EEPROM	150 ns	10 ms	Byte/Page	10,000 cycle	yes
06		128K x 8 EEPROM	150 ns	5 ms	Byte/Page	10,000 cycle	yes
07,19		128K x 8 EEPROM	120 ns	10 ms	Byte/Page	10,000 cycle	yes
08		128K x 8 EEPROM	120 ns	3 ms	Byte/Page	10,000 cycle	yes
09		128K x 8 EEPROM	90 ns	10 ms	Byte/Page	10,000 cycle	yes
10		128K x 8 EEPROM	90 ns	3 ms	Byte/Page	10,000 cycle	yes
11		128K x 8 EEPROM	70 ns	10 ms	Byte/Page	10,000 cycle	yes
12		128K x 8 EEPROM	70 ns	3 ms	Byte/Page	10,000 cycle	yes
13		128K x 8 EEPROM	120 ns	3 ms	Byte/Page	10,000 cycle	yes
14		128K x 8 EEPROM	90 ns	3 ms	Byte/Page	10,000 cycle	yes
15		128K x 8 EEPROM	70 ns	3 ms	Byte/Page	10,000 cycle	yes

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in QML-38535 and MIL-HDBK-103.

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T32 or CDIP2-T32	32	Dual in-line
Y	CQCC1-N44	44	Square chip carrier
Z	See figure 1	32	Flat package
U	CQCC1-N32	32	Rectangular chip carrier
T	See figure 1	30	Grid array
W	See figure 1	36	Grid array
M	See figure 1	32	Flat package
N	See figure 1	32	Flat package
6	See figure 1(enhanced rad tolerant)	32	Flat package
7	See figure 1(enhanced rad tolerant)	32	Flat package

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 2/ 3/

Supply voltage range (V_{CC})	-0.5 V dc to +6.0 V dc 4/
Operating case temperature range	-55°C to +125°C
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC}):	
Cases X, Y and U	See MIL-STD-1835
Cases T and W	21°C/W 5/
Case Z	18°C/W 5/
Case M	3°C/W 5/
Case N	2°C/W 5/
Case 6	1.5°C/W 5/
Case 7	1.5°C/W 5/
Maximum power dissipation (P_D)	1.0 watts
Junction temperature (T_J)	+175°C 6/
Endurance	10,000 cycles/byte (minimum)
Data retention	20 years minimum

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Supply voltage (V_{SS})	0.0 V dc
High level input voltage range (V_{IH})	2.0 V dc to V_{CC} + 1.0 V dc 7/
Low level input voltage range (V_{IL})	-0.1 V dc to 0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	100 percent

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

3/ All voltages referenced to V_{SS} (V_{SS} = ground), unless otherwise specified.

4/ Negative undershoots to a minimum of -1.0 V are allowed with a maximum of 20 ns pulse width.

5/ When the thermal resistance for this case is specified in MIL-STD-1835, that value shall supersede the value indicated herein.

6/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

7/ For device types 16-19 only, V_{IH} on $\overline{RES}$ shall be V_{CC} - 0.5 V min. to V_{CC} + 1.0 V max.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-00 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to: ASTM International, PO Box C700, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959; http://www.astm.org.)

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard EIA/JESD78 - IC Latch-Up Test.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201; http://www.jedec.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 3 herein. When required, in screening (see 4.2 herein), or quality conformance inspection groups A, B, C, or D (see 4.4 herein), the devices shall be programmed by the manufacturer prior to test in a checkerboard or similar pattern (a minimum of 50 percent of the total number of bits programmed).

3.2.3.2 Programmed devices. The requirements for supplying programmed devices are not part of this document.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-PRF-38535, appendix A).

3.11 Processing of EEPROMs. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.11.1 Conditions of the supplied devices. Devices will be supplied in an unprogrammed or clear state. No provision will be made for supplying programmed devices.

3.11.2 Erasure of EEPROMs. When specified, devices shall be erased in accordance with procedures and characteristics specified in 4.5.1.

3.11.3 Programming of EEPROMs. When specified, devices shall be programmed in accordance with procedures and characteristics specified in 4.5.2.

3.11.4 Verification of state of EEPROMs. When specified, devices shall be verified as either written to the specified pattern or cleared. As a minimum, verification shall consist of performing a read of the entire array to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure and the device shall be removed from the lot or sample.

3.11.5 Power supply sequence of EEPROMs. In order to reduce the probability of inadvertent writes, the following power supply sequences shall be observed.

a. For device types 1-19, a logic high state shall be applied to $\overline{WE}$ and/or $\overline{CE}$ at the same time or before the application of V_{CC}. For device types 16-19, an additional precaution is available; a logic low state shall be applied to $\overline{RES}$ at the same time or before the application of V_{CC}.

b. For device types 1-19, a logic high state shall be applied to $\overline{WE}$ and/or $\overline{CE}$ at the same time or before the removal of V_{CC}. For device types 16-19, an additional precaution is available; a logic low state shall be applied to $\overline{RES}$ at the same time or before the removal of V_{CC}.

3.12 Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitors. This reprogrammability test shall be done for initial characterization and after any design or process changes which may affect the reprogrammability of the device. The methods and procedures may be vendor specific, but shall guarantee the number of program/erase endurance cycles listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

3.13 Data retention. A data retention stress test shall be completed as part of the vendor's reliability monitors. This test shall be done for initial characterization and after any design or process change which may affect data retention. The methods and procedures may be vendor specific, but shall guarantee the number of years listed in section 1.3 herein over the full military temperature range. The vendor's procedure shall be kept under document control and shall be made available upon request of the acquiring or preparing activity, along with test data.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V; $4.5 \text{ V} \le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
High level input current	I_{IH}	$V_{CC} = 5.5$ V, $V_{IN} = 5.5$ V	1, 2, 3	All	-5	5	µA
Low level input current	I_{IL}	$V_{CC} = 5.5$ V, $V_{IN} = 0.1$ V	1, 2, 3	All	-5	5	µA
		For $\overline{RES}$ input		16-19	-100	100	
High impedance output leakage current 1/	I_{OZH}	$V_{IH} \le \overline{OE} \le V_{CC}$ $V_{CC} = 5.5$ V, $V_O = 5.5$ V	1, 2, 3	All	-10	10	µA
	I_{OZL}	$V_{IH} \le \overline{OE} \le V_{CC}$ $V_{CC} = 5.5$ V, $V_O = 0.0$ V	1, 2, 3		-10	10	
Output high voltage	V_{OH}	$I_{OH} = -400$ µA, $V_{CC} = 4.5$ V $V_{IH} = 2.0$ V, $V_{IL} = 0.8$ V	1, 2, 3	All	2.4		V
Output low voltage	V_{OL}	$I_{OL} = 2.1$ mA, $V_{CC} = 4.5$ V $V_{IH} = 2.0$ V, $V_{IL} = 0.8$ V	1, 2, 3	All		0.4	V
Input high voltage 2/	V_{IH}	$V_{CC} = 5.5$ V	1, 2, 3	01-15	2.0	6.0	V
				16-19	2.2	6.0	
Input low voltage 2/	V_{IL}	$V_{CC} = 4.5$ V	1, 2, 3	All	-0.5	0.8	V
$\overline{OE}$ high voltage	V_H		1, 2, 3	01-15	12	13	V
$\overline{RES}$ high voltage				16-19	V_{CC} - 0.5	V_{CC} + 1.0	
Operating supply current	I_{CC1}	$V_{CC} = 5.5$ V, $\overline{WE} = V_{IH}$, $\overline{CE} = \overline{OE} = V_{IL}$ $f = 1/t_{AVAV}$ min	1, 2, 3	01-06, 08,13, 16,17		80	mA
				07,18, 19		100	
				09-12, 14,15		120	
Standby supply current TTL	I_{CC2}	$V_{CC} = 5.5$ V, $\overline{CE} = V_{IH}$, all I/O's = open, $\overline{OE} = V_{IL}$, f = 0 Hz	1, 2, 3	All		3	mA
Standby supply current CMOS	I_{CC3}	$V_{CC} = 5.5$ V, $\overline{CE} = V_{CC} - 0.3$ V Inputs = V_{IH}, I/O's = open, $\overline{OE} = V_{IL}$, f = 0 Hz	1, 2, 3	01-07		850	µA
				08-12		500	
				13-15, 16-19		350	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V; $4.5 V \le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Input capacitance 3/ 4/	C_{IN}	$V_{IN} = 0$ V, f = 1.0 MHz, $T_C = +25°C$, see 4.4.1c	4	All		10.0	pF
Output capacitance 3/ 4/	C_{OUT}	$V_{OUT} = 0$ V, f = 1.0 MHz $T_C = +25°C$, see 4.4.1c	4	All		12.0	pF
Functional tests		See 4.4.1d	7,8A,8B	All			
Read cycle time	t_{AVAV}	See figures 4, 5, and 6 as applicable. 5/	9, 10, 11	01-02,16	250		ns
				03-04,17	200		
				05-06,18	150		
				07,08, 13,19	120		
				09,10, 14	90		
				11,12, 15	70		
Address access time	t_{AVQV}		9, 10, 11	01-02,16		250	ns
				03-04,17		200	
				05-06,18		150	
				07,08, 13,19		120	
				09,10, 14		90	
				11,12, 15		70	
$\overline{CE}$ access time	t_{ELQV}		9, 10, 11	01-02,16		250	ns
				03-04,17		200	
				05-06,18		150	
				07,08, 13,19		120	
				09,10, 14		90	
				11,12, 15		70	
$\overline{OE}$ access time	t_{OLQV}		9, 10, 11	01-06		55	ns
				07-15		50	
				16-19		75	
$\overline{CE}$ to output in low Z 4/	t_{ELQX}		9, 10, 11	All	0		ns
Chip disable to output in high Z 4/	t_{EHQZ}		9, 10, 11	01-06		55	ns
				07-19		50	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V; $4.5 V \le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
$\overline{OE}$ to output in low Z 4/	t_{OLQX}	See figures 4, 5, and 6 as applicable. 5/	9, 10, 11	All	0		ns
Output disable to output in high Z 4/	t_{OHQZ}		9, 10, 11	01-06		55	ns
				07-19		50	
Output hold from address change	t_{AXQX}		9, 10, 11	All	0		ns
Write cycle time	t_{WHWL1} t_{EHEL1}		9, 10, 11	01,03, 05,07, 09,11, 16-19		10	ms
				02,04 06		5	
				08,10, 12-15		3	
Address setup time	t_{AVWL} t_{AVEL}		9, 10, 11	All	0		ns
Address hold time	t_{WLAX} t_{ELAX}		9, 10, 11	16-19	150		ns
				01-08, 13	70		
				09-12, 14,15	50		
Write setup time	t_{ELWL} t_{WLEL}		9, 10, 11	All	0		ns
Write hold time	t_{WHEH} t_{EHWH}		9, 10, 11	All	0		ns
$\overline{OE}$ setup time	t_{OHWL} t_{OHEL}		9, 10, 11	01-15	10		ns
				16-19	0		
$\overline{OE}$ hold time	t_{WHOL} t_{EHOL}		9, 10, 11	01-15	10		ns
				16-19	0		
Write pulse width (page or byte write)	t_{WLWH} t_{ELEH}		9, 10, 11	01-15	100		ns
				16-19	250		
Data setup time	t_{DVWH} t_{DVEH}		9, 10, 11	16-19	100		ns
				01-08, 13	60		
				09-12, 14,15	40		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{SS} = 0 V; 4.5 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Data hold time	t_{WHDX} t_{EHDX}	See figures 4, 5, and 6 as applicable. 5/	9, 10, 11	01-07 16-19	10		ns
				08-15	0		
Byte load cycle	t_{WHWL2}		9, 10, 11	01-15	.20	149	µs
				16-19	.3	30	
Last byte loaded to data polling	t_{WHEL} t_{EHEL}		9, 10, 11	01-02,16		250	ns
				03-04,17		200	
				05-06,18		150	
				07,08, 13,19		120	
				09,10, 14		90	
				11,12, 15		70	
$\overline{CE}$ setup time (chip erase)	t_{ELWL}	See figures 4, 5, and 6 as applicable. 5/ 6/	9, 10, 11	01-15	5		µs
$\overline{OE}$ setup time (chip erase)	t_{OVHWL}		9, 10, 11	01-15	5		µs
$\overline{WE}$ pulse width (chip erase)	t_{WLWH2}		9, 10, 11	01-07	10		ms
				08-15	10		µs
$\overline{CE}$ hold time (chip erase)	t_{WHEH}		9, 10, 11	01-15	5		µs
$\overline{OE}$ hold time (chip erase)	t_{WHOH}		9, 10, 11	01-15	5		µs
High voltage (chip erase)	V_H		9, 10, 11	01-15	12	13	V
Clear recovery (chip erase)	t_{OLEL}		9, 10, 11	01-15		50	ms
Data setup time (chip erase) 7/	t_{DHWL}		9, 10, 11	01-15	1		µs
Data hold time during chip erase cycle 7/	t_{WHDX}		9, 10, 11	01-15	1		µs

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{SS} = 0$ V; $4.5 V \le V_{CC} \le 5.5$ V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
$\overline{RES}$ low to output float	t_{DFR}	See figures 4, 5, and 6 as applicable. 5/ 8/	9, 10, 11	16-19	0	350	ns
$\overline{RES}$ to output delay	t_{RR}		9, 10, 11	16-19	0	450	ns
Reset protect time	t_{RP}		9, 10, 11	16-19	100		µs
Reset high time	t_{RES}		9, 10, 11	16-19	1.0		µs
Time to device busy	t_{DB}		9, 10, 11	16-19	120		ns

1/ Connect all address inputs and $\overline{OE}$ to V_{IH} and measure I_{OZL} and I_{OZH} with the output under test connected to V_{OUT}. Terminal conditions for the output leakage current test shall be as follows:
   a. $V_{IH} = 2.0$ V for device types 01-15 and 2.2 V for device types 16-19; $V_{IL} = 0.8$ V.
   b. For I_{OZL}: Select an appropriate address to acquire a logic "1" on the designated output. Apply V_{IH} to $\overline{CE}$. Measure the leakage current while applying the specified voltage.
   c. For I_{OZH}: Select an appropriate address to acquire a logic "0" on the designated output. Apply V_{IH} to $\overline{CE}$. Measure the leakage current while applying the specified voltage.

2/ A functional test shall verify the dc input and output levels and applicable patterns as appropriate, all input and I/O pins shall be tested. Terminal conditions are as follows:
   a. Inputs: H =2.0 V for device types 01-15 and 2.2 V for device types 16-19; L = 0.8 V. Outputs: H = 2.4 V minimum and L = 0.4 V maximum.
   b. The functional tests shall be performed with $V_{CC} = 4.5$ and $V_{CC} = 5.5$ V.

3/ All pins not being tested are to be open.

4/ Tested initially and after any design or process changes which may affect that parameter, and therefore shall be guaranteed to the limits specified in table I.

5/ Tested by application of specified timing signals and conditions.
   Equivalent ac test conditions:
   Output load, see figure 5; input rise and fall times ≤ 10 ns; input pulse levels, 0.4 V and 2.4 V; timing measurement reference levels, inputs, 1.5 V for device types 1-15 and 1 V and 2 V for device types 16-19; outputs, 1.5 V for device types 1-15 and 0.8 V and 2 V for device types 16-19.

6/ Chip erase functions are applicable to device types 01-15 only.

7/ This parameter not applicable for internal timer controlled devices.

8/ $\overline{RES}$ functions are applicable to device types 16-19 only.

Case T

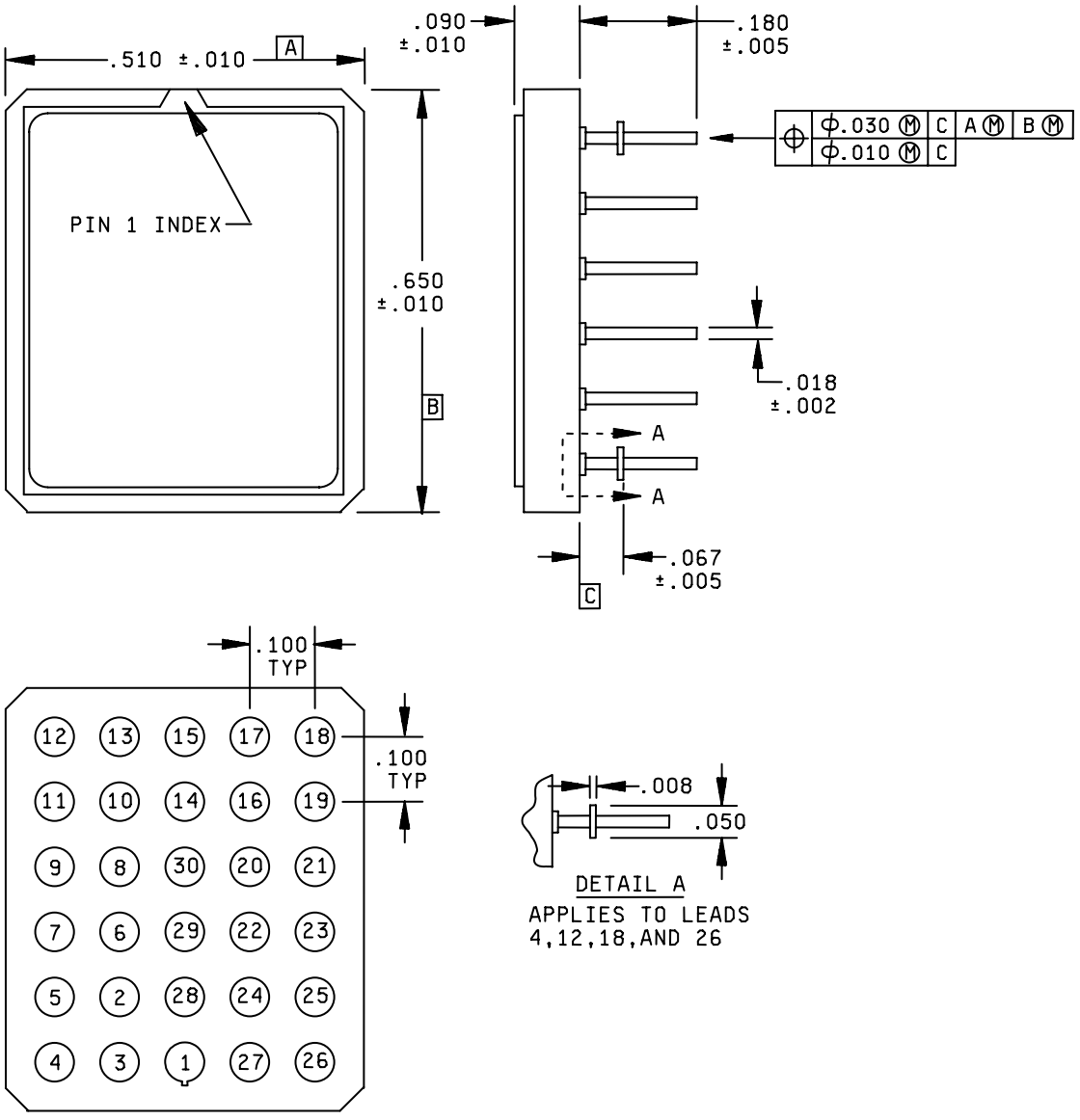


FIGURE 1. Case outline.

Case W

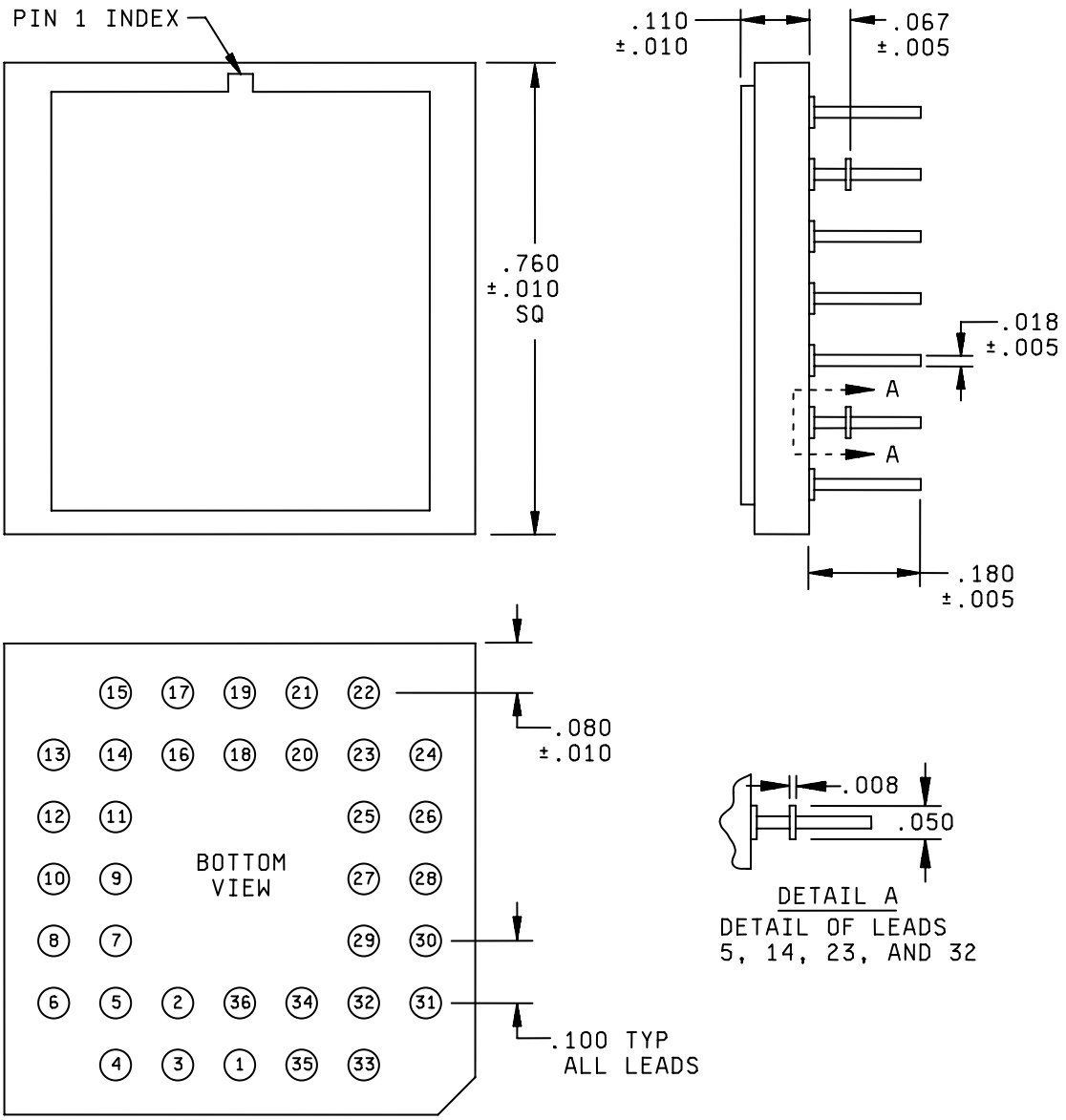


FIGURE 1. Case outline – Continued.

Case Z

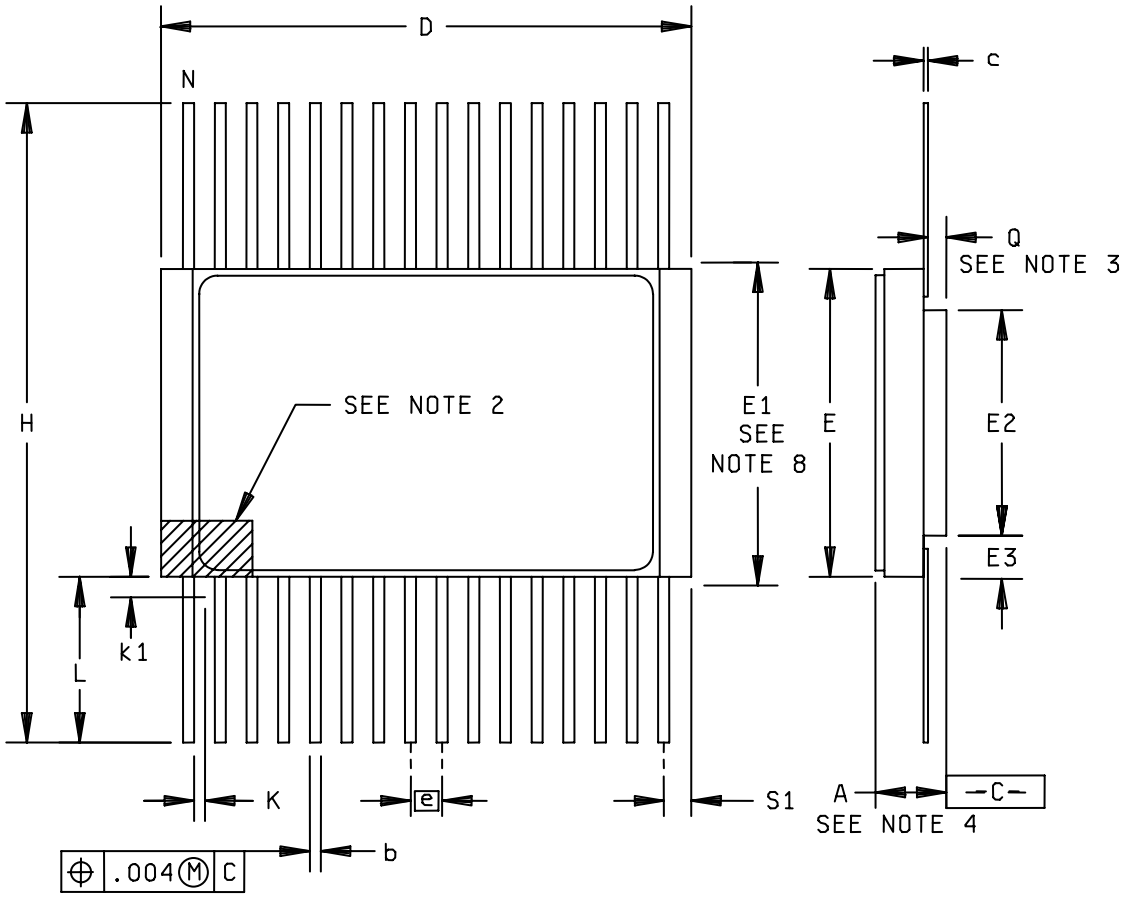


FIGURE 1. Case outline – Continued.

Case Z

Variations (all dimensions shown in inches)			
Symbol	Min	Max	Notes
A	.090	.120	4
b	.015	.020	
c	.004	.007	
D		..830	
E	.430	.488	
E1		.498	
E2	.330		8
E3	.030		
e	.050 BSC		
H		1.228	
K	.008	.015	2, 5
k1	.025 ref		2, 5
L	.270	.370	
Q	.026	.045	3
S1		.045	
N	32		6

Inches	mm	Inches	mm	Inches	mm
.004	0.10	.020	0.51	.270	6.86
.005	0.13	.025	0.64	.350	8.89
.006	0.15	.026	0.66	.370	9.40
.007	0.18	.030	0.76	.472	11.99
.008	0.20	.045	1.14	.488	12.40
.015	0.38	.050	1.27	.498	12.65
.019	0.48	.120	3.05	1.228	31.19

NOTES:
1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Index area: An identification mark shall be located adjacent to pin 1 within the shaded area shown. Alternatively, a tab (dim k) may be used as shown.
3. Dimension Q shall be measured from the point on the lead located opposite the braze pad.
4. This dimension includes lid thickness.
5. Optional, see note 2. If pin 1 identification is used instead of this tab, the minimum dimension does not apply.
6. (N) indicates number of leads.
7. Uses a metal lid.
8. Includes braze fillet.
9. Metric equivalents are given for general information only.

FIGURE 1. Case outline – Continued.

Case M

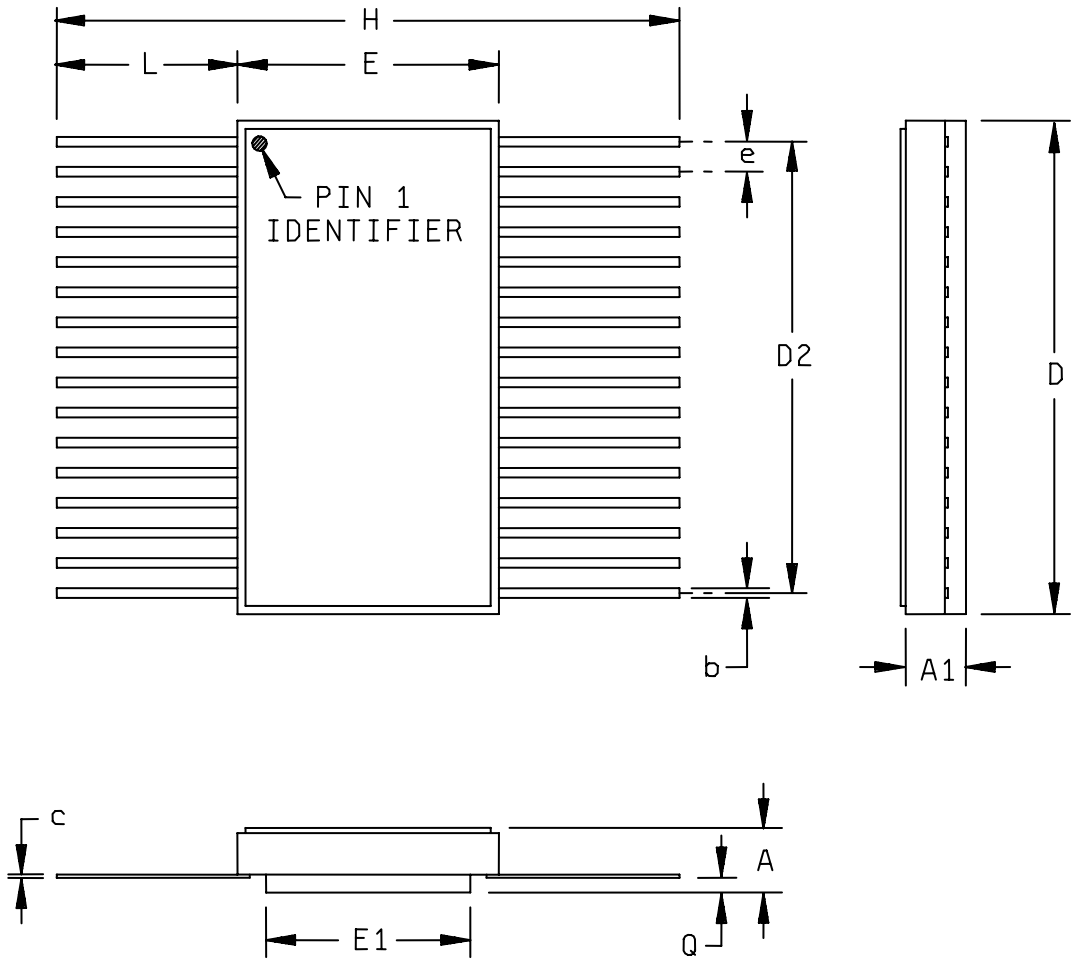


FIGURE 1. Case outline – Continued.

Case M

Variations				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.46	3.12	.097	.123
A1	2.29	2.79	.090	.110
b	.038	.048	.015	.019
c	0.08	0.18	.003	.007
D	20.57	21.08	.810	.830
D2	18.92	19.18	.745	.755
E	10.80	11.30	.425	.445
E1	8.38	9.04	.330	.356
e	1.14	1.40	.045	.055
H	25.40	27.94	1.00	1.10
L	7.37	7.87	.290	.310
Q	0.66	0.94	.026	.037
N	32			

NOTE: Although dimensions are in inches, the US government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the two, the inch-pound units shall take precedence. Metric equivalents are for general information only.

FIGURE 1. Case outline – Continued.

Case N

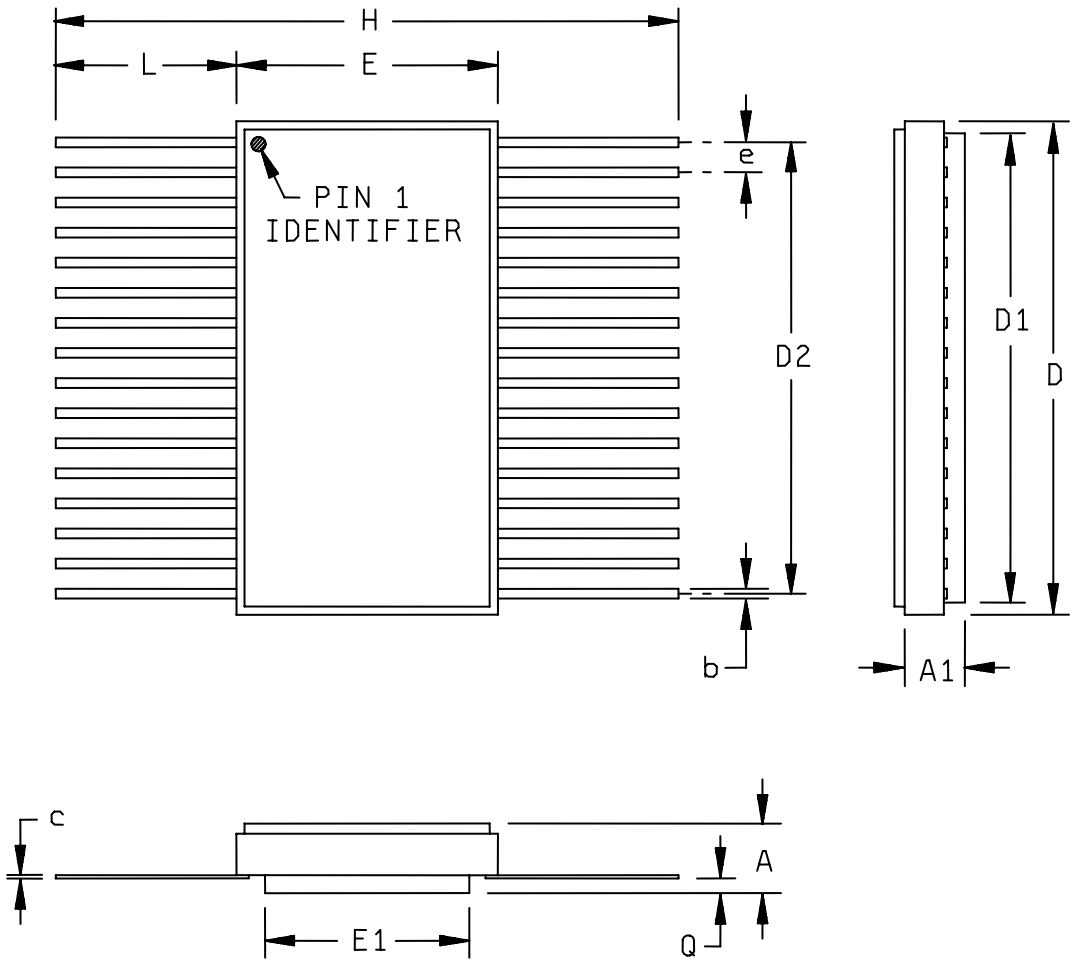


FIGURE 1. Case outline – Continued.

Case N

Variations				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	3.18	3.81	.125	.150
A1	2.29	2.79	.090	.110
b	0.38	0.48	.015	.019
c	0.08	0.18	.003	.007
D	20.57	21.08	.810	.830
D1	19.69	19.94	.775	.785
D2	18.92	19.18	.745	.755
E	10.80	11.30	.425	.445
E1	7.37	7.87	.290	.310
e	1.14	1.40	.045	.055
H	25.40	27.94	1.00	1.10
L	7.37	7.87	.290	.310
Q	0.66	0.94	.026	.037
N	32			

NOTE: Although dimensions are in inches, the US government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the two, the inch-pound units shall take precedence. Metric equivalents are for general information only.

FIGURE 1. Case outline – Continued.

Case 6

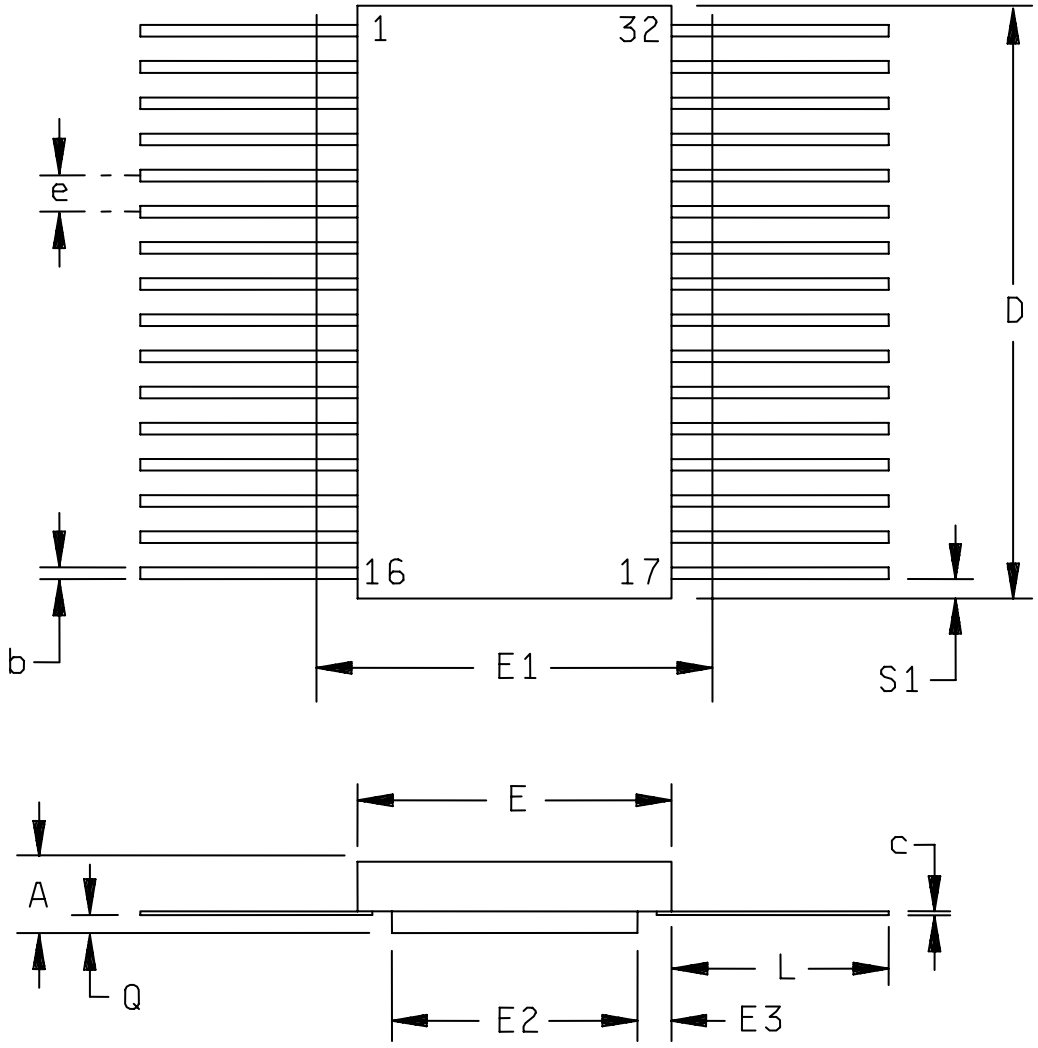


FIGURE 1. Case outline – Continued.

Case 6

Variations				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	3.07	3.81	.121	.150
b	0.38	0.56	.015	.022
c	0.10	0.18	.004	.009
D		21.08		.830
E	11.99	12.40	.472	.488
E1		7.87		.498
E2	7.72		.304	
E3	0.76		.030	
e	1.27		.050 BSC	
S1	0.13		.005	
L	9.02	9.53	.355	.375
Q	0.51	1.14	.020	.045
N	32			

NOTE: Although dimensions are in inches, the US government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the two, the inch-pound units shall take precedence. Metric equivalents are for general information only.

This package is manufactured for additional Rad tolerant capabilities; contact the vendor for specific information.

FIGURE 1. Case outline – Continued.

Case 7

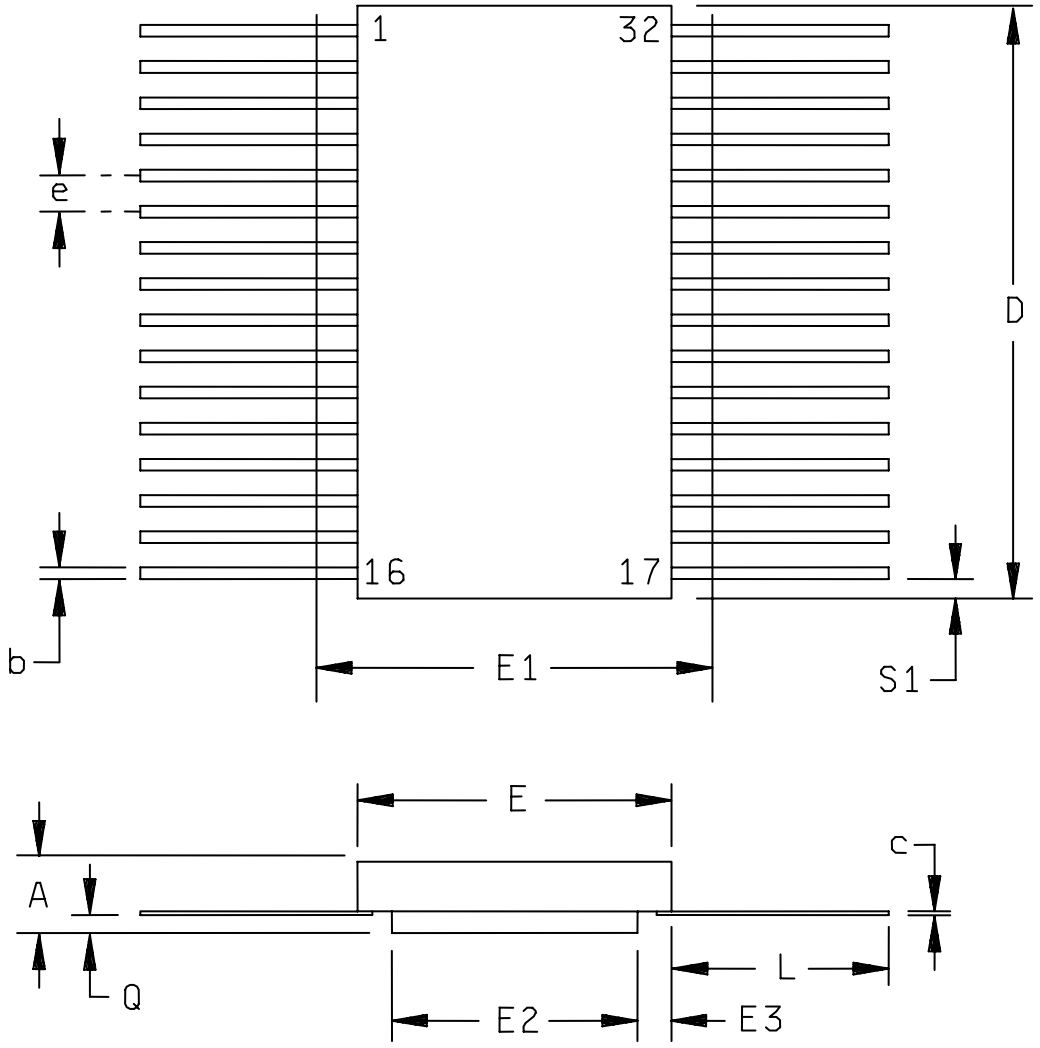


FIGURE 1. Case outline – Continued.

Case 7

Variations				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.97	3.63	.117	.143
b	.38	0.56	.015	.022
c	0.08	0.23	.003	.009
D		21.08		.830
E	10.26	10.57	.404	.416
E1		11.18		.440
E2	5.94		.234	
E3	0.76		.030	
e	1.27		.050 BSC	
S1	0.13		.005	
L	8.89	10.41	.350	.410
Q	0.53	0.91	.021	.036
N	32			

NOTE: Although dimensions are in inches, the US government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the two, the inch-pound units shall take precedence. Metric equivalents are for general information only.

This package is manufactured for additional Rad tolerant capabilities; contact the vendor for specific information.

FIGURE 1. Case outline – Continued.

Device types	01 – 15				16 – 19	
Case outlines	X, Z, U	Y	W	T	U	M, N,6,7
Terminal number	Terminal symbol					
1	NC	NC	NC	A14	RDY/$\overline{\text{BUSY}}$	RDY/$\overline{\text{BUSY}}$
2	A16	NC	NC	A12	A16	A16
3	A15	NC	NC	A7	A14	A14
4	A12	NC	A16	A6	A12	A12
5	A7	A16	A15	A5	A7	A7
6	A6	A15	A12	A4	A6	A6
7	A5	A12	A7	A3	A5	A5
8	A4	A7	A6	A2	A4	A4
9	A3	A6	A5	A1	A3	A3
10	A2	A5	A4	A0	A2	A2
11	A1	NC	A3	I/O0	A1	A1
12	A0	NC	A2	I/O1	A0	A0
13	I/O0	NC	A1	I/O2	I/O0	I/O0
14	I/O1	A4	A0	VSS	I/O1	I/O1
15	I/O2	A3	I/O0	I/O3	I/O2	I/O2
16	VSS	A2	I/O1	I/O4	VSS	VSS
17	I/O3	A1	I/O2	I/O5	I/O3	I/O3
18	I/O4	A0	VSS	I/O6	I/O4	I/O4
19	I/O5	I/O0	I/O3	I/$\overline{\text{O7}}$	I/O5	I/O5
20	I/O6	I/O1	I/O4	$\overline{\text{CE}}$	I/O6	I/O6
21	I/$\overline{\text{O7}}$	I/O2	I/O5	A10	I/$\overline{\text{O7}}$	I/$\overline{\text{O7}}$
22	$\overline{\text{CE}}$	VSS	I/O6	$\overline{\text{OE}}$	$\overline{\text{CE}}$	$\overline{\text{CE}}$
23	A10	NC	I/$\overline{\text{O7}}$	A11	A10	A10
24	$\overline{\text{OE}}$	I/O3	$\overline{\text{CE}}$	A9	$\overline{\text{OE}}$	$\overline{\text{OE}}$
25	A11	I/O4	A10	A8	A11	A11
26	A9	I/O5	$\overline{\text{OE}}$	A13	A9	A9
27	A8	I/O6	A11	$\overline{\text{WE}}$	A8	A8
28	A13	I/$\overline{\text{O7}}$	A9	VCC	A13	A13
29	A14	$\overline{\text{CE}}$	A8	A15	$\overline{\text{WE}}$	$\overline{\text{WE}}$
30	NC	A10	A13	A16	RES	RES
31	$\overline{\text{WE}}$	$\overline{\text{OE}}$	A14	---	A15	A15
32	VCC	NC	NC	---	VCC	VCC
33	---	NC	NC	---	---	---
34	---	NC	NC	---	---	---
35	---	NC	$\overline{\text{WE}}$	---	---	---
36	---	A11	VCC	---	---	---
37	---	A9	---	---	---	---
38	---	A8	---	---	---	---
39	---	A13	---	---	---	---
40	---	A14	---	---	---	---
41	---	NC	---	---	---	---
42	---	NC	---	---	---	---
43	---	$\overline{\text{WE}}$	---	---	---	---
44	---	VCC	---	---	---	---

NC = no connection

FIGURE 2. Terminal connections.

Device types 01-15

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby	V_{IH}	X	X	High Z
Write inhibit	X	X	V_{IH}	D_{OUT} or High Z
Write inhibit	V_{IH}	X	X	High Z
Write inhibit	X	V_{IL}	X	D_{OUT} or High Z
Write inhibit	V_{IL}	V_{IL}	V_{IL}	No operation
Software chip clear	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Software write protect	V_{IL}	V_{IH}	V_{IL}	D_{IN}
High voltage chip clear	V_{IL}	V_H	V_{IL}	V_{IH}

V_{IH} = High logic, "1" state, V_{IL} = Low logic, "0" state.
X = logic "don't care" state, High Z = high impedance state.
V_H = Chip clear voltage, D_{OUT} = Data out, and
D_{IN} = Data in.

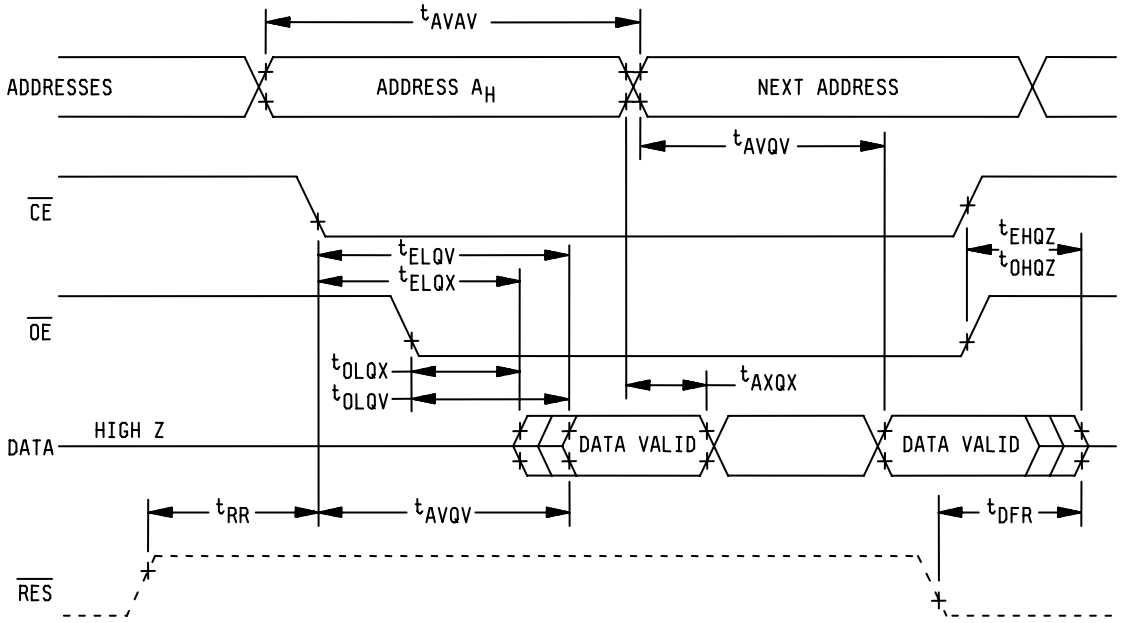
Device types 16-19

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RES}$	RDY/$\overline{BUSY}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_H	High Z	D_{OUT}
Standby	V_{IH}	X	X	X	High Z	High Z
Write	V_{IL}	V_{IH}	V_{IL}	V_H	High Z to V_{OL}	D_{IN}
Deselect	V_{IL}	V_{IH}	V_{IH}	V_H	High Z	High Z
Write inhibit	X	X	V_{IH}	X	---	---
Write inhibit	X	V_{IL}	X	X	---	---
$\overline{DATA}$ polling	V_{IL}	V_{IL}	V_{IH}	V_H	V_{OL}	D_{OUT} (I/O7)
Program reset	X	X	X	V_{IL}	High Z	High Z

V_{IH} = High logic, "1" state, V_{IL} = Low logic, "0" state.
X = logic "don't care" state, High Z = high impedance state.
D_{IN} = Data in, D_{OUT} = Data out, and V_H = V_{CC}-0.5 V to V_{CC}+1.0 V.

FIGURE 3. Truth table.

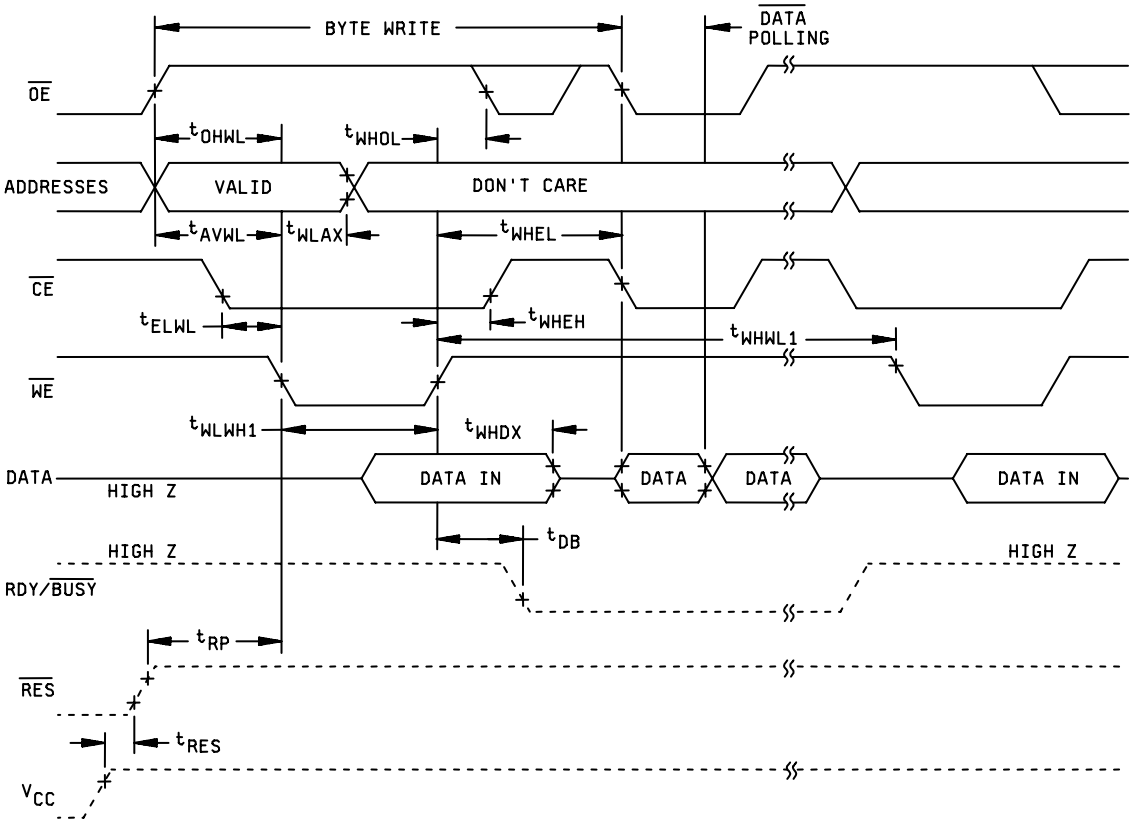
READ MODE WAVEFORM



NOTE: $\overline{RES}$ waveform is applicable to device types 16-19 only.

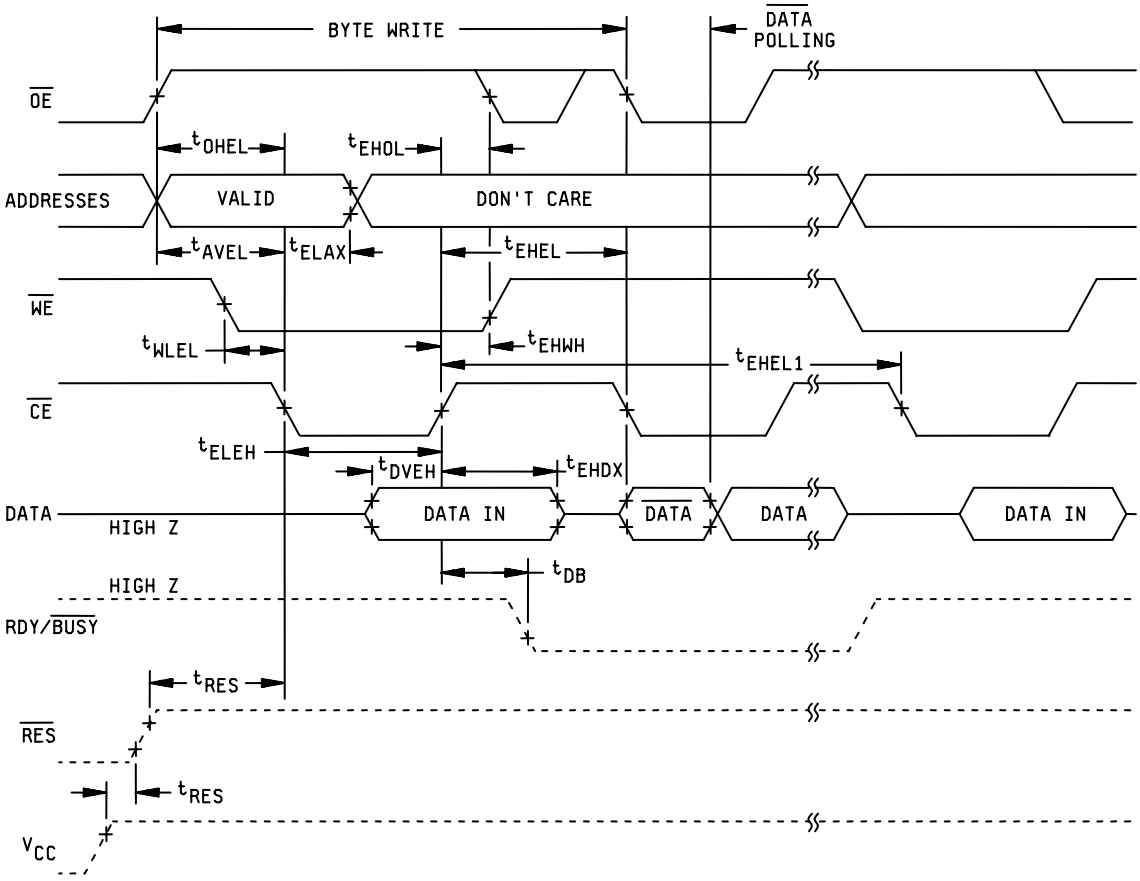
FIGURE 4. Waveforms.

$\overline{WE}$ CONTROLLED BYTE WRITE WAVEFORMS



NOTE: RDY/$\overline{BUSY}$, $\overline{RES}$, and V_{CC} waveforms are applicable to device types 16-19 only.

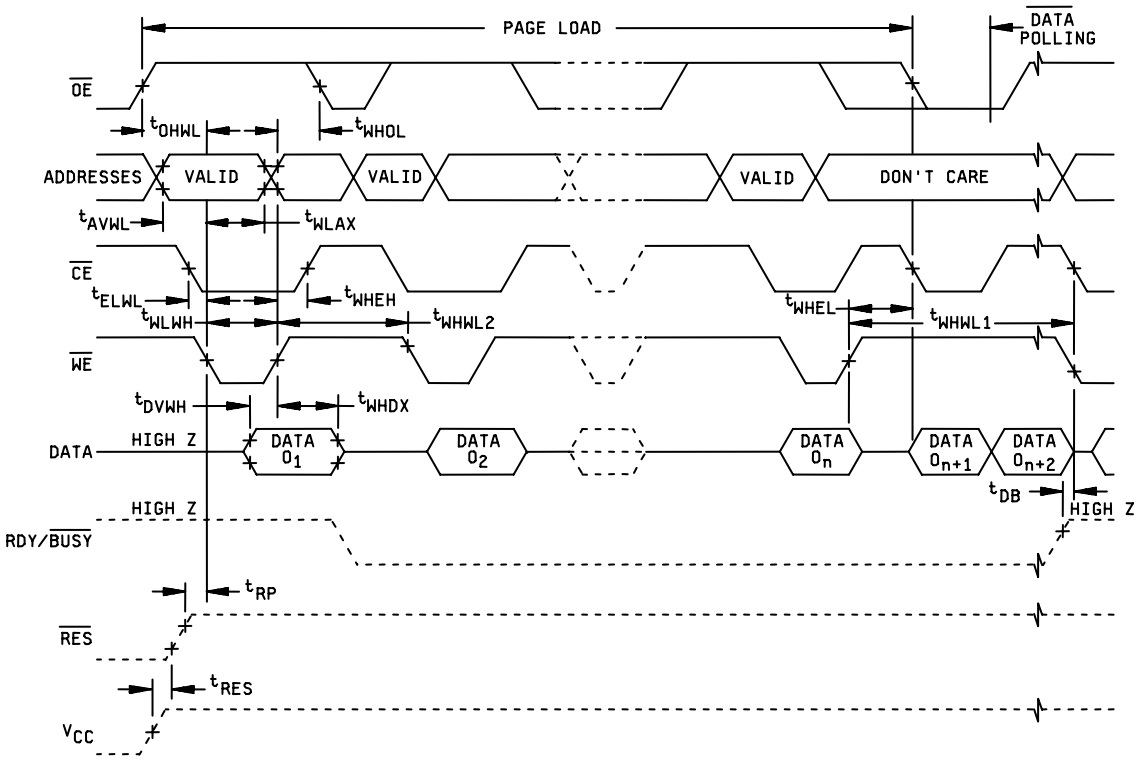
$\overline{CE}$ CONTROLLED BYTE WRITE WAVEFORMS



NOTE: RDY/$\overline{BUSY}$, $\overline{RES}$, and V_{CC} waveforms are applicable to device types 16-19 only.

FIGURE 4. Waveforms - Continued.

PAGE WRITE MODE CYCLE WAVEFORMS



NOTE: RDY/$\overline{\text{BUSY}}$, $\overline{\text{RES}}$, and V_{CC} waveforms are applicable to device types 16-19 only.

FIGURE 4. Waveforms - Continued.

CHIP ERASE WAVEFORMS (device types 01 – 15 only)

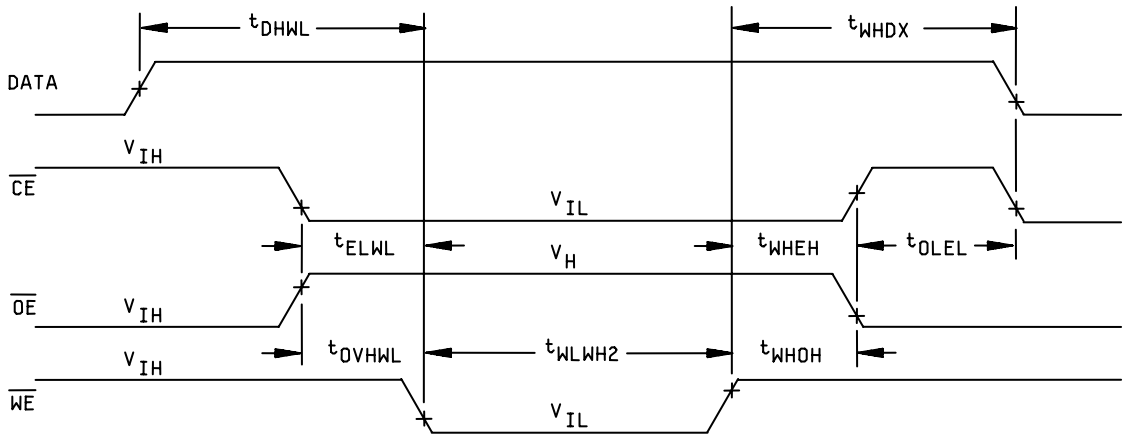
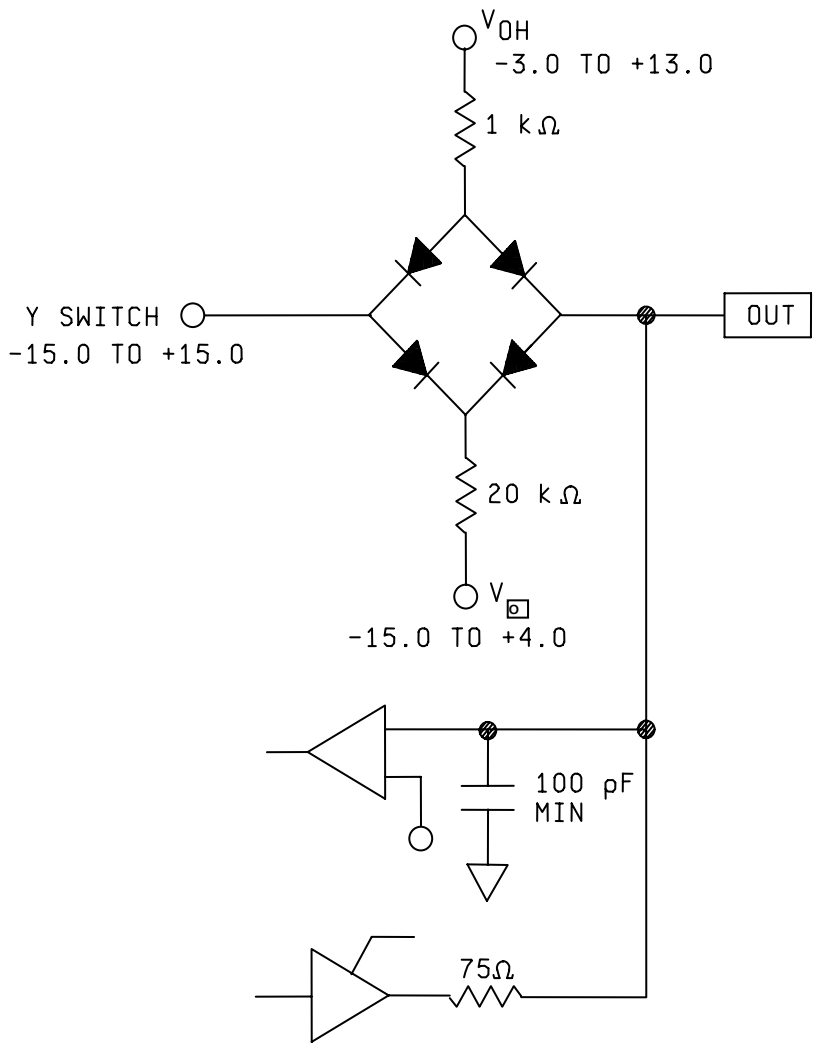


FIGURE 4. Waveforms - Continued.



NOTES:
1. V_{OH} and V_{OL} will be adjusted to meet load conditions of table I.
2. Use this circuit or equivalent circuit.

FIGURE 5. Switching load circuit.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1, 7, 9 or 2, 8A, 10	1, 7, 9 or 1, 2, 8A, 10
2	Static burn-in (method 1015)	Not required	Not required	Required
3	Same as line 1			1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*, 7* Δ
6	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	1*, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	2, 3, 7, 8A, 8B	2, 3, 7, 8A, 8B
10	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1c.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1e.

TABLE IIB. Delta limits at +25°C.

Test 1/	All device types
I_{CC3} standby	± 10% of specified value in table I
I_{IH}, I_{IL}	± 10% of specified value in table I
I_{OHZ}, I_{OLZ}	± 10% of specified value in table I

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta Δ.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. Prior to burn-in, the devices shall be programmed (see 4.5.2 herein) with a checkerboard pattern or equivalent (manufacturers at their option may employ an equivalent pattern provided it is a topologically true alternating bit pattern). The pattern shall be read before and after burn-in. Devices having bits not in the proper state after burn-in shall constitute a device failure and shall be included in the PDA calculation and shall be removed from the lot.

c. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(1) Dynamic burn-in (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1c herein).

d. Interim and final electrical parameters shall be as specified in table IIA herein.

e. After the completion of all screening, the device shall be erased and verified prior to delivery.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device, these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

e. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard EIA/JESD78 may be used for reference.

f. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified, (except devices submitted for groups C and D testing).

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply to group C and shall consist of tests specified in table IIB herein.

4.4.2.1 Additional criteria for device class M.

a. Steady-state life test conditions, method 1005 of MIL-STD-883:

(1) The device selected for testing shall be programmed with a checkerboard pattern. After completion of all testing, the devices shall be erased and verified (except devices submitted for group D testing).

(2) Test condition D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005.

(3) T_A = +125°C, minimum.

(4) Test duration: 1,000 hours, except as specified in method 1005 of MIL-STD-883.

b. All devices requiring end-point electrical testing shall be programmed with a checkerboard or equivalent alternating bit pattern.

c. After the completion of all testing, the devices shall be cleared and verified prior to delivery.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein. The devices selected for testing shall be programmed with a checkerboard pattern. After completion of all testing, the devices shall be erased and verified.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25ºC ±5ºC, after exposure, to the subgroups specified in table IIA herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate figures and tables herein.

4.5.1 Erasing procedures. The erasing procedures shall be as specified by the device manufacturer and shall be available upon request.

4.5.2 Programming procedure. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

4.5.3 Software data protect procedures. The software data protect procedures shall be as specified by the device manufacturer and shall be made available upon request.

4.6 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

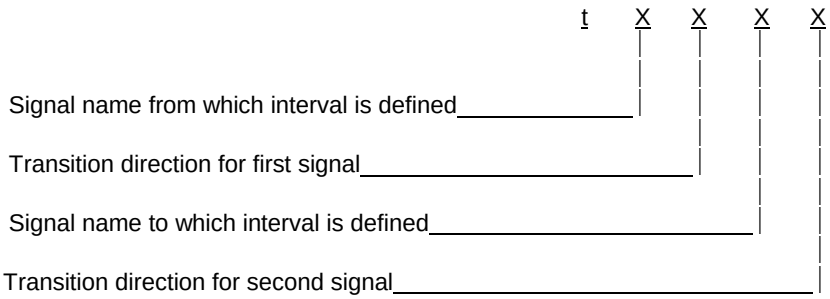
6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331, and as follows:

C_{IN}, C_{OUT} ..... Input and bidirectional output, terminal-to-GND capacitance.
GND ..... Ground zero voltage potential.
I_{CC} ..... Supply current.
I_{IL} ..... Input current low.
I_{IH} ..... Input current high.
T_C ..... Case temperature.
T_A ..... Ambient temperature.
V_{CC} ..... Positive supply voltage.
V_H ..... Output enable and Write enable voltage during chip erase.
O/V ..... Latchup over-voltage.

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.2 Timing parameter abbreviations. All timing abbreviations use lower case characters with upper case subscripts. The initial character is always "t" and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal specify the signal name and the signal transition. Thus the format is:



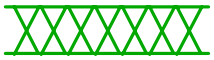
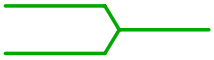
a. Signal definitions:

A = Address
D = Data in
Q = Data out
W = Write enable
E = Chip enable
G = Output enable

b. Transition definitions:

H = Transition to high
L = Transition to low
V = Transition to valid
X = Transition to invalid or don't care
Z = Transition to off (high impedance)

6.5.3 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 06-05-15

Approved sources of supply for SMD 5962-38267 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-3826701MXA	1FN41 34371 3/ 3/	AT28C010-25DM/883 28C010 X28C010DMB-25 CM28C010-250
5962-3826701MYA	1FN41 3/	AT28C010-25LM/883 LM28C010-250
5962-3826701MZA 5962-3826701MZC	1FN41 3/ 3/	AT28C010-25FM/883 X28C010FMB-25 FM28C010-250
5962-3826701MTA	1FN41	AT28C010-25UM/883
5962-3826701MUA	1FN41	AT28C010-25EM/883
5962-3826701MWC	3/ 3/	X28C010KMB-25 TM28C010-250
5962-3826702MXA	3/	CM28C010H-250
5962-3826702MYA	3/	LM28C010H-250
5962-3826702MZA	3/	FM28C010H-250
5962-3826702MWA	3/	TM28C010H-250
5962-3826703MXA	1FN41 3/ 3/	AT28C010-20DM/883 X28C010DMB-20 CM28C010-200
5962-3826703MYA	1FN41 3/	AT28C010-20LM/883 LM28C010-200
5962-3826703MZA 5962-3826703MZC	1FN41 3/ 3/	AT28C010-20FM/883 X28C010FMB-20 FM28C010-200
5962-3826703MTA	1FN41	AT28C010-20UM/883
5962-3826703MUA	1FN41	AT28C010-20EM/883
5962-3826703MWC	3/ 3/	X28C010KMB-20 TM28C010-200
5962-3826704MXA	3/	CM28C010H-200
5962-3826704MYA	3/	LM28C010H-200
5962-3826704MZA	3/	FM28C010H-200
5962-3826704MWA	3/	TM28C010H-200

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-3826705MXA	1FN41 34371 3/ 3/	AT28C010-15DM/883 28C010 X28C010DMB-15 CM28C010-150
5962-3826705MYA	1FN41 3/	AT28C010-15LM/883 LM28C010-150
5962-3826705MZA 5962-3826705MZC	1FN41 3/ 3/	AT28C010-15FM/883 X28C010FMB-15 FM28C010-150
5962-3826705MTA	1FN41	AT28C010-15UM/883
5962-3826705MUA	1FN41	AT28C010-15EM/883
5962-3826705WC	3/ 3/	X28C010KMB-15 TM28C010-150
5962-3826706MXA	3/	CM28C010H-150
5962-3826706MYA	3/	LM28C010H-150
5962-3826706MZA	3/	FM28C010H-150
5962-3826706MWA	3/	TM28C010H-150
5962-3826707MXA	1FN41 34371 3/ 3/	AT28C010-12DM/883 28C010 X28C010DMB-12 CM28C010-120
5962-3826707MYA	1FN41 3/	AT28C010-12LM/883 LM28C010-120
5962-3826707MZA 5962-3826707MZC	1FN41 3/ 3/	AT28C010-12FM/883 X28C010FMB-12 FM28C010-120
5962-3826707MTA	1FN41	AT28C010-12UM/883
5962-3826707MUA	1FN41	AT28C010-12EM/883
5962-3826707MWC	3/ 3/	X28C010KMB-12 TM28C010-120
5962-3826716QUA	0EU86	AS58C1001ECA-25/883C
5962-3826716QMA	0EU86	AS58C1001F-25/883C
5962-3826716QMC	68911	28C010TFB-25
5962-3826716VMC	68911	28C010TFS-25
5962-3826716QNA	0EU86	AS58C1001SF-25/883C
5962-3826716Q6C	68911	28C010TRPFB-25
5962-3826716V6C	68911	28C010TRPFS-25
5962-3826716Q7C	68911	28C011TRPFB-25
5962-3826716V7C	68911	28C011TRPFS-25

See footnotes at end of table.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-3826717QUA	0EU86	AS58C1001ECA-20/883C
5962-3826717QMA	0EU86	AS58C1001F-20/883C
5962-3826717QMC	68911	28C010TFB-20
5962-3826717VMC	68911	28C010TFS-20
5962-3826717QNA	0EU86	AS58C1001SF-20/883C
5962-3826717Q6C	68911	28C010TRPFB-20
5962-3826717V6C	68911	28C010TRPFS-20
5962-3826717Q7C	68911	28C011TRPFB-20
5962-3826717V7C	68911	28C011TRPFS-20
5962-3826718QUA	0EU86	AS58C1001ECA-15/883C
5962-3826718QMA	0EU86	AS58C1001F-15/883C
5962-3826718QMC	68911	28C010TFB-15
5962-3826718VMC	68911	28C010TFS-15
5962-3826718QNA	0EU86	AS58C1001SF-15/883C
5962-3826718Q6C	68911	28C010TRPFB-15
5962-3826718V6C	68911	28C010TRPFS-15
5962-3826718Q7C	68911	28C011TRPFB-15
5962-3826718V7C	68911	28C011TRPFS-15
5962-3826719QMC	68911	28C010TFB-12
5962-3826719VMC	68911	28C010TFS-12
5962-3826719Q6C	68911	28C010TRPFB-12
5962-3826719V6C	68911	28C010TRPFS-12
5962-3826719Q7C	68911	28C011TRPFB-12
5962-3826719V7C	68911	28C011TRPFS-12

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
1FN41	Atmel Corporation 2125 O'Nel Drive San Jose, CA 95131
34371	Intersil Corporation 1001 Murphy Ranch Road Milpitas, CA 95035 - 5680
0EU86	Austin Semiconductor 8701 Cross Park Drive Austin, TX 78754-4566
68911	Maxwell Technologies 9244 Balboa Avenue San Diego, CA 92123