Switching from the *Ambassador*® T8100 to the T8100A/02/05 H.100/H.110 Interface and Time-Slot Interchangers

Introduction

This advisory will assist T8100 customers in their switch to a T8100A/02/05 design. Switching to the T8100A/02/05 involves two pin changes and may involve register programming changes.

It may be of interest to note that the T8100A/02/05 is available in a 217-ball PBGA package, as well as the 208-pin SQFP. The T8100 is available in the 208-pin SQFP package.

Functional Changes

The T8100A/02/05 functions the same way as the T8100, with the following exceptions:

1. The bit slider runs in the opposite direction on the T8100A/02/05.
   — T8100 reduces the frame size by 1 clock cycle/frame.
   — T8100A/02/05 increases the frame size by 1 clock cycle/frame.
   — The direction of the slide may make a difference when a T8100 and a T8100A/02/05 interface to the same H.100/H.110 bus.
2. The frame center sampling is determined by the recovered clock in the T8100A/02/05. The T8100 used the incoming clock to determine the frame center.

Pin Changes

1. CT_NETREF2 was added to T8100A/02/05. CT_NETREF2 was a V_{SS} pin on T8100.
2. LPUE was added to T8100A/02/05. LPUE was a no connect (NC) on T8100.

If a T8100A/02/05 part is placed on an existing T8100 layout, CT_NETREF2 will be grounded, but this should not pose a problem since the driver is 3-stated when not used. LPUE was an NC, so users should tie LPUE to /RESET or equivalent if used in a hot-swap application. If not used, LPUE should be left unconnected.

Register Issues to Consider

1. The biggest issue is CKN because the function of bits 6 and 7 changes and, unfortunately, it's not backward compatible. The table below describes the changes.

CKN Register Bits 7:6	T8100 Function	T8100A/02/05 Function
00	Output disabled	Outputs disabled, NRSEL-mux routed to LSCs.
01	Output disabled	NETREF2-out enabled. NETREF1-in routed to LSCs.
10	Output enabled	NETREF1-out enabled. NETREF2-in routed to LSCs.
11	Invalid, equivalent to 01	Both outputs enabled, NETREF divider-out routed to LSCs.

2. NRSEL in the T8100A/02/05 uses up two of the reserved definitions from the T8100, but this should not be a problem.
3. FCSEL in the T8100A/02/05 is redefined with "001" selecting "NETREF2"; it selected internal oscillator in the T8100. ("100" selects "NETREF1" where it is defined as just "NETREF" in the T8100.)
4. If CKSEL in CKM is set to "0001" (NETREF), then the CON register must be set properly to choose between NETREF1 and NETREF2. CON defaults correctly if the reserved bits are set low.
5. CKP register bit 0 is reserved in the T8100, but becomes the FR_COMP width bit in the T8100A/02/05.
6. The T8100A/02/05 also have the following new control registers to be aware of:
   — 0x17—GPD, the direction control for GPIO which is enabled through CON.
   — 0x2C—CLKERR3 for the two NETREFs.
   — 0xFE—Device ID.
   — 0xFF—GMODE, device mode control.

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Ambassador™ T8100
H.100/H.110 Interface and Time-Slot Interchanger

This advisory details two changes to the Ambassador™ *T8100 H.100/H.110 Interface and Time-Slot Interchanger* Preliminary Data Sheet: DS98-195NTNB.

Change Affecting Page 15, Section 2.1.3 Address Mode Register

Problem: There is a minor bug in the T8100. If a write is issued to the address mode register (AMR) address 0x70 (local bus, holding registers, and reset), the T8100's RDY line gets stuck low (not ready state).

Workaround: To solve this, issue another write command to any of the four direct registers (MCR, LAR, AMR, or IDR) and the RDY signal will reset.

Change Affecting Page 38, Section 2.4.2 Dividers and Rate Multipliers

There is an anomaly in the digital phase-lock loop (DPLL) performance of the device. The behavior affects all versions of the T8100 but has been corrected in the T8100A, T8102, and T8105. This anomaly affects applications that use the DPLL for CT bus clock generation.

When used for clocking, the DPLL uses the 16.384 MHz internal oscillator to rate multiply an 8 kHz input signal. In order for the DPLL to lock to the 8.000000 kHz signal, the required internal oscillator frequency range should be centered at 16.388 MHz. A frequency of 16.384 MHz is too low for the DPLL to perform properly.

If this crystal adaptation is used for the DPLL, there are several limitations. First, do not select the crystal as a fallback clock source. When the crystal is a clock source, the generated clocks are all multiples of the crystal. In that case, they will be offset by the same ratio as the crystal. Second, do not use TCLKOUT. It is also derived from the crystal and will be offset by the same ratio. Third, the watchdogs will be slightly more sensitive due to the increased clock frequency. In designs affected by these limitations, conversion to the T8100A is recommended.

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Bell Labs Innovations

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Ambassador™ T8100
H.100/H.110 Interface and Time-Slot Interchanger

1 Product Overview

1.1 Introduction

Increasingly, enhanced telephony services are provided by equipment based on mass-market computer-telephony architectures. The H.100 time-division multiplexed (TDM) bus has emerged as the industry standard used in these systems. The *Ambassador* T8100 is a single device that provides a complete interface for H.100/H.110-based systems.

The T8100 will support the newer bus standards, H-*MVIP** and ECTF H.100, but remain downward compatible with *MVIP*-90 and *Dialogic*'s† SC-Bus. Data can be buffered in either minimum delay or constant delay modes on a connection-by-connection basis.

The T8100 will take advantage of new technology: it is based on 0.35 micron feature sizes and a robust standard-cell library. It utilizes associative memory (content addressable memories [CAM]) in addition to traditional static RAM and register file structures for the connection and data memories. The T8100 operates on a single 3.3 V supply, but all inputs are 5 V tolerant and standard TTL output levels are maintained.

1.2 Features

- Complete solution for interfacing board-level circuitry to the H.100 telephony bus
- H.100 compliant interface; all mandatory signals
- Programmable connections to any of the 4096 time slots on the H.100 bus
- Up to 16 local serial inputs and 16 local serial outputs, programmable for 2.048 Mbits/s, 4.096 Mbits/s, and 8.192 Mbits/s operation per CHI specifications
- Programmable switching between local time slots, up to 1024 connections
- Programmable switching between local time slots and H.100 bus, up to 256 connections
- Choice of frame integrity or minimum latency switching on a per-time-slot basis
  — Frame integrity to ensure proper switching of wideband data
  — Minimum latency switching to reduce delay in voice channels
- On-chip phase-locked loop (PLL) for H.100, *MVIP*, or SC-Bus clock operation in master or slave clock modes
- Serial TDM bus rate and format conversion between most standard buses
- Optional 8-bit parallel input and/or 8-bit parallel output for local TDM interfaces
- High-performance microprocessor interface
  — Provides access to device configuration registers and to time-slot data
  — Supports both *Motorola*‡ nonmultiplexed and *Intel*§ multiplexed/nonmultiplexed modes
- Two independently programmable groups of up to 12 framing signals each
- 3.3 V supply with 5 V tolerant inputs and TTL-compatible outputs
- Boundary-scan testing support
- 208-pin, plastic SQFP package
- 217-pin BGA package (industrial temperature range)

* *MVIP* is a registered trademark of GO-MVIP, Inc.
† *Dialogic* is a registered trademark of Dialogic Corporation.
‡ *Motorola* is a registered trademark of Motorola, Inc.
§ *Intel* is a registered trademark of Intel Corporation.

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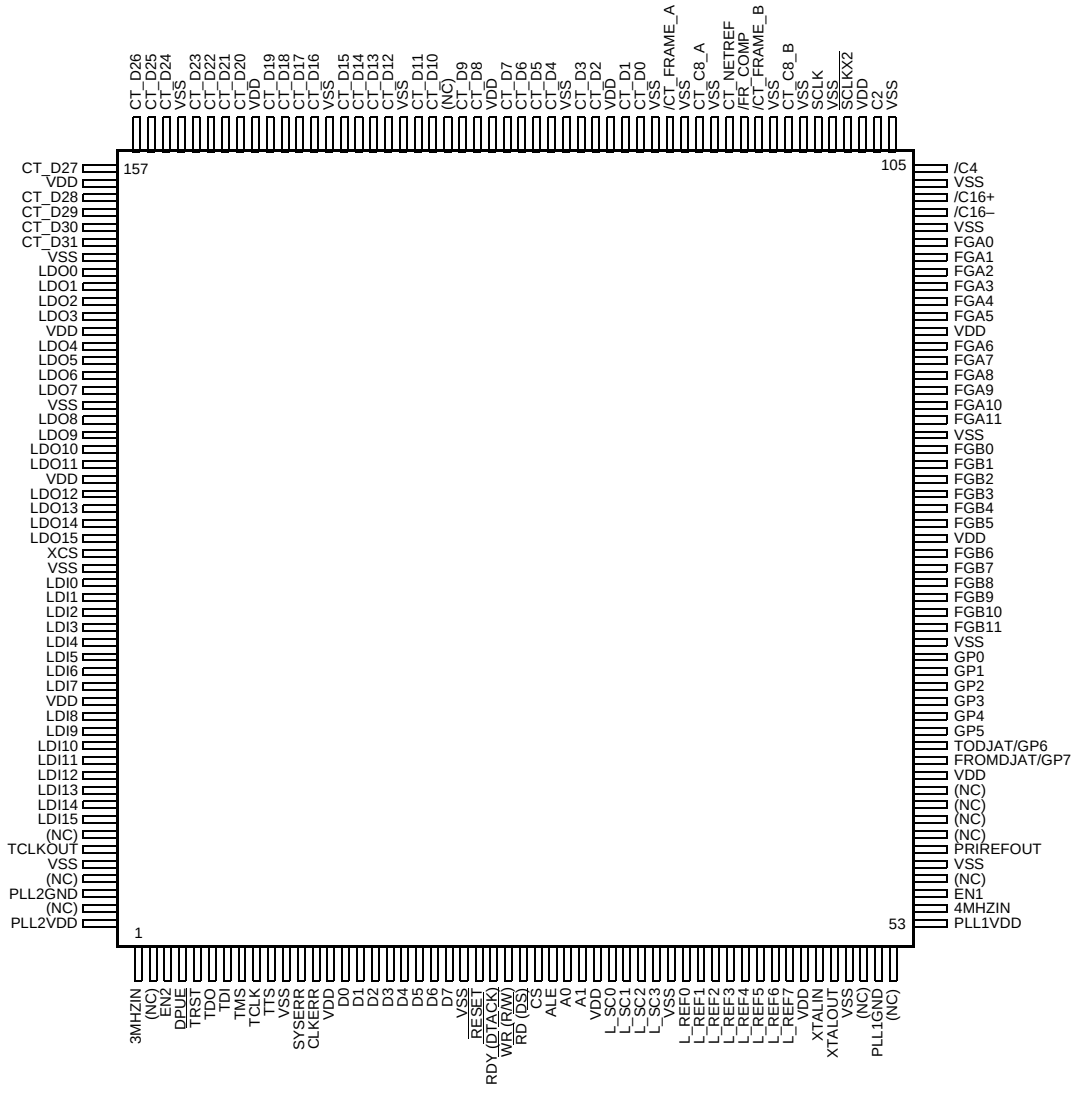

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Figure 1. Pin Diagram

1 Product Overview (continued)

1.3 Pin Information (continued)

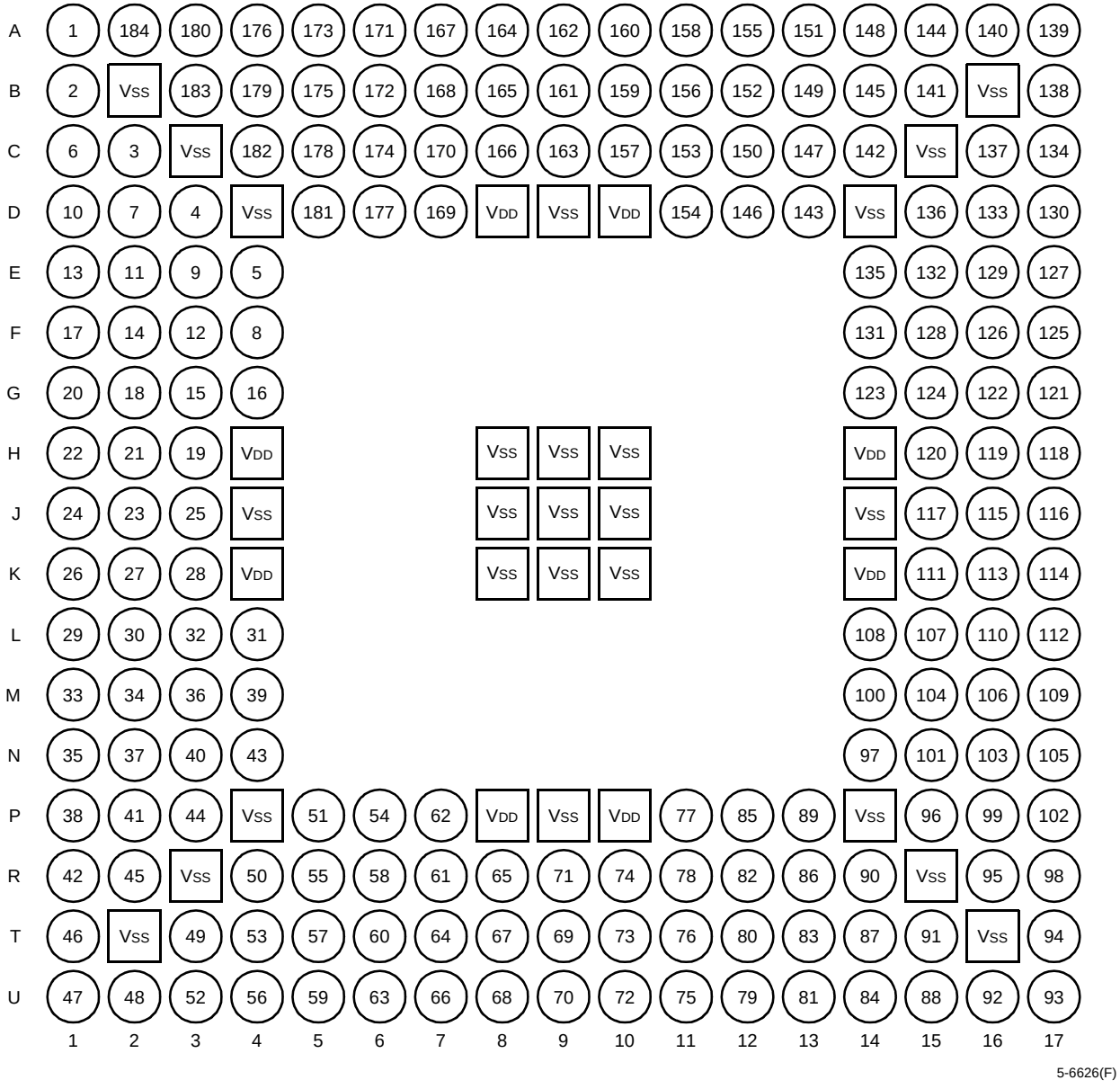

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Figure 2. 217 PBGA—Top View

Table 1. Pin Descriptions: Clocking and Framing Pins

Symbol	Pin	Ball	Type	Name/Description
L_REF[7:0]	45—38	P3, N4, R1, P2, N3, M4, P1, N2	I	**Local Frame Reference Inputs.** 50 kΩ internal pull-up.
/C16+ /C16–	102 101	R14 P13	I/O	**H-*MVIP* 16.384 MHz Clock Signals.** Differential 24 mA drive, Schmitt in, 50 kΩ internal pull-up.

1 Product Overview (continued)

1.3 Pin Information (continued)

Table 1. Pin Descriptions: Clocking and Framing Pins (continued)

Symbol	Pin	Ball	Type	Name/Description
/C4	104	U16	I/O	***MVIP* 4.096 MHz Clock.** 8 mA drive, Schmitt in, 50 kΩ internal pull-up.
C2	106	T17	I/O	***MVIP* 2.048 MHz Clock.** 8 mA drive, Schmitt in, 50 kΩ internal pull-up.
SCLK	110	R17	I/O	**SC-Bus 2/4/8 MHz Clock.** 24 mA drive, Schmitt in, 50 kΩ internal pull-up.
$\overline{\text{SCLKX2}}$	108	P15	I/O	**SC-Bus Inverted 4/8 MHz Clock (Active-Low).** 24 mA drive, Schmitt in, 50 kΩ internal pull-up.
L_SC[3:0]	36—33	M3, N1, M2, M1	O	**Local Selected Clocks.** 1.024 MHz, 2.048 MHz, 4.096 MHz, 8.192 MHz, 16.384 MHz, frame (8 kHz), or secondary (NETREF). 8 mA drive, 3-state.
FGA[5:0]	94—99	R12, T13, U14, P12, R13, T14	O	**Frame Group A.** 8 mA drive, 3-state.
FGA[11:6]	87—92	T11, P11, R11, U12, T12, U13		
FGB[5:0]	80—85	U9, R9, U10, T10, R10, U11	O	**Frame Group B.** 8 mA drive, 3-state.
FGB[11:6]	73—78	U6, T7, R8, U7, T8, U8		
PRIREFOUT	58	P5	O	**Output from Primary Clock Selector/Divider.** 8 mA drive.
PLL1V_{DD}	53	U1	—	**PLL #1 VCO Power.** This pin must be connected to power, even if PLL #1 is not used.
PLL1GND	51	No ball for this signal, internally connected.	—	**PLL #1 VCO Ground.** This pin must be connected to ground, even if PLL #1 is not used.
EN1	55	T3	I	**PLL #1 Enable.** Requires cap to V_{SS} to form power-on reset, or may be driven with $\overline{\text{RESET}}$ line. 50 kΩ internal pull-up.
4MHZIN	54	U2	I	**PLL #1 Rate Multiplier.** Can be 2.048 MHz or 4.096 MHz. 50 kΩ internal pull-up.
PLL2V_{DD}	208	A2	—	**PLL #2 VCO Power.** This pin must be connected to power if PLL #2 is not used and 3MHZIN is used. Can be left floating only if both PLL #2 and 3MHZIN are not used.
PLL2GND	206	No ball for this signal, internally connected.	—	**PLL #2 VCO Ground.** This pin must be connected to ground if PLL #2 is not used and 3MHZIN is used. Can be left floating only if both PLL #2 and 3MHZIN are not used.
EN2	3	C2	I	**PLL #2 Enable.** Requires cap to V_{SS} to form power-on reset, or may be driven with $\overline{\text{RESET}}$ line. 50 kΩ internal pull-up.
3MHZIN	1	A1	I	**PLL #2 Rate Multiplier.** Input, 50 kΩ internal pull-up.
XTALIN	47	R2	I	**16.384 MHz Crystal Connection or External Clock Input.**
XTALOUT	48	T1	O	**16.384 MHz Crystal, Feedback Connection.**
TCLKOUT	203	C4	O	Selected output to drive framers. 8 mA drive, 3-state.

1 Product Overview (continued)

1.3 Pin Information (continued)

Table 2. Pin Descriptions: Local Streams Pins

Symbol	Pin	Ball	Type	Name/Description
LDI[15:8] LDI[7:0]	201—194 192—185	A3, B4, C5, D6, A4, B5, C6, A5 B6, A6, C7, D7, B7, A7, C8, B8	I	**Local Data Input Streams.** 50 kΩ internal pull-up.
LDO[15:12] LDO[11:8] LDO[7:4] LDO[3:0]	182—179 177—174 172—169 167—164	C9, A9, B9, A10 B10, A11, C10, B11 D11, C11, B12, A13 B13, A14, C13, D12	O	**Local Data Output Streams.** 8 mA drive, 3-state.

Table 3. Pin Descriptions: H-Bus Pins

Symbol	Pin	Ball	Type	Name/Description
CT_D[31:28] CT_D[27:24] CT_D[23:20] CT_D[19:16] CT_D[15:12] CT_D[11:10] CT_D[9:8] CT_D[7:4] CT_D[3:2] CT_D[1:0]	162—159 157—154 152—149 147—144 142—139 137—136 134—133 131—128 126—125 123—122	A15, D13, C14, B15 A17, C16, D15, E14 C17, D16, E15, F14 D17, E16, F15, E17 F16, F17, G15, G14 G16, G17 H15, H16 H17, J15, J17, J16 K17, K16 L17, K15	I/O	**H-Bus, Data Lines.** Variable rate 2 Mbits/s, 4 Mbits/s, 8 Mbits/s. 5 V tolerant, PCI compliant, 50 kΩ internal pull-up. To conform to H.100, connect an external 24 Ω series, 1/8 W resistor between each pin and the bus. Also, data lines 16—31 should be programmed to 8 Mbits/s.
/CT_FRAME_A	120	L14	I/O	**H-Bus, 8 kHz, Frame.** 5 V tolerant, PCI compliant, 24 mA drive, Schmitt in. No pull-up.
/CT_FRAME_B	114	P17	I/O	**H-Bus, Alternate 8 kHz Frame.** 5 V tolerant, PCI compliant, 24 mA drive. Schmitt in. No pull-up.
/FR_COMP	115	M15	I/O	**H-Bus, Compatibility Frame Signal.** 24 mA drive, Schmitt in, 50 kΩ internal pull-up.
CT_NETREF	116	N17	I/O	**H-Bus, Network Reference.** 8 kHz, 2.048 MHz, or 1.544 MHz. 8 mA drive, slew rate limited, Schmitt in. Not internally pulled up.
CT_C8_A	118	M16	I/O	**H-Bus, Main Clock.** 5 V tolerant, PCI compliant, 24 mA drive, Schmitt in. No pull-up.
CT_C8_B	112	M14	I/O	**H-Bus, Alternate Main Clock.** 5 V tolerant, PCI compliant, 24 mA drive, Schmitt in. No pull-up.
DPUE	4	D3	I	**Data Pull-Up Enable.** High enables pull-ups on CT_Dxx only for H.100, low disables for H.110. 50 kΩ internal pull-up.

1 Product Overview (continued)

1.3 Pin Information (continued)

Table 4. Pin Descriptions: Microprocessor Interface Pins

Symbol	Pin	Ball	Type	Name/Description
$\overline{\text{RESET}}$	24	J1	I	**Master Reset (Active-Low).** See Section 3.1 Resets. 50 kΩ internal pull-up.
A[1:0]	31—30	L4, L2	I	**Microprocessor Interface, Address Lines.** Internal 20 kΩ pull-down.
D[7:0]	22—15	H1, H2, G1, H3, G2, F1, G4, G3	I/O	**Microprocessor Interface, Data Lines.** 8 mA drive, 50 kΩ internal pull-up.
ALE	29	L1	I	**Address Latch Enable.** Internal 20 kΩ pull-down.
$\overline{\text{CS}}$	28	K3	I	**Chip Select (Active-Low).** 50 kΩ internal pull-up.
$\overline{\text{RD}}$ ($\overline{\text{DS}}$)	27	K2	I	**Read Strobe (*Intel* Mode [Active-Low]), Data Strobe (*Motorola* [Active-Low]).** 50 kΩ internal pull-up.
$\overline{\text{WR}}$ ($\overline{\text{R/W}}$)	26	K1	I	**Write Strobe (*Intel* [Active-Low]), Read/Write Select (*Motorola* [Active-Low]).** 50 kΩ internal pull-up.
RDY ($\overline{\text{DTACK}}$)	25	J3	O	**Data Ready (*Intel*), Data Transfer (*Motorola* [Active-Low]).** 8 mA, open drain (user should add pull-up to this line).
CLKERR	13	E1	O	**Clock Error.** Logical OR of CLKERR register flags (only). 8 mA drive, 3-state
SYSERR	12	F3	O	**System Error.** Logical OR of all CLKERR and SYSERR register flags. 8 mA drive, 3-state.

Table 5. Pin Descriptions: JTAG Pins

Symbol	Pin	Ball	Type	Name/Description
TCLK	9	E3	I	**JTAG Clock Input.**
TMS	8	F4	I	**JTAG Mode Select.** 50 kΩ internal pull-up.
TDI	7	D2	I	**JTAG Data Input.** 50 kΩ internal pull-up.
TDO	6	C1	O	**JTAG Data Output.** 8 mA drive, 3-state.
$\overline{\text{TRST}}$	5	E4	I	**JTAG Reset (Active-Low).** 50 kΩ internal pull-up.

Table 6. Pin Descriptions: Power Pins

Symbol	Pin	Ball	Type	Name/Description
V_{SS}	11, 23, 37, 49, 57, 72, 86, 100, 103, 105, 109, 111, 113, 117, 119, 121, 127, 138, 143, 153, 163, 173, 184, 204	B2, B16, C3, C15, D4, D9, D14, H8, H9, H10, J4, J8, J9, J10, J14, K8, K9, K10, L15, N14, P4, P9, P14, P16, R3, R15, T2, T15, T16, U15, U17	—	**Chip Ground.**
V_{DD}	14, 32, 46, 63, 79, 93, 107, 124, 132, 148, 158, 168, 178, 193	A16, D8, D10, F2, H4, H14, K4, K14, L16, P8, P10, T9	—	**3.3 V Supply Voltage**.

1 Product Overview (continued)

1.3 Pin Information (continued)

Table 7. Pin Descriptions: Other Pins

Symbol	Pin	Ball	Type	Name/Description
GP[5:0]	66—71	T5, R6, U5, T6, R7, P7	I/O	**General-Purpose Bidirectional Register.** 8 mA drive, Schmitt in, 50 kΩ internal pull-up.
TODJAT/GP6	65	U4	I/O	**Output from Selector to Drive DJAT (for NETREF) or GP Register Bit 6.** 8 mA drive, Schmitt in, 50 kΩ internal pull-up.
FROMDJAT/GP7	64	R5	I/O	**Smoothed Input to NETREF Divider and Drivers or GP Register Bit 7.** 8 mA drive, input, Schmitt in, 50 kΩ internal pull-up.
XCS	183	A8	O	**Serial Output from Connection Memory.** 8 mA drive, 3-state.
TTS	10	D1	I	**Test Type Select.** 0 = JTAG, 1 = forced output test, internal pulldown.
(NC)	2, 50, 52, 56, 59, 60, 61, 62, 135, 202, 205, 207	A12, B1, B3, B14, B17, C12, D5, E2, J2, L3, M17, N15, N16, P6, R4, R16, T4, U3	—	**Reserved, No Connection.**

1.4 Enhanced Local Stream Addressing

Local stream addressing has 1024 locations. Separate connection and data memories maintain all necessary information for local stream interconnections. The streams may operate at maximum rate on eight physical inputs and eight physical outputs. Choices for slower input or output rates allow enabling of additional physical inputs or outputs for a maximum of 16 pins each. Data rates are 2.048 Mbits/s, 4.096 Mbits/s, or 8.192 Mbits/s.

In addition to the enhanced serial streaming, the local memories may be used for 8-line-serial-in/1-byte-parallel-out, 1-byte-parallel-in/8-line-serial-out, or 1-byte-parallel-in/1-byte-parallel-out options. All three data rates are supported in the parallel modes. The addresses for the local memories have been simplified so that stream and time-slot designations are automatically translated to the appropriate memory address, regardless of rate or serial/parallel modes.

1.5 Full H.100 Stream Address Support

The T8100 provides access to the full 4096 H.100 bus slots (32 streams x 128 slots) or any standard subset (H-*MVIP* has a maximum 24 streams x 128 time slots, for example). The number of stored time-slot addresses is limited to 256 at any one time, but these may be updated on the fly. In addition, accesses to and from the H.100 bus can be directed through the 1024 local stream/time slots, giving a total space of 5120 time slots. Data rates are programmable on each of the 32 physical streams, selected in groups of four. The rates are 2.048 Mbits/s, 4.096 Mbits/s, or 8.192 Mbits/s.

1 Product Overview (continued)

1.6 Onboard PLLs and Clock Monitors

The T8100 uses rate multipliers and state machines to generate onboard frequencies for supporting the H.100, H-*MVIP*, *MVIP*, MC-1, and SC-Buses. Pins are provided for coupling the internal clock circuitry with commonly available clock adapters and jitter attenuators. If external resources are not available, an internal digital phase-locked loop (DPLL) can be used to generate all the bus frequencies and remain synchronized to an 8 kHz reference. One of several clock input reference sources may be selected, and separate input-active detection logic can identify the loss of the individual input references. The entire clocking structure operates from a 16.384 MHz crystal or external input.

1.7 Phase Alignment of Referenced and Generated Frames

If this resource is selected, special control logic will create bit-sliding in the data streams when the reference frame and generated frame are out of phase. The bit-sliding refers to removing a fraction of a bit time per frame until the frames are in phase.

1.8 Interfaces

1.8.1 Microprocessors

The T8100 provides the user a choice of either *Motorola* or *Intel* interfacing through an 8-bit data bus, a 2-bit address bus, and multifunction control pins. All access to T8100 memory blocks and registers use indirect addressing.

1.8.2 Framing Groups

Two groups of programmable framing signals are available. Each group is composed of 12 sequenced lines operating in one of four modes. The T8100 supports 1-bit, 2-bit, 1-byte, and 2-byte pulse widths. Starting position of the pulse sequences are also programmable.

1.8.3 General-Purpose Register and I/O

A general-purpose register is provided as either a byte-wide input or byte-wide output through a separate set of pins.

1.9 Applications

- Computer-telephony systems
- Enhanced service platforms
- WAN access devices
- PBXs
- Wireless base stations

1.10 Application Overview

The integration of computers and telecommunications has enabled a wide range of new communications applications and has fueled an enormous growth in communications markets. A key element in the development of computer-based communications equipment has been the addition of an auxiliary telecom bus to existing computer systems. Most manufacturers of high-capacity, computer-based telecommunications equipment have incorporated some such telecom bus in their systems. Typically, these buses and bus interfaces are designed to transport and switch N x 64 kbits/s low-latency telecom traffic between boards within the computer, independent of the computer's I/O and memory buses. At least a half dozen of these PC-based telecom buses emerged in the early 1990s for use within equipment based on ISA/EISA and MCA computers.

With the advent of the H.100 bus specification by the Enterprise Computer Telephony Forum, the computer-telephony industry has agreed on a single telecom bus for use with PCI and compact PCI computers. H.100 facilitates interoperation of components, thus providing maximum flexibility to equipment manufacturers, value-added resellers, system integrators, and others building computer-based telecommunications applications.

2 Architecture and Functional Description

The T8100 is an H.100-compliant device that provides a complete interface between the H.100 bus and a wide variety of telephony interface components, processors, and other circuits. The bus interface provides all signals needed for the H.100 bus, the H-*MVIP* and *MVIP*-90 buses, or the SC-Bus. Local interfaces include 16 serial inputs and 16 serial outputs based on the Lucent Technologies Microelectronics Group concentration highway interface (CHI). Two built-in time-slot interchangers are included. The first provides a local switching domain with up to 1024 programmable connections between time slots on the local CHI inputs and outputs. The second supports up to 256 programmable connections between any time slot on the H.100 bus and any time slot in the local switching domain. The *Ambassador* is configured via a microprocessor interface. This interface can also read and write time slot and device data. Onboard clock circuitry, including a DPLL, supports all H.100 clock modes including *MVIP* and SC-Bus compatibility clocks.
The local CHI interfaces support PCM rates of 2.048 Mbits/s, 4.096 Mbits/s, and 8.192 Mbits/s. The T8100 has internal circuitry to support either minimum latency or multi-time-slot frame integrity. Frame integrity is a requisite feature for applications that switch wide-band data (ISDN H-channels). Minimum latency is advantageous in voice applications.

The T8100 has four major sections:

- Local bus—refers to the local streams.
- H-Bus—refers to the H.100/H.110/H-*MVIP* and legacy streams.
- Interface—refers to the microprocessor interface, frame groups, and general-purpose I/O (GPIO).
- Timing—the rate multipliers, DPLL, and clocking functions.

Figure 3 shows a T8100 block diagram. The T8100 operates on a 3.3 V supply for both the core and I/Os, though the I/Os are TTL compatible and 5 V tolerant.

2 Architecture and Functional Description (continued)

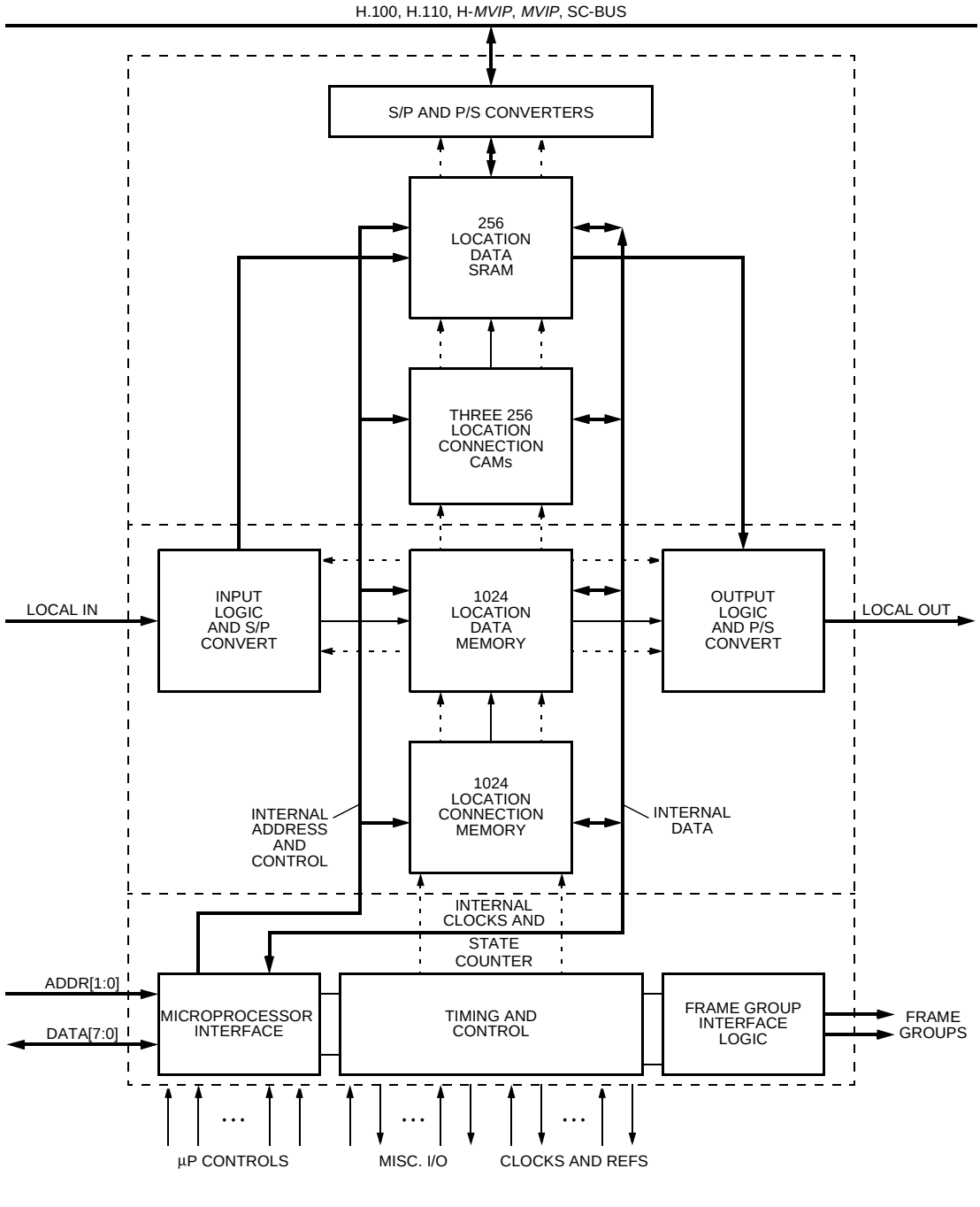


Figure 3. Block Diagram of the T8100

2 Architecture and Functional Description (continued)

2.1 Register/Memory Maps

In this section, a general overview of the registers and the indirect mapping to different memory spaces is described. More detailed descriptions for using the registers in software can be found in Section 3.2 Basic Connections.

(Throughout this document, all registers are defined with the MSB on the left and the LSB on the right.)

2.1.1 Main Registers

The address bits are used to map a large memory space.

All registers default to 0 at powerup.

Table 8. Addresses of Programming Registers

A1	A0	Name	Description
0	0	MCR	Master Control and Status Register (read/write)
0	1	LAR	Lower Address Register—Lower Indirect Address (time slot) (write only)
1	0	AMR	Address Mode Register—Upper Address (stream) and Address Type (write only)
1	1	IDR	Indirect Data Register (read/write)

2.1.2 Master Control and Status Register

Table 9. Master Control and Status Register

Bit	Name	Description
7	MR	**Master (Software) Reset**. A high reinitializes the T8100 registers.
6	CER	**Clock Error Reset**. A high resets the error bits of the CLKERR registers.
5	SER	**System Error Reset**. A high resets the error bits of the SYSERR register. (Note that MR, CER, and SER are automatically cleared by the T8100 after the requested reset is complete.)
4	AP	**Active Page**. This bit identifies which of the double-buffered data memories are active. A zero indicates buffer 0; a one indicates buffer 1. The AP identifies which data buffer is being accessed during a write operation (i.e., input from local streams or input from H-Bus).
3	HBE	**H-Bus Enable**. On powerup or software reset, all H-Bus pins (including clocks) are disabled. HBE must be set high to reenable the 3-stated buffers.
2	LBE	**Local Bus Enable**. Same function as HBE for local data outputs.
1	LCE	**Local Clock Enable**. Enables all other local functions: clocks, frame groups, etc. (Note that the TCLKO is disabled during a Master Reset and is unaffected by HBE, LBE, or LCE, though there are control bits for this signal in the CKP register, Section 2.4.6 Clock Control Register Definitions.)
0	CB	**CAM Busy**. A status bit indicating microprocessor activity in any of the CAM blocks. A high means that one (or more) of the CAMs is being accessed by the microprocessor. In most cases, this bit will read low since there are many internal operational cycles dedicated to the microprocessor, which allow it to finish quickly.

2 Architecture and Functional Description (continued)

2.1 Register/Memory Maps (continued)

2.1.3 Address Mode Register

The AMR is defined in Table 10 below where (aaaa) is the stream address and the LAR is the time-slot address of the selected memory space.

Note: All unused AMR values are reserved.

Table 10. Address Mode Register

Bits 7—4	Bits 3—0	Register Function
0000	0000	Control Registers.
0001	(aaaa)	Local Bus, Data Memory 1.
0010	(aaaa)	Local Bus, Data Memory 2.
0100	(aaaa)	Local Bus, Connection Memory, Time-Slot Field.
0101	(aaaa)	Local Bus, Connection Memory, Stream, and Control Bit Field.
0111	0000	Local Bus, Holding Registers, Reset.
1001	0000	CAM, Data Memory 1.
1010	0000	CAM, Data Memory 2.
1011	0000	CAM, Connection, Time-Slot Field.
1011	0001	CAM, Connection, Stream, and Control Bit Field.
1011	0010	CAM, Connection, Tag Field.
1110	0000	CAM, Even, Make Connection (MKCE). Write to next free location.
1110	0001	CAM, Odd, Make Connection (MKCO). Write to next free location.
1110	0011	CAM, Local, Make Connection (MKCL). Write to next free location.
1110	0100	CAM, Even, Break Connection (BKCE).
1110	0101	CAM, Odd, Break Connection (BKCO).
1110	0111	CAM, Local, Break Connection (BKCL).
1110	1000	CAM, Even, Clear Location (CLLE). Requires LAR.
1110	1001	CAM, Odd, Clear Location (CLLO). Requires LAR.
1110	1011	CAM, Local, Clear Location (CLLL). Requires LAR.
1110	1100	CAM, Even, Read Location (RDCE). Requires LAR, IDR holds results.
1110	1101	CAM, Odd, Read Location (RDCO). Requires LAR, IDR holds results.
1110	1111	CAM, Local, Read Location (RDCL). Requires LAR, IDR holds results.
1111	0000	CAM, Even, Find Entry (FENE). IDR holds results.
1111	0001	CAM, Odd, Find Entry (FENO). IDR holds results.
1111	0011	CAM, Local, Find Entry (FENL). IDR holds results.
1111	1000	CAM, Even, Reset (RSCE).
1111	1001	CAM, Odd, Reset (RSCO).
1111	1011	CAM, Local, Reset (RSCL).
1111	1100	CAM, Holding Registers, Reset (RCH).
1111	1111	CAM, Initialize (CI). Reset all CAM locations and holding registers.

2 Architecture and Functional Description (continued)

2.1 Register/Memory Maps (continued)

2.1.4 Control Register Memory Space

Function of LAR values when AMR = 0x00. All control registers reset to 0x00.

Table 11. Control Register Memory Space

Register Address	Register Mnemonic	Description	Refer to Section
0, 0x00	CKM	Clocks, Main Clock Selections	2.4.6
1, 0x01	CKN	Clocks, NETREF Selections	2.4.6
2, 0x02	CKP	Clocks, Programmable Outputs	2.4.6
3, 0x03	CKR	Clocks, Resource Selection	2.4.6
4, 0x04	CKS	Clocks, Secondary (Fallback) Selection	2.4.6
5, 0x05	CK32	Clocks, Locals 3 and 2	2.4.6
6, 0x06	CK10	Clocks, Locals 1 and 0	2.4.6
7, 0x07	CKMD	Clocks, Main Divider	2.4.6
8, 0x08	CKND	Clocks, NETREF Divider	2.4.6
9, 0x09	CKRD	Clocks, Resource Divider	2.4.6
10—11, 0x0A—0x0B	(Reserved)	—	—
12, 0x0C	LBS	Local Stream Control	2.2.4
13, 0x0D	(Reserved)	—	—
14, 0x0E	CON	Connection Delay Type	Appendix B
15, 0x0F	(Reserved)	—	—
16, 0x10	HSL	H-Bus Stream Control, Low Byte	2.3.5
17, 0x11	HSH	H-Bus Stream Control, High Byte	2.3.5
18—23, 0x12—0x17	(Reserved)	—	—
24, 0x18	GPR	General-purpose I/O Register	2.5.2
25—31, 0x19—0x1F	(Reserved)	—	—
32, 0x20	FRLA	Frame Group A, Start Address, Low	2.5.3
33, 0x21	FRHA	Frame Group A, High Address and Control	2.5.3
34, 0x22	FRLB	Frame Group B, Start Address, Low	2.5.3
35, 0x23	FRHB	Frame Group B, High Address and Control	2.5.3
36, 0x24	FRPL	Frame Group B, Programmed Output, Low	2.5.3
37, 0x25	FRPH	Frame Group B, Programmed Output, High	2.5.3
38—39, 0x26—0x27	(Reserved)	—	—
40, 0x28	CLKERR1	Clock Error Register, Error Indicator	2.6
41, 0x29	CLKERR2	Clock Error Register, Current Status	2.6
42, 0x2A	SYSERR	System Error Register	2.6
43, 0x2B	CKW	Clock Error/Watchdog Masking Register	2.4.6 & 2.6
44—47, 0x2C—0x2F	(Reserved)	—	—
48, 0x30	DIAG1	Diagnostics Register 1	2.8.2
49, 0x31	DIAG2	Diagnostics Register 2	2.8.2
50, 0x32	DIAG3	Diagnostics Register 3	2.8.2
51—255, 0x33—0x0FF	(Reserved)	—	—

2 Architecture and Functional Description (continued)

2.1 Register/Memory Maps (continued)

2.1.4 Control Register Memory Space (continued)

This section is a summary of the register functions. The reader is encouraged to read through the rest of this specification to learn the details of the individual registers and their interactions with the overall architecture.

Table 12. CKM: Clocks, Main Clock Selection, 0x00

Bit	Description
7	Phase Alignment Enable
6	Phase Alignment Select
5	Compatibility Clock Direction
4	Input Clock Invert
3	Input Clock Select, MSB
2	Input Clock Select
1	Input Clock Select
0	Input Clock Select, LSB

Table 13. CKN: Clocks, NETREF Selections, 0x01

Bit	Description
7	Output Enable
6	I/O Select
5	Bypass Select
4	Input Clock Invert
3	Input Clock Select, MSB
2	Input Clock Select
1	Input Clock Select
0	Input Clock Select, LSB

Table 14. CKP: Clocks, Programmable Outputs, 0x02

Bit	Description
7	TCLK Select, MSB
6	TCLK Select
5	TCLK Select, LSB
4	CT_C8 Pins, Input Type Select
3	CT_C8A Output Enable
2	CT_C8B Output Enable
1	CT_C8 Pins, Output Type Select
0	(Reserved)

Table 15. CKR: Clocks, Resource Selection, 0x03

Bit	Description
7	Resource Select, MSB
6	Resource Select, LSB
5	PLL #1 Bypass
4	PLL #1 Rate Select
3	PLL #2 Bypass
2	PLL #2 Rate Select
1	SCLK Output Select, MSB
0	SCLK Output Select, LSB

Table 16. CKS: Clocks, Secondary (Fallback) Selection, 0x04

Bit	Description
7	Secondary Resource Select, MSB
6	Secondary Resource Select, LSB
5	Fallback Type Select, MSB
4	Fallback Type Select, LSB
3	Fallback, Force Selection of Secondary Input
2	Secondary Input Clock Select, MSB
1	Secondary Input Clock Select
0	Secondary Input Clock Select, LSB

Table 17. CK32: Clocks, Locals 3 and 2, 0x05

Bit	Description
7	Local Clock 3 Select, MSB
6	Local Clock 3 Select
5	Local Clock 3 Select
4	Local Clock 3 Select, LSB
3	Local Clock 2 Select, MSB
2	Local Clock 2 Select
1	Local Clock 2 Select
0	Local Clock 2 Select, LSB

Table 18. CK10: Clocks, Locals 1 and 0, 0x06

Bit	Description
7	Local Clock 1 Select, MSB
6	Local Clock 1 Select
5	Local Clock 1 Select
4	Local Clock 1 Select, LSB
3	Local Clock 0 Select, MSB
2	Local Clock 0 Select
1	Local Clock 0 Select
0	Local Clock 0 Select, LSB

2 Architecture and Functional Description (continued)

2.1 Register/Memory Maps (continued)

2.1.4 Control Register Memory Space (continued)

Table 19. CKMD: Clocks, Main Divider; CKND: Clocks, NETREF Divider; CKRD: Clocks, Resource Divider, 0x07, 0x08, 0x09

Bit	Description
7	Divide Value, MSB
6	Divide Value
5	Divide Value
4	Divide Value
3	Divide Value
2	Divide Value
1	Divide Value
0	Divide Value, LSB

Table 20. LBS: Local Stream Control, 0x0C

Bit	Description
7	Parallel/Serial Select, MSB
6	Parallel/Serial Select, LSB
5	Local Group A Rate Select, MSB
4	Local Group A Rate Select, LSB
3	Local Group B Rate Select, MSB
2	Local Group B Rate Select, LSB
1	Local Group C Rate Select, MSB
0	Local Group C Rate Select, LSB

Table 21. CON: Connection Delay Type, 0x0E

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	Reserved
1	Disabled Connection-by-Connection Delay Setting
0	Enable Linear Delay

Table 22. HSL: H-Bus Stream Control, Low Byte, 0x10

Bit	Description
7	H-Bus Group D Rate Select, MSB
6	H-Bus Group D Rate Select, LSB
5	H-Bus Group C Rate Select, MSB
4	H-Bus Group C Rate Select, LSB
3	H-Bus Group B Rate Select, MSB
2	H-Bus Group B Rate Select, LSB
1	H-Bus Group A Rate Select, MSB
0	H-Bus Group A Rate Select, LSB

Table 23. HSH: H-Bus Stream Control, High Byte, 0x11

Bit	Description
7	H-Bus Group H Rate Select, MSB
6	H-Bus Group H Rate Select, LSB
5	H-Bus Group G Rate Select, MSB
4	H-Bus Group G Rate Select, LSB
3	H-Bus Group F Rate Select, MSB
2	H-Bus Group F Rate Select, LSB
1	H-Bus Group E Rate Select, MSB
0	H-Bus Group E Rate Select, LSB

Table 24. GPR: General-Purpose I/O Register, 0x18

Bit	Description
7	General-Purpose I/O, MSB
6	General-Purpose I/O
5	General-Purpose I/O
4	General-Purpose I/O
3	General-Purpose I/O
2	General-Purpose I/O
1	General-Purpose I/O
0	General-Purpose I/O, LSB

2 Architecture and Functional Description (continued)

2.1 Register/Memory Maps (continued)

2.1.4 Control Register Memory Space (continued)

Table 25. FRLA: Frame Group A, Start Address Low, 0x20

Bit	Description
7	Start Address, Bit 7, or Programmed Output, Bit 7
6	Start Address, Bit 6, or Programmed Output, Bit 6
5	Start Address, Bit 5, or Programmed Output, Bit 5
4	Start Address, Bit 4, or Programmed Output, Bit 4
3	Start Address, Bit 3, or Programmed Output, Bit 3
2	Start Address, Bit 2, or Programmed Output, Bit 2
1	Start Address, Bit 1, or Programmed Output, Bit 1
0	Start Address, LSB, or Programmed Output, Bit 0

Table 26. FRHA: Frame Group A, High Address and Control, 0x21

Bit	Description
7	Rate Select, MSB
6	Rate Select, LSB
5	Pulse Width Select, MSB
4	Pulse Width Select, LSB
3	Frame Invert, or Programmed Output, Bit 11
2	Start Address, MSB, or Programmed Output, Bit 10
1	Start Address, Bit 9, or Programmed Output, Bit 9
0	Start Address, Bit 8, or Programmed Output, Bit 8

Table 27. FRLB: Frame Group B, Start Address Low, 0x22

Bit	Description
7	Start Address, Bit 7
6	Start Address, Bit 6
5	Start Address, Bit 5
4	Start Address, Bit 4
3	Start Address, Bit 3
2	Start Address, Bit 2
1	Start Address, Bit 1
0	Start Address, LSB

Table 28. FRHB: Frame Group B, High Address and Control, 0x23

Bit	Description
7	Rate Select, MSB
6	Rate Select, LSB
5	Pulse Width Select, MSB
4	Pulse Width Select, LSB
3	Frame Inversion Select
2	Start Address, MSB
1	Start Address, Bit 9
0	Start Address, Bit 8

Table 29. FRPL: Frame Group B, Programmed Output, Low, 0x24

Bit	Description
7	Programmed Output, Bit 7
6	Programmed Output, Bit 6
5	Programmed Output, Bit 5
4	Programmed Output, Bit 4
3	Programmed Output, Bit 3
2	Programmed Output, Bit 2
1	Programmed Output, Bit 1
0	Programmed Output, Bit 0

Table 30. FRPH: Frame Group B, Programmed Output, High, 0x25

Bit	Description
7	Group A Output Pins Select, MSB
6	Group A Output Pins Select, LSB
5	(Reserved, Use 0)
4	Group B Output Pins Select
3	Programmed Output, Bit 11
2	Programmed Output, Bit 10
1	Programmed Output, Bit 9
0	Programmed Output, Bit 8

2 Architecture and Functional Description (continued)

2.1 Register/Memory Maps (continued)

2.1.4 Control Register Memory Space (continued)

Table 31. CLKERR1: Clock Error Register, Error Indicator, 0x28

Bit	Description
7	C8A or Frame A Error
6	C8B or Frame B Error
5	FR_COMPn Error
4	C16+ or C16– Error
3	C4n or C2 Error
2	$\overline{\text{SCLKX2}}$ Error
1	SCLK Error
0	NETREF Error

Table 32. CLKERR2: Clock Error Register, Current Status, 0x29

Bit	Description
7	C8A or Frame A Fault Status
6	C8B or Frame B Fault Status
5	FR_COMPn Fault Status
4	C16+ or C16– Fault Status
3	C4n or C2 Fault Status
2	$\overline{\text{SCLKX2}}$ Fault Status
1	SCLK Fault Status
0	NETREF Fault Status

Table 33. SYSERR: System Error Register, 0x2A

Bit	Description
7	Even CAM Underflow Error (No Match)
6	Odd CAM Underflow Error (No Match)
5	Local CAM Underflow Error (No Match)
4	Even CAM Overflow or No-Match Error
3	Odd CAM Overflow or No-Match Error
2	Local CAM Overflow or No-Match Error
1	(Reserved)
0	Fallback Enable Indicator

Table 34. CKW: Clock Error/Watchdog Masking Register, 0x2B

Bit	Description
7	C8A and Frame A Error Mask
6	C8B and Frame B Error Mask
5	FR_COMPn Error Mask
4	C16+ and C16– Error Mask
3	C4n and C2 Error Mask
2	$\overline{\text{SCLKX2}}$ Error Mask
1	SCLK Error Mask
0	NETREF Error Mask

Table 35. DIAG1: Diagnostics Register 1, 0x30

Bit	Description
7	Frame Group A Output Select, MSB
6	Frame Group A Output Select, LSB
5	Frame Group B Output Select, MSB
4	Frame Group B Output Select, LSB
3	Memory Fill Enable
2	Memory Fill Pattern Select, MSB
1	Memory Fill Pattern Select, LSB
0	Memory Fill Status Bit (Read Only)

Table 36. DIAG2: Diagnostics Register 2, 0x31

Bit	Description
7	Frame Groups Cycle Test Enable
6	Break State Counter into Subsections
5	Bypass Internal Frame with FR_COMPn
4	(Reserved)
3	Enable State Counter Parallel Load
2	Parallel Load Value of State Counter, MSB
1	Parallel Load Value of State Counter, Bit 9
0	Parallel Load Value of State Counter, Bit 8

Table 37. DIAG3: Diagnostics Register 3, 0x32

Bit	Description
7	Parallel Load Value of State Counter, Bit 7
6	Parallel Load Value of State Counter, Bit 6
5	Parallel Load Value of State Counter, Bit 5
4	Parallel Load Value of State Counter, Bit 4
3	Parallel Load Value of State Counter, Bit 3
2	Parallel Load Value of State Counter, Bit 2
1	Parallel Load Value of State Counter, Bit 1
0	Parallel Load Value of State Counter, LSB

2 Architecture and Functional Description (continued)

2.2 Local Bus Section

Figure 4 shows the local bus section function diagram.

Note: Routing and MUXing for the H-Bus section is included since the H-Bus requires access to the converters for local bus-to-H-Bus or H-Bus-to-local bus transfers (the H-Bus is discussed in Section 2.3 H-Bus Section).

XCS is a pseudo serial stream, read out from the connection memory on each memory access. It is read out directly, i.e., not passing through any parallel/serial converters or holding registers, so it precedes the connection associated with it by one time slot.

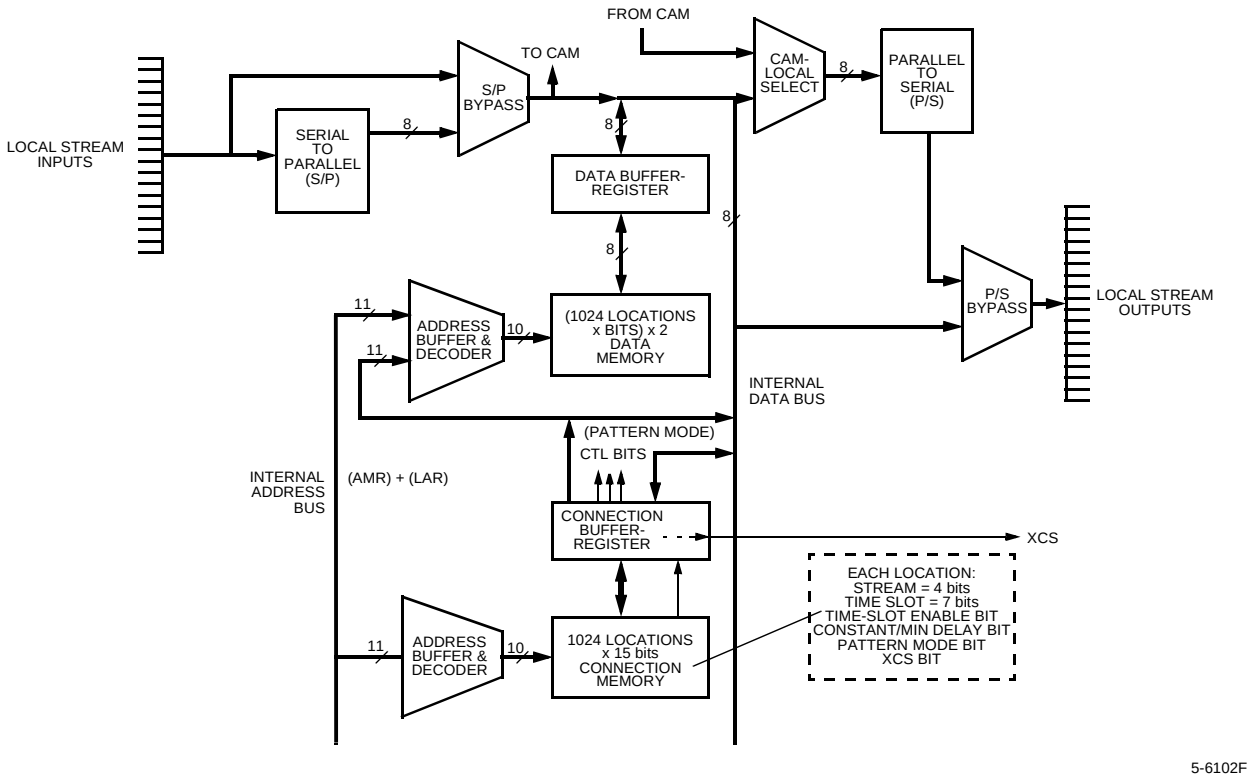


Figure 4. Local Bus Section Function

2 Architecture and Functional Description (continued)

2.2 Local Bus Section (continued)

2.2.1 Constant Frame Delay and Minimum Delay Connections

The local bus section contains the local connection memory and the double-buffered local data memory. Collectively, the connection memory and data memory are referred to as local memory since it is used for implementing local-to-local switching only. Operation is similar to other time-slot interchangers. Data is written into the memory in a fixed order and then read out according to the indirect addresses held in the connection memory. If any of the connections on the T8100 are operating in constant frame delay (also called constant delay) mode, then the output data is accessed from a second block of data memory. The input data will not be output until the next frame boundary has been crossed and the memory blocks have swapped functions. Figure 5 shows an example of a set of connections which create the delay types referred to as minimum delay and constant delay.

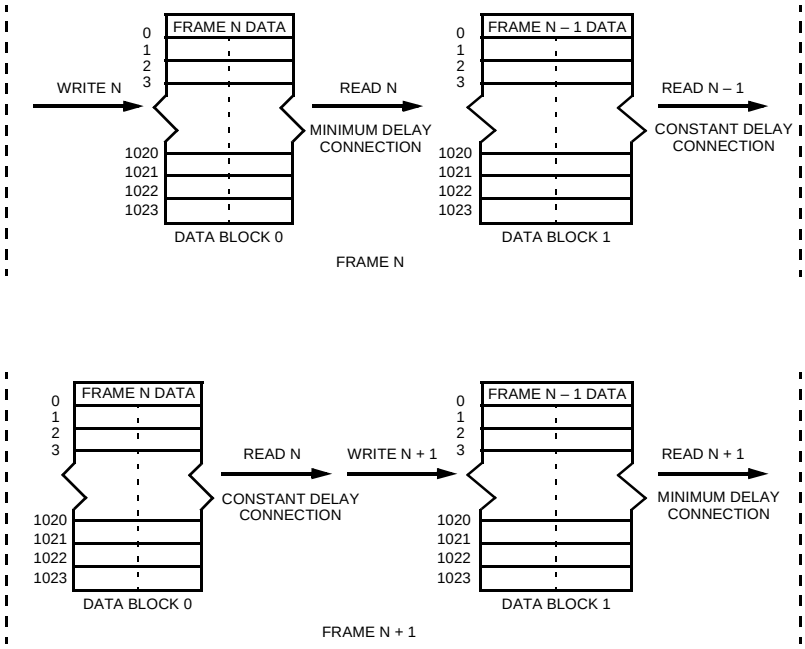


Figure 5. Local Bus Memory Connection Modes

2 Architecture and Functional Description (continued)

2.2 Local Bus Section (continued)

2.2.2 Serial and Parallel

Nominally, the memory will be accessed by serial data streams which will require conversion of serial-to-parallel (S/P) for write accesses and parallel-to-serial (P/S) for read accesses. Since the local memory can have up to 16 serial inputs and 16 serial outputs, there will be a maximum of 16 S/P converters and 16 P/S converters operating simultaneously. If desired, eight of the S/P converters, local inputs 0—7, can be bypassed for a direct parallel write to the data memory. Likewise, eight of the P/S converters, local outputs 0—7, can be bypassed for a direct parallel read of the data memory. Unused S/P or P/S converters are nonfunctional in these modes.

Note: The normal serial-to-serial local streaming is not available simultaneously with any of the parallel modes.

2.2.3 Data Rates and Time-Slot Allocation

At its maximum, the T8100 will be able to process 1024 nonblocking-to-local connections. The data rate 8.192 Mbits/s corresponds to 128 time slots, 4.096 Mbits/s corresponds to 64 time slots, and 2.048 Mbits/s corresponds to 32 time slots. Since different data rates require different amounts of memory, the local memory can be filled in a number of ways. A nonblocking switch permits any time slot on any stream to be switched to another time slot on any stream in any direction.

The local streams are arranged in three groups: A, B, and C. Group A corresponds to the local data pins 0—7, group B with local data pins 8—11, and group C with local data pins 12—15. The groups may be operated at any of the three data rates: 2.048 Mbits/s, 4.096 Mbits/s, or 8.192 Mbits/s; however, group B is activated only when group A is operating below 8.192 Mbits/s. Likewise, group C is activated when group B is operating below 8.192 Mbits/s.

Note: In order to efficiently fill the memory, the memory locations are read or filled in the same order regardless of their activation or rate.

The streams are scanned in intervals equal to 8.192 Mbits/s time slots: first group A from 0 through 7, then group B from 8 through 11, then group C from 12 through 15. If a group is active, the data is input from or output to the streams in that group. If a group is operating below 8.192 Mbits/s and has already been scanned (at the 8.192 Mbits/s rate), then the data transfer operation is ignored.

For T8100 addressing, the user directly provides stream and time-slot information. The T8100 will map this into the physical memory, regardless of which stream groups are active or at what rate. While this makes programming simpler, it makes the internal operation more difficult to understand. Several diagrams are required to illustrate how the memory utilization works.

Unassigned time slots in the local output section are 3-stated. Therefore, multiple lines can be connected together.

2 Architecture and Functional Description (continued)

2.2 Local Bus Section (continued)

2.2.3 Data Rates and Time-Slot Allocation (continued)

Figure 6 below shows the overall structure of the local memory:

Note: Both the connection and two data memories are arranged in four blocks of 256 locations each (i.e., 4 x [4 x 64]).

The arrangement is important to establishing a memory fill pattern which supports all of the various groups and rates. The rows of each memory, which are split into four groups of 4, correspond to the 16 streams. The columns correspond to 64 time-slot addresses.

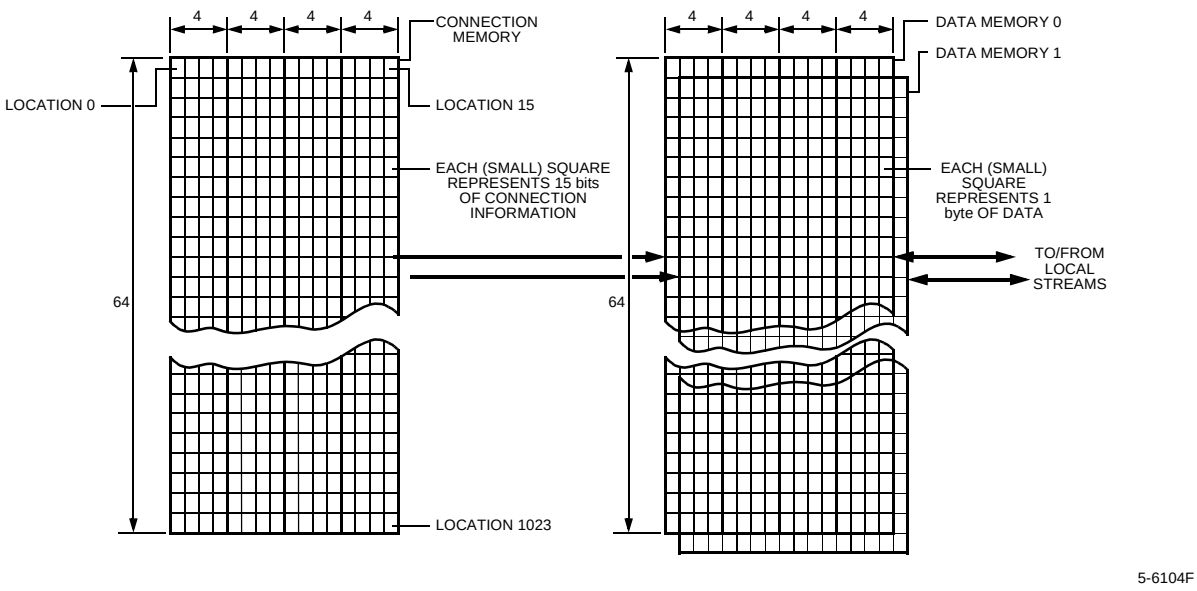


Figure 6. Local Streams, Memory Structure

2 Architecture and Functional Description (continued)

2.2 Local Bus Section (continued)

2.2.3 Data Rates and Time-Slot Allocation (continued)

Examples of how the memory is filled are found in Figure 7.

Note: Again, the user needs only to provide stream and time-slot addresses; the T8100 will generate the internal memory addresses.

Both the connection and data memories are filled using the same algorithm. In the case where group C is running at 8.192 Mbits/s, group B is at 4.096 Mbits/s (or 2.048 Mbits/s), and group A is at 2.048 Mbits/s, then an additional virtual memory space of 4 x 64 locations is created by the T8100 from unused locations in other parts of the memory.

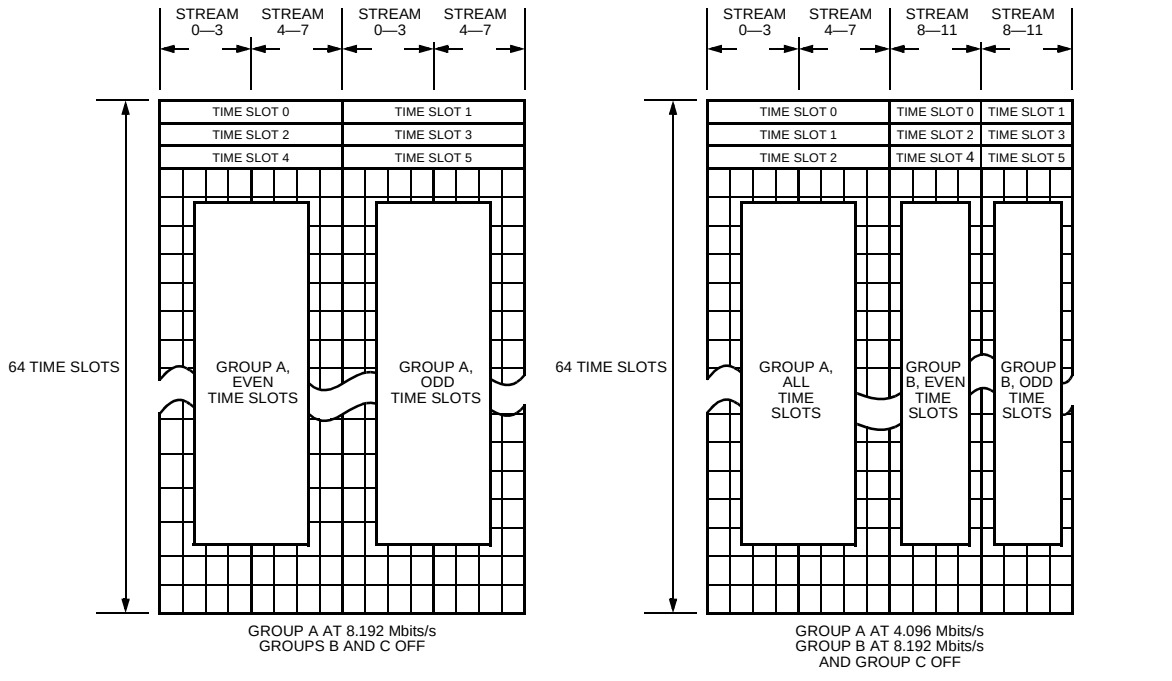


Figure 7. Local Memory, Fill Patterns

2 Architecture and Functional Description (continued)

2.2 Local Bus Section (continued)

2.2.3 Data Rates and Time-Slot Allocation (continued)

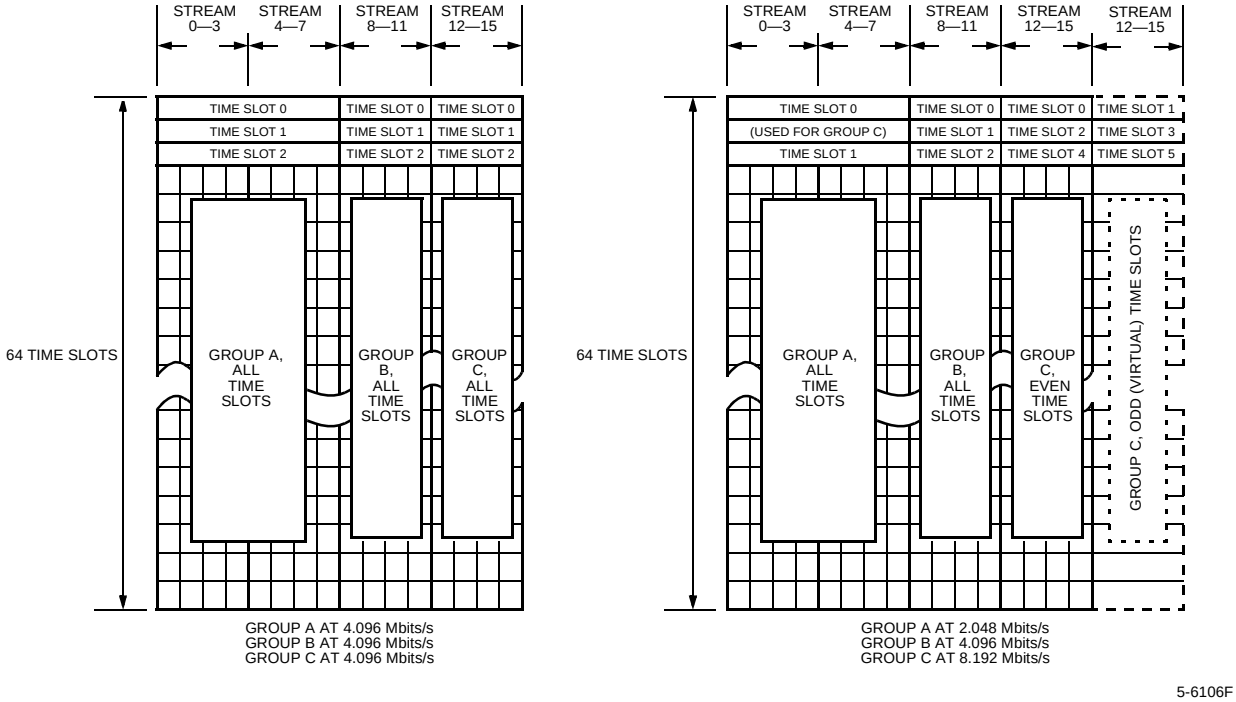


Figure 7. Local Memory, Fill Patterns (continued)

In any of the parallel modes (S/P, P/S, P/P), the local memories treat parallel data as a series of sequential time slots (i.e., all one stream): 8.192 Mbits/s corresponds to 1024 time slots, 4.096 Mbits/s corresponds to 512 time slots, and 2.048 Mbits/s corresponds to 256 time slots. The memory locations are scanned in order from 0 to 1023 at 8.192 Mbits/s, even locations are scanned at 4.096 Mbits/s (odd locations are skipped), and at 2.048 Mbits/s, every second even location is scanned.

2 Architecture and Functional Description (continued)

2.2 Local Bus Section (continued)

2.2.4 LBS: Local Stream Control, 0x0C

The normal mode of operation for local streams is serial in/serial out, but parallel modes are available. Modes and data rates are controlled by register LBS. The mapping is shown below. See the preceding pages for a full description.

Table 38. LBS: Local Stream Control, 0x0C

REG	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LBS	—	P/S		SGa		SGb		SGc	

Symbol	Bit	Name/Description
P/S	7—6	P/S = 00. Serial In/Serial Out. The SGa bits control the group A pins, SGb bits control the group B pins, and SGc bits control the group C pins. As serial streams, input and output rates within the same group are constrained to be identical so both inputs and outputs share the same 2 bits for programming. The SGb bits are enabled when SGa ≠ 11. The SGc bits are enabled when SGb ≠ 11.
		P/S = 01. Serial In/Parallel Out. SGa sets input (serial) rate using the rate definition within this table. SGb is reserved. SGc sets the output (parallel) rate using the rate definition within this table.
		P/S = 10. Parallel In/Serial Out. SGa sets input (parallel) rate. SGb is reserved. SGc sets output (serial) rate.
		P/S = 11. Parallel In/Parallel Out. SGa sets input (parallel) rate. SGb is reserved. SGc sets output (parallel) rate.
SGa	5—4	SGa = 00, 3-state. SGa = 01, 2.048 Mbits/s. SGa = 10, 4.096 Mbits/s. SGa = 11, 8.192 Mbits/s.
SGb	3—2	SGb = 00, 3-state. SGb = 01, 2.048 Mbits/s. SGb = 10, 4.096 Mbits/s. SGb = 11, 8.192 Mbits/s.
SGc	1—0	SGc = 00, 3-state. SGc = 01, 2.048 Mbits/s. SGc = 10, 4.096 Mbits/s. SGc = 11, 8.192 Mbits/s.

There are no additional registers required for addressing the local memory other than the main address registers (discussed in Section 2.1 Register/Memory Maps). The data and connection memory locations can be queried for their contents by indirect reads through the main address registers; however, the memory locations are referred to by the stream and time-slot designators, rather than physical address locations, to simplify the queries.

2 Architecture and Functional Description (continued)

2.2 Local Bus Section (continued)

2.2.5 State Counter Operation

All operations are synchronized to the master state counter. The state counter is in turn synchronized to the internal frame signal and driven by an internal 65.536 MHz clock. In normal operation, the internal frame and clock are synchronized to either the H-Bus or trunks (see Section 2.4 Clocking Section, for a more detailed explanation of clocking options). The local memory states are illustrated in Figure 8. The state counter is a modulo-8192 counter (7 bits for time slot, 4 bits for stream, 2 bits for state function) which can also be reset and loaded with other values for diagnostic purposes (as described in Section 2.8 Testing and Diagnostics). The H-Bus memories are also referenced to this state counter so that T8100 maintains synchronization with the H-Bus to ensure proper access to the bus as well as ensure synchronization between the H-Bus and local memory structures. The H-Bus memories are discussed in Section 2.3 H-Bus Section.

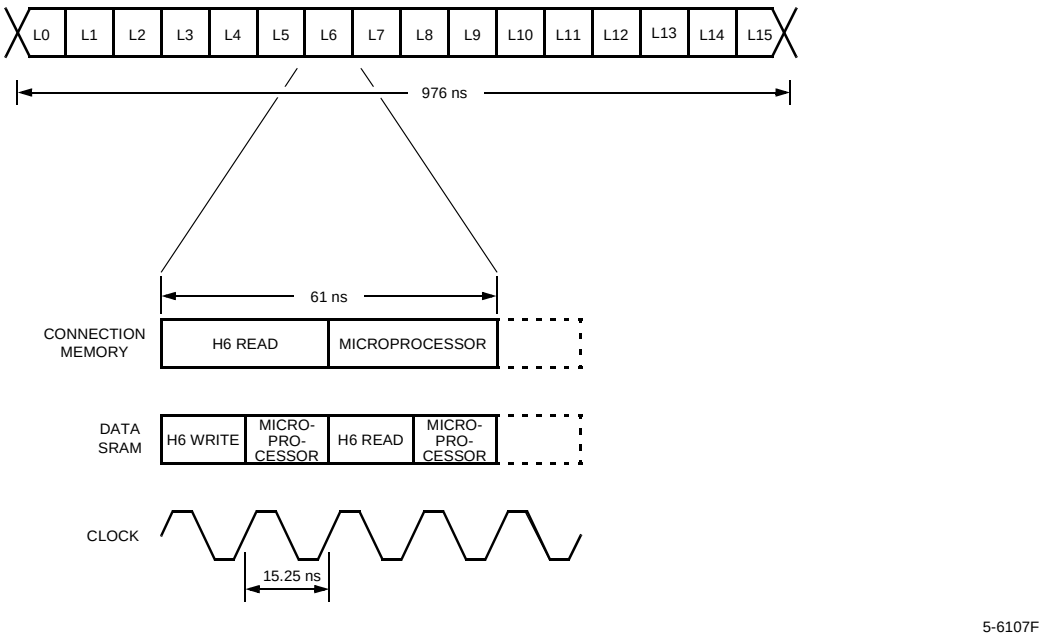


Figure 8. Simplified Local Memory State Timing, 65.536 MHz Clock

2 Architecture and Functional Description (continued)

2.3 H-Bus Section

2.3.1 Memory Architecture

To access the H-Bus, the T8100 uses a new twist on an existing approach to accessing large address spaces: the data is stored in an independent double-buffered SRAM which acts like the local data memory, but the connection information for the H-Bus is held in three 256 location CAMs. Two CAMs are used for two groups of 16 H-Bus streams each, and one CAM for all 16 local input/output pairs. Each CAM compares 16 streams for read and write and allows access time to the host microprocessor for updates to the connections. Thus, each stream is allotted three operations per 976 ns time slot, so there are a maximum of 48 accesses per CAM per time slot. The CAMs must operate for at least 20.34 ns/access* or faster. The selected technology operates at 13 ns/access maximum, so an internal clock speed of 15.26 ns (65.536 MHz) is used.

For the following discussions, the reader should refer to Figure 9. The combined comparison plus retrieval operations take 2 CAM cycles, leaving little time for microprocessor updates. To circumvent this, a separate SRAM (actually, a register file) is tied to each CAM. Each entry of this register file is associated with an entry in the CAM on a location-by-location basis. (For example, physical address 0xA7 in the CAM is coupled with physical address 0xA7 of the register file.) The CAMs will have only the comparand field for stream and time-slot addresses, and the associated register files will hold the data field, which is comprised of a tag (an indirect pointer to the double-buffered data SRAM) and some control bits. Using the associated SRAM allows the operations to be pipelined so that the data retrieval occurs while the CAMs are doing the next comparison. The SRAM is double-buffered to permit constant delay or minimum delay on a connection-by-connection basis, as described in Section 2.2.1 Constant Frame Delay and Minimum Delay Connections and as illustrated in Figure 5.

* The H-Bus presents a unique set of problems. A full nonblocking, double-buffered switch of 5120 locations has significant barriers in size and in control of memory access time. Further, the traffic between the local bus and H-Bus is generally limited to a small number of time slots at any given moment (120 full duplex is typical, although we are permitting 128 duplex or 256 simplex connections), but the requirement to access any time slot out of the full range of 5120 locations remains. To solve this, content addressable memories (CAM) are utilized. They provide access to the full 5120 locations through an encoded width (13 bits), but require a depth equal to the maximum number of connections required (256).

2 Architecture and Functional Description (continued)

2.3 H-Bus Section (continued)

2.3.1 Memory Architecture (continued)

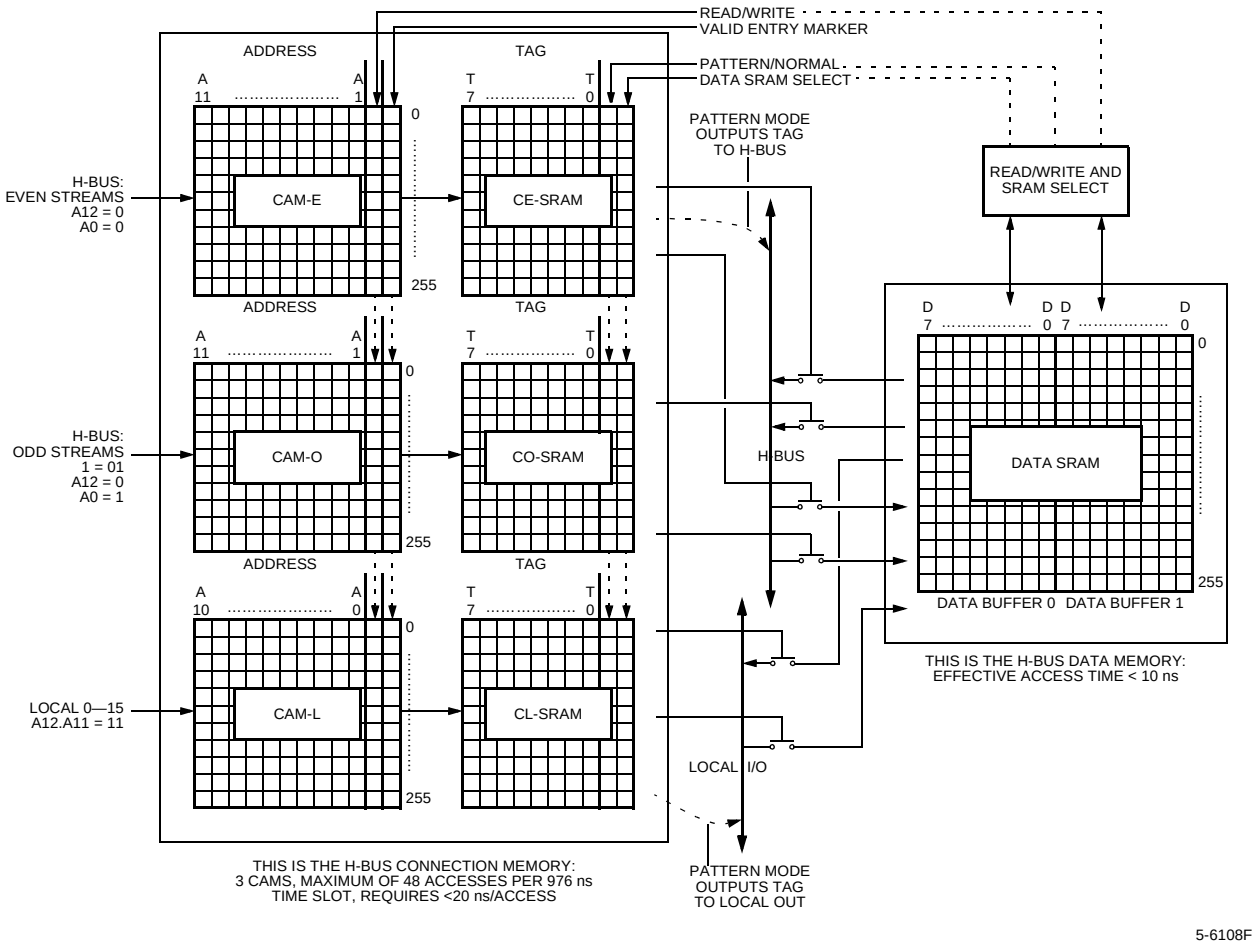


Figure 9. CAM Architecture

The maximum number of connections is set by the number of locations in the data SRAM and the CAMs. In this implementation, 256 simplex connections are permitted. Since one connection requires two CAM entries pointing to a common data location, the maximum number of connections could be reduced to 128 simplex if all connection entries reside within only one CAM. The maximum number of connections is increased above 256 simplex if the connection type is broadcast, i.e., from one to many.

2 Architecture and Functional Description (continued)

2.3 H-Bus Section (continued)

2.3.2 CAM Operation and Commands

The three CAMs operate in parallel. Each CAM's comparand field is compared with the state counter (Section 2.2.5 State Counter Operation) which holds the existing stream and time-slot value*. If there is a match, the CAM issues a hit. If there is more than one match, then it is considered a multiple hit. Likewise, no match is a miss. As a part of the state counter, a bit is toggled for read/write. The read/write bit is stored in the CAM, so it becomes part of the value to be compared. If the comparison for a write yields a hit, then there is a request for write access to the data memory for the incoming data from the H-Bus. If the comparison for a read yields a hit, then there is a request for a read access from the data memory for outgoing data to the H-Bus. Any multiple hit within one CAM block is treated as a controlled error although it is not reported. The action taken is to acknowledge the hit which corresponds to the lowest physical address of the CAM. A miss implies no action. A multiple hit is assigned to be more than one valid connection. These are prioritized such that the match with the lowest physical address (i.e., closest to CAM location 0x0) is the address which is processed. Thus, errors are handled in a controlled manner. Multiple hits can occur because multiple locations are assigned to the same time slot. Bad software can cause this problem. A controlled error has no impact on performance, and the CAM contents are not changed as a result of the error. The data SRAMs are actually dual-port register files which will process both writes and reads on each clock cycle of the clock. The T8100 can process a read and write request from each CAM and two microprocessor requests during the time of one address comparison. Due to the fixed order of operations, the data SRAM cannot overflow or underflow like the CAMs. The timing is shown in Figure 10.

* As mentioned in Section 2.2.5 State Counter Operation, for each stream and time-slot value, the state counter goes through four functional states for each stream and time slot. These states are used to synchronize the CAMs, pipeline register files, data SRAMs, and microprocessor accesses just as they are used to synchronize local memory operations and the frame groups. (Microprocessor accesses to the memories are initiated asynchronously, though the actual microprocessor cycles are synchronous.)

2 Architecture and Functional Description (continued)

2.3 H-Bus Section (continued)

2.3.2 CAM Operation and Commands (continued)

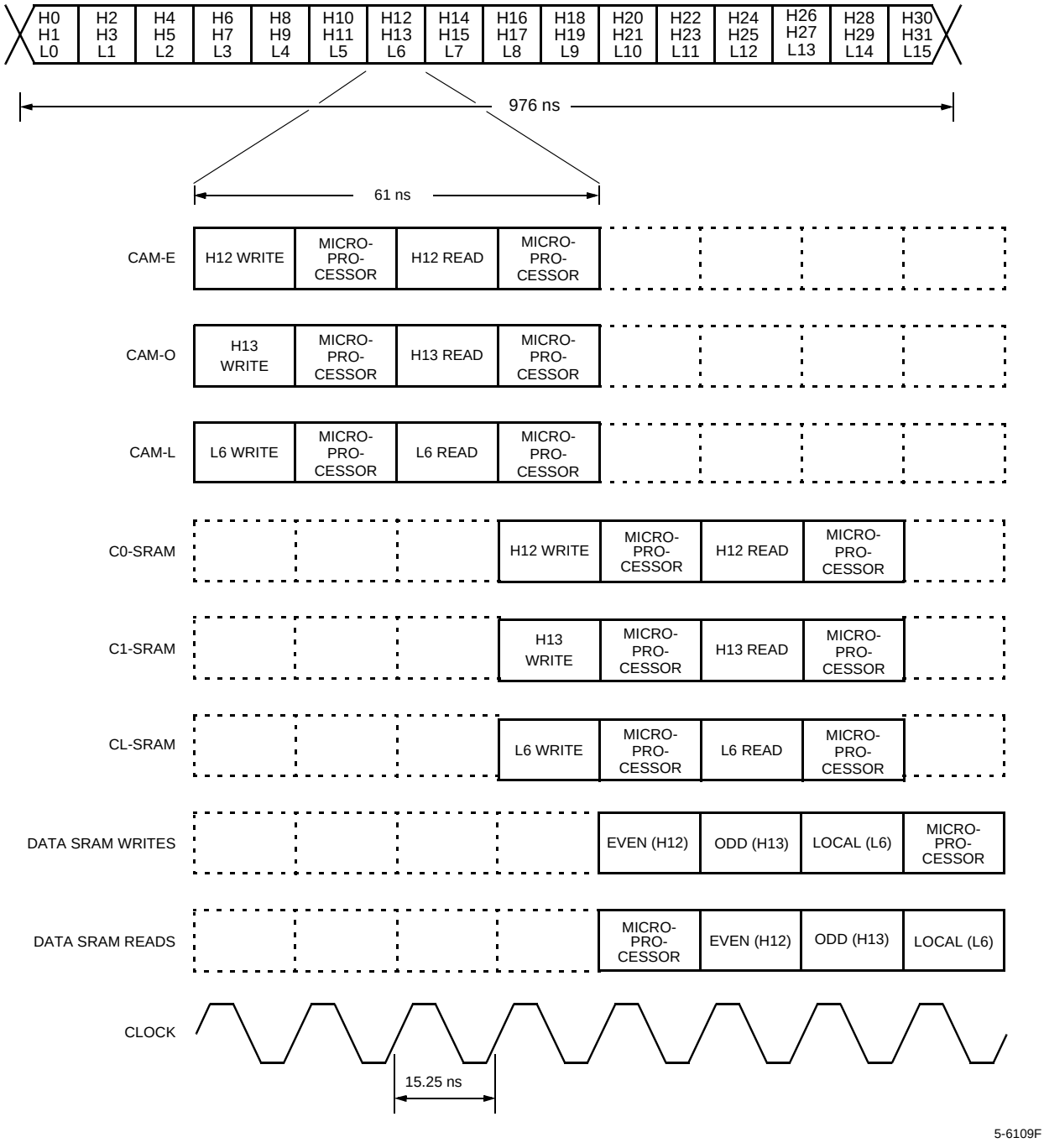


Figure 10. Simplified H-Bus State Timing, 65.536 MHz Clock

2 Architecture and Functional Description (continued)

2.3 H-Bus Section (continued)

2.3.2 CAM Operation and Commands (continued)

A number of commands are available to control the CAMs. Connections can be made or broken, entry data can be searched for, individual locations may be read or cleared, or the CAMs can be reset. The address mode register (AMR) (see Section 2.1 Register/Memory Maps) is used to issue the CAM control commands. Some commands require the use of the lower address register (LAR), and some use the IDR as a transfer register.

The tags in each CAM's associated register file reference the storage location of the data being transferred, so each CAM/tag location also has control information. The three control bits are read-to/write-from data SRAM (i.e., a direction bit, located in the CAM and used during the comparison operations), a pattern mode enable, which bypasses the data SRAM and outputs the tag directly into the specified time slot for writes to the bus, and an SRAM buffer select that controls the minimum delay or constant delay select, equivalent to the local memory's selection of minimum or constant delay.

In addition, the CAM carries a valid entry bit. This is an identifier for the status of the CAM (and corresponding register file) location. If the bit is low, as all validity bits are after a reset, then the location is available to be written into. When data is written into a location, then this bit is set, indicating that this is a valid entry. If specific data is no longer valid, such as when a connection is broken, then the bit is cleared.

The CAM commands make use of either one or two cycles. The two cycles are described pictorially in Figure 11. The reader will note that matching and retrieval are actually separate cycles. The need for two cycles accounts for the requirement of the pipeline register files.

Detailed descriptions of the commands follow:

The basic make connection command is referred to as MKCn, where n is the CAM designator*. The MKCn uses two CAM cycles: first, the CAM is searched to determine where to find the next free location (as determined by the validity bits), and during the second cycle, the next empty location is written into. The MKCn command uses holding registers which convey the connection information to the CAM and its associated register file. The three holding registers contain the lower connection address (i.e., time slot), the upper connection address (stream plus control bits), and the tag. An attempt to write to a full CAM (all 256 locations fully occupied) results in an overflow error flagged through the system error register, SYSERR (see Section 2.6 Error Registers).

Note: A single MKCn command only specifies one half of a connection. The MKCn specifies the connection address and a pointer to the data memory, but a second connection address and pointer to the same data memory location must also be provided for a complete connection.

* The H-Bus CAM covering the 16 even-numbered H-Bus streams is designated E, the H-Bus CAM covering the 16 odd-numbered H-Bus streams is designated O, and the CAM that services the 16 local stream pairs is designated L.

2 Architecture and Functional Description (continued)

2.3 H-Bus Section (continued)

2.3.2 CAM Operation and Commands (continued)

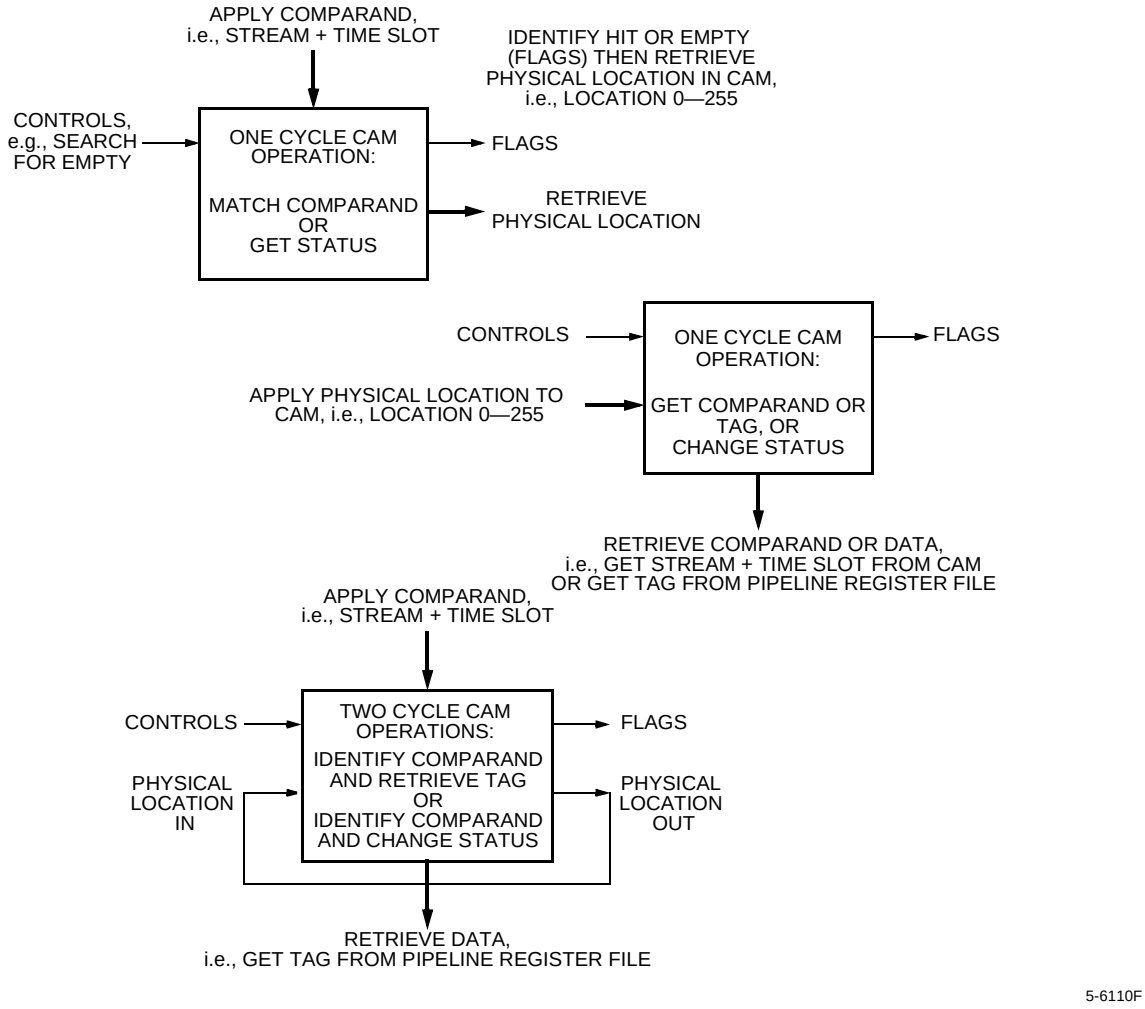


Figure 11. Illustration of CAM Cycles

2 Architecture and Functional Description (continued)

2.3 H-Bus Section (continued)

2.3.2 CAM Operation and Commands (continued)

If the user determines that a stream/time slot is no longer valid, then the validity bit may be cleared by presenting the connection address to the CAM and by using the BKCn, break connection, command. The connection that the user intends to break, which consists of the time slot, and the stream plus control bits, but not the tag, is transferred to the holding registers prior to issuing this command. This is a two-cycle command: during the first cycle, the connection address is presented to the CAM to identify which physical location holds that connection address, and then, in the second cycle, the validity bit is cleared for the identified physical location. If there is a miss, it flags a no-match error through the underflow bit in SYSERR.

Note: A complete connection break requires two BKCn commands, one for each half of the connection, as with the MKCn command.

The clear location command, CLLn, is a one-cycle command. The LAR contains the physical address (i.e., the physical CAM location) to be cleared. When it is presented to the CAM, the validity bit is cleared, returning the location to an empty status (i.e., it becomes available for new make connection commands). The CLLn can also be regarded as the second cycle of a break connection command. CLLn is valuable if several outputs are driven from a common input (broadcast) and the user wishes to break one of the output connections, but leave the others intact. When the physical location in the CAM is identified, either by software tracking or by use of the find entry command (later in this section), then the CLLn can be issued.

If the user wishes to poll the CAM for its contents, then the RDCn or read CAM command can be used to query a particular location (0—255) in a specific block using the LAR for the location address. The contents of the CAM and tag location are transferred to the holding registers, and then the time slot, stream plus control, and tag are returned (in sequence) from three consecutive IDR reads. The actual RDCn operation is one-cycle.

The converse of the RDCn is the FENn, or find entry command. It can be thought of as the first cycle of a BKCn command. Only time slot and stream plus control bits are necessary for identifying the location. The tag is not needed. The value returned to the IDR is the physical location of the entry in the CAM block, if it is found. If the entry is not found, then the underflow error bit in the SYSERR register will be set. FENn is a one-cycle command.

RSCn is the reset CAM command, and this renders all locations in one CAM block invalid. This can be considered a CLLn for all locations in the CAM. Two special resets are the RCH command, which resets only the holding registers, and the CI command, which resets all three CAM blocks and the holding registers. All resets are one-cycle.

2.3.3 H-Bus Access

There are 32 bidirectional pins available for accessing the H-Bus. The direction of the pins is selected by the CAM read and write bits. Data rates for the pins are selected in accordance with the H.100/H.110 specifications. Unassigned time slots on the H-bus are 3-stated. Details about rate selection are provided below. Two bits of the 13-bit address are used to select the CAM block as indicated in Figure 9. The remaining 11 bits plus a read/write bit form a comparand that is stored in a CAM location.

2 Architecture and Functional Description (continued)

2.3 H-Bus Section (continued)

2.3.4 L-Bus Access

The input and output of the CAM have the appropriate links to the local stream pins so that the H-Bus streams may be routed to and from the local bus streams. The LBS register (Section 2.2.4 LBS: Local Stream Control, 0x0C) programs the local stream rates even if accessed by the CAMs. To address the local bus CAM block, the two most significant address bits of the physical address are set to the appropriate values as described in Figure 9. The other bits form the comparand along with a read/write bit. When the CAM is outputting data to the local bus, it has priority over the local bus memory. In other words, if both the local bus and H-Bus access the same local stream and time slot, the H-Bus data memory will provide the actual data, not the local connection.

2.3.5 H-Bus Rate Selection and Connection Address Format

Operating rates are selected in a manner similar to the local side. Two registers, HSH and HSL, shown below, define the operation of the 32 streams. Again, SGx refers to stream groups: HSH holds SGh—SGe where SGh programs streams 28—31, SGg programs streams 24—27, SGf programs streams 20—23, and SGe programs streams 16—19. HSL holds SGd—SGa where SGd programs streams 12—15, SGc programs streams 8—11, SGb programs streams 4—7, and SGa programs streams 0—3.

SGh	SGg	SGf	SGe
SGd	SGc	SGb	SGa

SGn = 00, 3-state
SGn = 01, 2.048 Mbits/s
SGn = 10, 4.096 Mbits/s
SGn = 11, 8.192 Mbits/s

A quick summary:

The CAMs and the pipeline register files operate as connection memories. The key CAM operation is based on 11 bits of stream and time slot plus 1 bit of read/write in the CAM locations compared against the state counter which tracks the current stream and time slots (Section 2.2.5 State Counter Operation). Each H-Bus CAM is looking for matches on 16 of the 32 H-Bus streams, and the local CAM is looking for a match on 16 local inputs and 16 local outputs per time slot.

Thirteen bits are required to cover the 5120 possible time slots, but the MSB, LSB combination is used to determine which H-Bus CAM is accessed: even H-Bus (0, 0), odd H-Bus (0, 1). The local H-Bus is accessed by selecting the upper 2 MSBs, both equal to 1. The CAM address can be thought of as following this format:

CAM Select Field	Time-Slot Field	Stream Field
2 bits	7 bits	4 bits

This format is rate independent. The CAM select field is part of the address mode register (AMR) for CAM commands (Section 2.1.3 Address Mode Register and Section 2.3.2 CAM Operation and Commands). Programming examples for setting up connections can be found in Section 3.2 Basic Connections.

2.4 Clocking Section

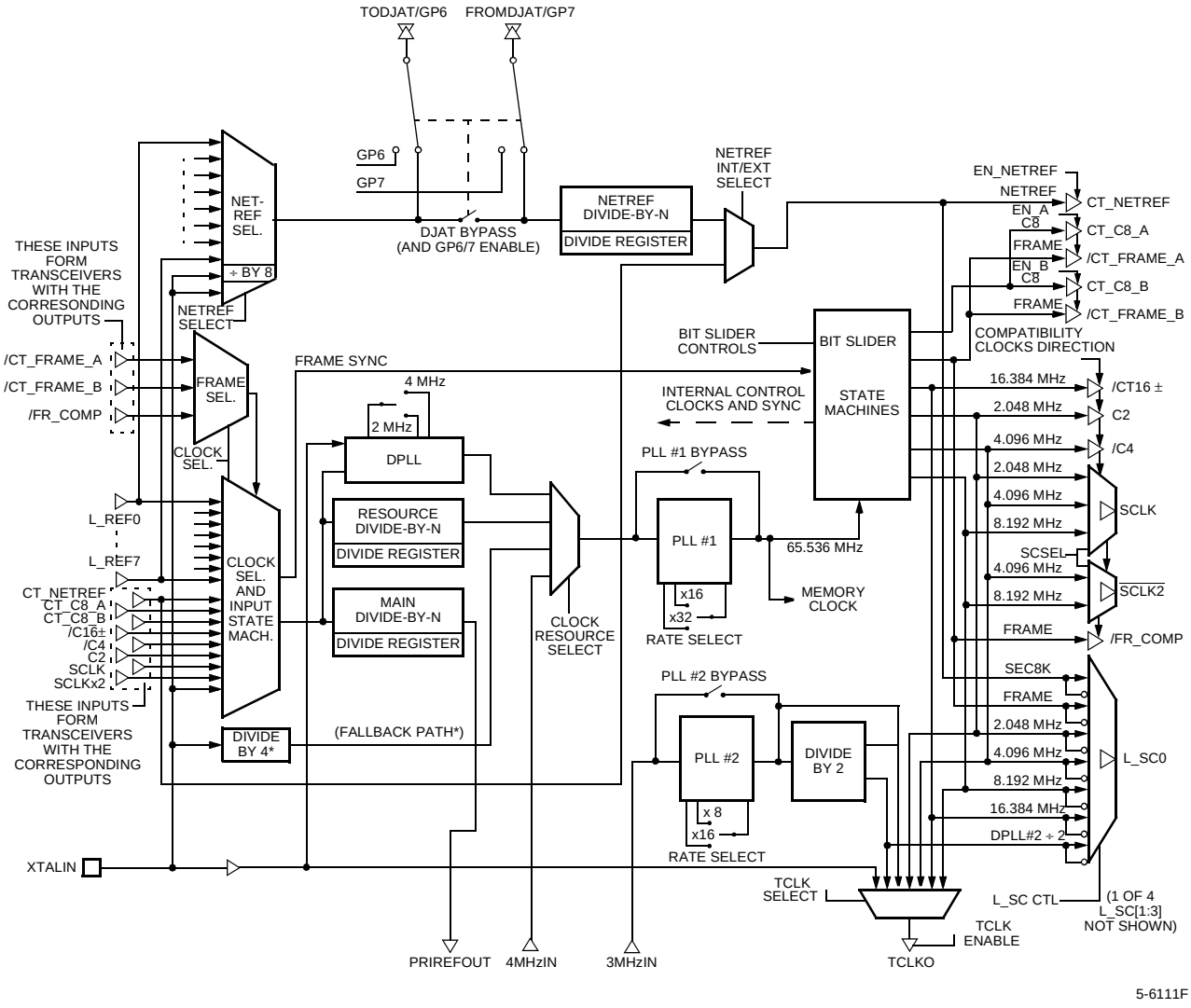
The clocking section performs several functions which are detailed in the following paragraphs. In general, when the T8100 is a bus master, it will have one or more companion devices which provide the basic clock extraction and jitter attenuation from a source (such as a trunk). As a slave, the T8100 can work independently of, or in conjunction with, external resources. Examples of different operating modes are provided in Appendix A. Refer to Figure 12 for a block diagram of the T8100 clocking section.

When the T8100 is used as a bus master, an input clock of a tolerance of ±32 ppm is required. This can come from several sources. For example:

- ±32 ppm crystal tolerance is the suggested value if either the DPLL is used or fallback to the oscillator is enabled while mastering the bus. Otherwise, a crystal with a lesser tolerance can be used.
- If a crystal is not used, a 16.384 MHz (±32 ppm tolerance or less) signal must be provided to the XTALIN pin, and XTALOUT should be left unconnected.
- The L_REF inputs can also be used and must conform to ±32 ppm in a bus master situation.

2 Architecture and Functional Description (continued)

2.4 Clocking Section (continued)



* The path for XTALIN **divide-by-4** is for fallback only.

Figure 12. Clocking Section

2 Architecture and Functional Description (continued)

2.4 Clocking Section (continued)

2.4.1 Clock and NETREF Selection

The inputs to the T8100 clocking come from three selectors. The clock selector and frame selector operate from a common set of selection options in register CKM (see Section 2.4.6 Clock Control Register Definitions for register details), where FRAMEA is selected along with clock C8A and FRAMEB is selected along with clock C8B. Typically, one of the local references (LREF[0:7]) will be selected when the T8100 is operating as a master, though the local oscillator is also available. As a slave, the most common selections will be one of the bus types. Each bus type has a state machine associated with it for determining the frame sync. All clock inputs are sampled to check for proper switching. If the expected clock edge does not occur, and there is no switching on CT_NETREF for 125 µs, a bit corresponding to the errant clock is set in the CLKERR register (see Section 2.6 Error Registers for more details). NETREF can be created from one of the local references or from the oscillator independent of the clock generation.

2.4.2 Dividers and Rate Multipliers

The clock and NETREF selections are routed to dividers*. In the case of NETREF, the divider is usually used to reduce a bit rate clock to 8 kHz, so the most common divisors will be 1, 193 (1.544 MHz/8 kHz), and 256 (2.048 MHz/8 kHz), although a full range of values (from 1—256) is possible. For the clock selector, the signal will most often be routed through the main divider when the T8100 is operating as a master or through the resource divider when operating as a slave. Both the main and resource dividers are fully programmable.

The ultimate destination for the main or resource divider is intended to be PLL #1. PLL #1 accepts either a 2.048 MHz or 4.096 MHz input and will rate multiply up to 65.536 MHz. The divisor of the main or resource dividers is chosen in conjunction with the rate select of the PLL, i.e., a divisor which generates a 4.096 MHz output and a rate selection of x16, or a divisor which generates a 2.048 MHz output and a rate selection of x32. This provides a great deal of flexibility in adapting to a variety of (external) clock adapters and jitter attenuators while acting as a master, as well as slaving to several bus types.

A digital PLL that can rate multiply to either 2.048 MHz or 4.096 MHz from an 8 kHz source in the absence of an external clock adapter is also provided. PLL #1 can be bypassed for diagnostic purposes or if an external clock adapter is used that provides a high-speed output (65.536 MHz). The input to the DPLL is for an 8 kHz signal only.

A second rate multiplier is provided for supporting T1 applications. It is optimized around either a 1.544 MHz or 3.088 MHz input rate which multiplies to 24.704 MHz and is then divided down to provide 50% duty cycle clocks of 12.352 MHz, though the direct 24.704 MHz is available as well. A bypass is provided so that an external clock can be buffered through the TCLK output. The internal oscillator or the various outputs derived from PLL #1 can also be selected for the TCLK output.

* If the A clocks have been selected as the clock source through the CKM register (described in Section 2.4.6 Clock Control Register Definitions), then the CT_C8A is the signal sent to the main and resource dividers; likewise, selecting B clocks results in sending CT_C8B; the *MVIP* selection sends /C4; the H-*MVIP* selection sends the recovered /C16 (derived from differential inputs); selecting SC2 sends $\overline{\text{SCLKX2}}$; and SC4/8 sends SCLK to the dividers.

2 Architecture and Functional Description (continued)

2.4 Clocking Section (continued)

2.4.3 State Machines

The purpose of the state machines is to generate internal control signals for the remainder of the T8100 circuitry and to provide all bus clocks when operating as a master. The state machines operate from the 65.536 MHz clock generated by PLL #1, and they are time referenced to the frame sync derived from the selected clock and frame inputs. As a master, the time sync is based on the T8100's own generated frame.

The dominant internal control signals are a noninverted 32.768 MHz clock, an inverted 16.384 MHz state clock, and a noninverted 122 ns wide sync pulse centered around the beginning of a frame. The memories are synchronized to the 65.536 MHz clock.

2.4.4 Bit Sliding (Frame Locking)

The T8100 generates its own frame signal based on the incoming clock and frame references and its generated clock signals. When slaving, it is sometimes necessary to align the edges of this generated frame signal to the incoming frame reference.

To accomplish this, the T8100 will compare the referenced frames with the current state of its clock state machine, and if the difference exceeds one 65.536 MHz clock cycle, the entire stream will have a fraction of a bit time removed from each frame; this is referred to as bit sliding. The process will repeat until the measurements fall within one clock cycle. The actual bit sliding will take place by reducing the generated frame by one 65.536 MHz clock cycle at the beginning of the frame. This means that the frame edges will phase-align at the rate of approximately 15.26 ns per frame. The maximum phase difference is slightly less than one frame or 124.985 µs. Thus, it will require approximately 8000 frames, or 1 second, to phase-align the frame. This is also mean time interval error (MTIE) compliant; performing phase adjustment of 162 ns per 1.326 ms of total sample time. Refer to the MTIE specifications document (ATT 62411).

The alternatives to bit sliding are snap alignment and no alignment. Snap alignment refers to an instantaneous phase alignment, i.e., a reset at the frame boundary. This mode is common to other devices. If no alignment is chosen, the T8100's generated frame is frequency-locked to the incoming frame sync, but not phase-aligned.

2.4.5 Clock Fallback

The following conditions must be met before fallback is initiated:

- Fallback must be enabled in register CKS.
- Failure of one or more of the clocks selected through the CKSEL bits in the CKM register.
- All clocks which comprise the selection from CKSEL must be unmasked in register CKW (see Section 2.6 Error Registers).

The T8100 contains a fallback register which enables a backup set of controls for the clock resources during a clock failure. In addition, a fallback state machine provides some basic decision-making for controlling some of the clock outputs when the feature is enabled. While slaving to the bus, the primary course of action in fallback is the swap between the A-clocks and B-clocks as the primary synchronization sources. A slave may become a master only under software control; i.e., there is no automatic promotion mechanism. As a master, the T8100 can detect its own failures and remove its clocks from the bus. If it detects a failure on the other main set (e.g., B master detects failures on the A master), then it can assume the role as the primary synchronization source by driving all compatibility clocks (H-*MVIP* and SC-Bus). Clock failures are flagged through the CLKERR1 and CLKERR2 registers (Section 2.6 Error Registers). Additional fallback details are discussed in relationship to the clock registers in the next section. The divide-by-4 block for XTALIN, shown in Figure 12, is used only for fallback. See Figure 13 for a diagram of the basic state machine which controls the A, B, and C (compatibility) clocks.

2 Architecture and Functional Description (continued)

2.4 Clocking Section (continued)

2.4.5 Clock Fallback (continued)

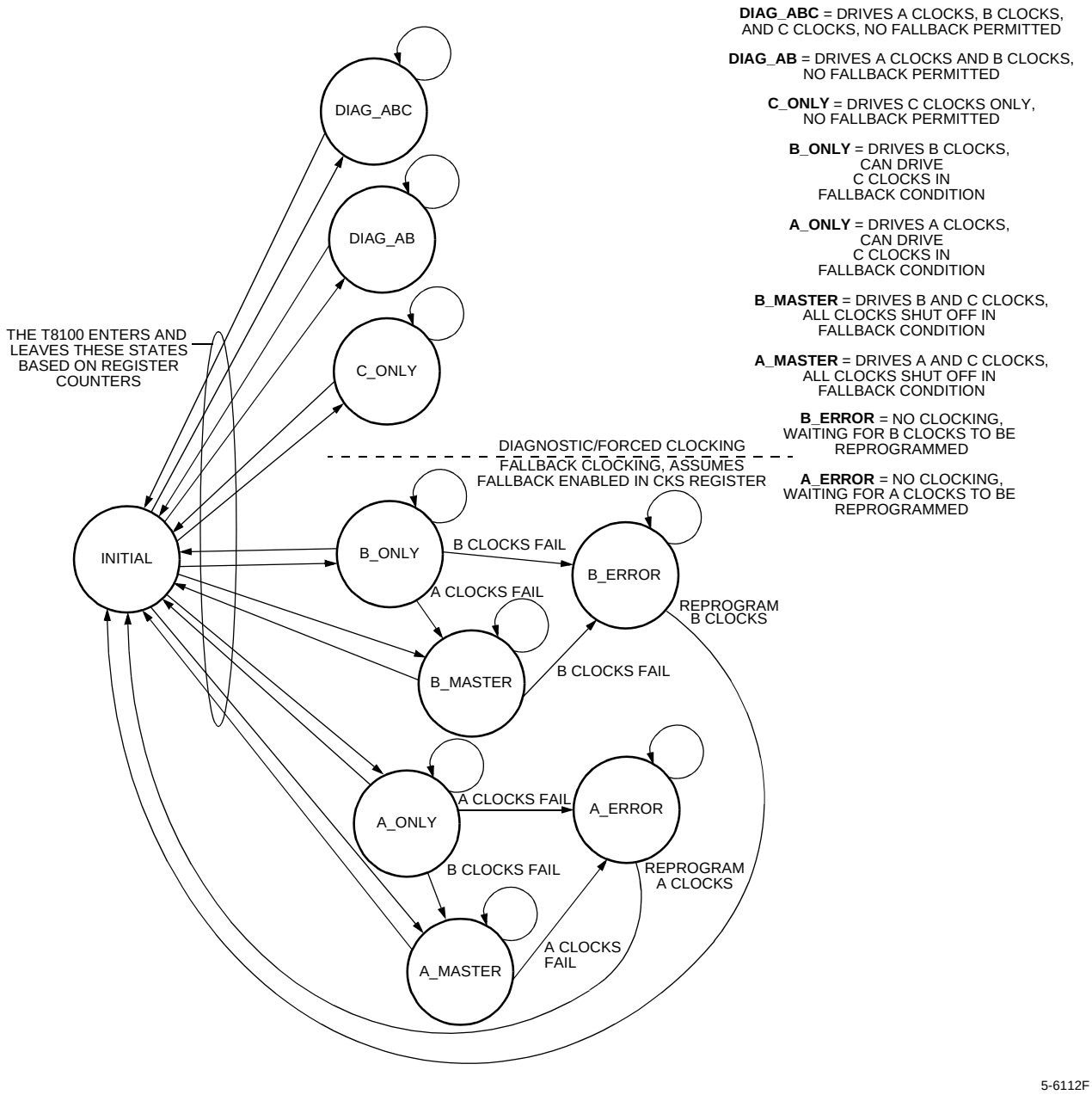


Figure 13. A, B, and C Clock Fallback State Diagram

2 Architecture and Functional Description (continued)

2.4 Clocking Section (continued)

2.4.6 Clock Control Register Definitions

Table 39. CKM: Clocks, Main Clock Selection, 0x00

The first register, 0x00, is the clock main (CKM) register. There are ten registers to control the various aspects of clocking.

REG	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CKM	—	PAE	PAS	CCD	CKI	CKSEL			

Symbol	Bit	Name/Description
PAE	7	Phase Alignment Enable. PAE = 0, Retains frequency lock without phase alignment PAE = 1, Enables phase alignment
PAS	6	Phase Alignment. PAS = 0, Phase alignment, snap PAS = 1, Phase alignment, slide
CCD	5	The CCD bit is the compatibility clock direction. This controls the I/O for the compatibility clocks /C16+/–, /C4, C2, SCLK, SCLKX2, and /FR_COMP (compatibility frame). The user can think of the CCD bit (in some respects) as a master/slave select for the compatibility clocks, though other registers require proper setup to establish true master or slave operation. The T8100 will assume control of this bit during a fallback if the previously designated compatibility clock master fails. CCD = 0, Slave, monitors compatibility signals CCD = 1, Master, drives compatibility signals **Note:** If bit 4 of the programmable clocks register, CKP, is low, then the state machines of the A clock and B clock will assume this is an MC-1 system and interpret the clocks as /C4(L/R) and FRAME(L/R). If this bit is high, then it interprets the clocks as C8(A/B) and FRAME(A/B).
CKI	4	CKI is used to invert the output of the clock selector, i.e., the signal which feeds the main divider, resource divider, and DPLL: CKI = 0, Normal CKI = 1, Invert
CKSEL	3—0	The decode for the clock selector (CKSEL) is illustrated below. These selections determine which input state machine is utilized*: CKSEL = 0000, Internal oscillator CKSEL = 0001, CT_NETREF CKSEL = 0010, A clocks (C8A & FRAMEA); ECTF or MC-1 CKSEL = 0011, B clocks (C8B & FRAMEB); ECTF or MC-1 CKSEL = 0100, *MVIP* CKSEL = 0101, H-*MVIP* CKSEL = 0110, SC-Bus, 2 MHz CKSEL = 0111, SC-Bus, 4 MHz or 8 MHz CKSEL = 1000—1111 Selects local references 0—7

* Selecting A clocks synchronizes the T8100 to CT_C8A and /CT_FRAMEA; selecting B clocks synchronizes the T8100 to CT_C8B and /CT_FRAMEB; *MVIP* uses /C4, C2, and /FR_COMP; H-*MVIP* uses /C16+/–, /C4, C2, and /FR_COMP; SC2 uses SCLKX2 and /FR_COMP; SC4/8 requires SCLK, SCLKX2, and /FR_COMP. MC-1 fallback clocks use the same inputs and state machine as the A clocks and B clocks with an inversion selected from register CKP. A pictorial view of the various clocks may be seen in Section 4.6.1 Clock Alignment.

2 Architecture and Functional Description (continued)

2.4 Clocking Section (continued)

2.4.6 Clock Control Register Definitions (continued)

Table 40. CKN: Clocks, NETREF Selections, 0x01

Clock register 0x01 is CKN, the CT_NETREF select register. This register selects features for generating and routing the CT_NETREF signal.

REG	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CKN	—	NOE	NIO	NDB	NRI	NRSEL			

Symbol	Bit	Name/Description
NOE	7	The NOE bit enables the NETREF output: NOE = 0, CT_NETREF output disabled (3-state) NOE = 1, CT_NETREF output enabled (NIO must be low)
NIO	6	The NIO bit controls the internal/external selector. It selects either the NETREF divider for outputs or the NETREF input. Since the latter is used for routing NETREF to the local clock outputs, it will automatically prevent the NETREF output from being enabled: NIO = 0, Select NETREF divider, i.e., NETREF as output NIO = 1, Select NETREF input (disables NETREF output) **Note:** When the NIO bit is high, general-purpose register (GPR), bits 6 and 7 are available. (The GPR is discussed in Section 2.5.2 General-Purpose Register.)
NDB	5	NDB = 0, TODJAT pin comes from NETREF selector, and FROMDJAT pin goes to NETREF divider NDB = 1, NETREF selector goes directly to NETREF divider
NRI	4	NRI inverts the output of the NETREF selector. NRI = 0, Normal NRI = 1, Invert
NRSEL	3—0	The NRSEL is similar to CKSEL but with fewer choices: NRSEL = 0000, Internal oscillator divided by 8 NRSEL = 0001, Internal oscillator NRSEL = 0010—0111, (Reserved) NRSEL = 1000—1111, Local references 0—7

2 Architecture and Functional Description (continued)

2.4 Clocking Section (continued)

2.4.6 Clock Control Register Definitions (continued)

Table 41. CKP: Clocks, Programmable Outputs, 0x02

Clock register 0x02, CKP, is the programmed clocks register. It is used for programming the CT_C8 clocks and enabling its outputs. It is also used to program the TCLK selector. CT_C8 may be operated as either 8 MHz (normal or inverted) or 4 MHz (normal or inverted). The register format is as follows:

REG	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CKP	—	PTS			C8IS	CAE	CBE	C8C4	CFW

Symbol	Bit	Name/Description
PTS	7—5	The three PTS bits select the output sent to the TCLK. This output is intended to be used for driving framers. PTS = 000, 3-state PTS = 001, Oscillator, buffered output PTS = 010, PLL #2, direct output PTS = 011, PLL #2, output divided by 2 PTS = 100, 2.048 MHz from state machines PTS = 101, 4.096 MHz from state machines PTS = 110, 8.192 MHz from state machines PTS = 111, 16.384 MHz from state machines
C8IS	4	C8IS is used to invert the synchronization on C8A and C8B when they are selected for input. The C8 and FRAME signals, which are also generated internally, are routed to both the CT_C8A and /CT_FRAMEA and to the CT_C8B and /CT_FRAMEB. The CAE and CBE pins enable these output pairs independently. The C8C4 pin selects 8.192 MHz or 4.096 MHz signals to be output on C8A and C8B (for supporting for either ECTF or MC-1* applications). CFW selects the output width of the compatibility frame. C8IS = 0, MC-1 (A and B clocks inputs interpreted as /C4 with /FRAME) C8IS = 1, ECTF (A and B clocks inputs interpreted as C8 with /FRAME)
CAE	3	CAE = 0, Disable CT_C8A & /CT_FRAMEA outputs CAE = 1, Enable CT_C8A & /CT_FRAMEA outputs (The T8100 will automatically disable these on an A clock failure.)
CBE	2	CBE = 0, Disable CT_C8B & /CT_FRAMEB outputs CBE = 1, Enable CT_C8B & /CT_FRAMEB outputs (The T8100 will automatically disable these on a B clock failure.)
C8C4	1	C8C4 = 0, Inverted 4.096 MHz (MC-1 output mode) C8C4 = 1, Noninverted 8.192 MHz (ECTF output mode)
CFW	0	CFW = 0, (Reserved) CFW = 1, (Reserved)

* MC-1 is a multichassis communication standard based on *MVIP*. The T8100 supports this standard.

2 Architecture and Functional Description (continued)

2.4 Clocking Section (continued)

2.4.6 Clock Control Register Definitions (continued)

Table 42. CKR: Clocks, Resource Selection, 0x03

Clock register 0x03, CKR, is the clock resources register. It is used for selecting and programming miscellaneous internal resources, the two PLLs, the DPLL, and the clock resource selector. It is also used to program the SCLK/SCLKX2 clock outputs. The register format is as follows:

REG	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CKR	—	CRS		P1B	P1R	P2B	P2R	SCS	

Symbol	Bit	Name/Description
CRS	7—6	The CRS[7:6] bits are used to select the input to PLL #1. CRS = 00, External input (through the 4 MHz In pin) CRS = 01, Resource divider CRS = 10, DPLL @ 2.048 MHz CRS = 11, DPLL @ 4.096 MHz
P1B	5	P1B and P1R control PLL #1. P1B = 0, Normal PLL #1 operation P1B = 1, Bypass PLL #1
P1R	4	P1R = 0, PLL #1 rate multiplier = 16 P1R = 1, PLL #1 rate multiplier = 32
P2B	3	P2B and P2R control PLL #2. P2B = 0, Normal PLL #2 operation P2B = 1, Bypass PLL #2
P2R	2	P2R = 0, PLL #2 rate multiplier = 8 P2R = 1, PLL #2 rate multiplier = 16
SCS	1—0	The SCS[1:0] bits are used to program the outgoing SC-Bus compatibility signals. SCS = 00, SC-Bus outputs 3-stated SCS = 01, SCLK @ 2.048 MHz, SCLKX2 @ 4.096 MHz SCS = 10, SCLK @ 4.096 MHz, SCLKX2 @ 8.192 MHz SCS = 11, SCLK @ 8.192 MHz, SCLKX2 @ phase shifted 8.192 MHz

2 Architecture and Functional Description (continued)

2.4 Clocking Section (continued)

2.4.6 Clock Control Register Definitions (continued)

Table 43. CKS: Clocks, Secondary (Fallback) Selection, 0x04

Clock register 0x04 is CKS, the secondary clock selection register. This is also referred to as fallback. Along with programming the CKS register, CKW and CKS should be programmed last. The register is defined as follows:

REG	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CKS	—	FRS		FTS		FF	FCSEL		

Symbol	Bit	Name/Description
FRS	7—6	FRS provides an alternate clock resource selection. FTS determines the basic fallback mode. FF forces the use of the FRS, FTS, and FCSEL. FCSEL is used to select an alternate synchronization source. FRS forces the clock resource selector to choose a new source for PLL #1. FRS = 00, External input (through the 4 MHz In pin) FRS = 01, Resource divider FRS = 10, DPLL @ 2.048 MHz FRS = 11, DPLL @ 4.096 MHz **Note:** The decode is the same as that of the CRS bits (in the clock resource register, CKR).
FTS	5—4	For fallback type select, the two FTS bits are used to enable the automatic fallback. These work in conjunction with the various clocks as described in Section 2.4.5 Clock Fallback. If the C8 input select (C8IS of the CKP register above) is low, then the T8100 is assumed to be in an MC-1 system. Thus, the A/B clocks can be interpreted as /C4L (or /C4R) for C8A and /C4R (or /C4L) for C8B. FTS = 00, Fallback from main clock to the oscillator divided by 4* when main clock fails. (Main clock determined by CKSEL bits of the CKM register.) FTS = 01, Fallback disabled; this is not recommended for operation, it is intended for initialization and diagnostic purposes only. FTS = 10, Fallback from main selection to secondary source (FCSEL). FTS = 11, Fallback from A or B clock (ECTF/MC-1) to secondary; this also enables the fallback state machine. When one of the selected bits goes high in the CLKERR register (i.e., clock failure, see Section 2.6 Error Registers), then clocks are changed to the selection indicated by FCSEL, the A or B clocks are disabled (if applicable), and the compatibility clocks are either driven or disabled (if applicable). Note that the change is “sticky”; once the fallback has occurred, it will stay in its new state until the system is reprogrammed. Clearing the CLKERR registers through the MCR (Section 2.1.2 Master Control and Status Register) clears the fallback condition. A bit in the SYSERR register will also note when a fallback has occurred.
FF	3	FF is used as a test of the fallback, but can also be used as a software-initiated fallback. FF = 0, Normal operation FF = 1, Force use of secondary (fallback) resources
FCSEL	2—0	The FCSEL choices are a subset of the CKSEL values from the CKM register above. The list is presented below: FCSEL = 000, Internal oscillator divided by 4 FCSEL = 001, Internal oscillator FCSEL = 010, A clocks (C8A & FRAMEA); ECTF or MC-1 FCSEL = 011, B clocks (C8B & FRAMEB); ECTF or MC-1 FCSEL = 100, NETREF FCSEL = 101—111, Selects local references 1—3

* This bypasses the CRS/FRS multiplexer and is the default condition. It is equivalent to letting the T8100 free run on a clock failure. It assumes PLL #1 has been set for x16. If PLL #1 is set for x32, then use FCSEL = 8 kHz local reference, FRS = 10, and FTS = 10.

2 Architecture and Functional Description (continued)

2.4 Clocking Section (continued)

2.4.6 Clock Control Register Definitions (continued)

Table 44. CK32 and CK10: Clocks, Locals 3, 2, 1, and 0, 0x05 and 0x06

Registers 0x05 and 0x06 set up L_SC0, 1, 2, & 3. The outputs L_SC[3:0] can be used as bit clocks for the local streams or as a secondary NETREF. These are programmed using CK32 and CK10, which are presented below:

REG	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CK32	—	LSC3				LSC2			
CK10	—	LSC1				LSC0			

Register	Bit	Symbol	Name/Description
CK32	7—4	LSC3	LSCn = 0000, Output low LSCn = 0001, Local frame LSCn = 0010, NETREF (Sec8K) LSCn = 0011, PLL #2 ≠ 2 LSCn = 0100, 2.048 MHz LSCn = 0101, 4.096 MHz LSCn = 0110, 8.192 MHz LSCn = 0111, 16.384 MHz LSCn = 1000, Output high LSCn = 1001, Local frame, inverted LSCn = 1010, NETREF, inverted LSCn = 1011, PLL #2 ≠ 2, inverted LSCn = 1100, 2.048 MHz, inverted LSCn = 1101, 4.096 MHz, inverted LSCn = 1110, 8.192 MHz, inverted LSCn = 1111, 16.384 MHz, inverted
CK32	3—0	LSC2	
CK10	7—4	LSC1	
CK10	3—0	LSC0	

2.4.7 CKMD, CKND, CKRD: Clocks, Main, NETREF, Resource Dividers, 0x07, 0x08, and 0x09

The remaining clock registers are used to program the three dividers. The main divider is programmed through CKMD; the NETREF divider, through CKND; and the resource divider, through CKRD. The dividers are fully programmable, but only binary divides (1, 2, 4, 8, etc.) and divide by 193 produce 50% duty-cycle outputs. All other divisors will produce a pulse equal to one-half of a (selected) clock cycle in width.

0x00 => Divide by 1 (bypass divider)
0x01 => Divide by 2
:
0xC0 => Divide by 193
:
0xFF => Divide by 256

In general, the register value is the binary equivalent of the divisor-minus-one; e.g., an intended divisor of 193 is reduced by 1 to 192, so the register is loaded with the binary equivalent of 192 which is 0xC0.

2.5 Interface Section

2.5.1 Microprocessor Interface

The grouping of the read, write, chip select, and address latch enable signals, along with the data bus and the address bus, permit access to the T8100 using *Intel* nonmultiplexed interface (ALE = low), *Motorola* nonmultiplexed interface (ALE = high), or *Intel* multiplexed interface (ALE = active). ALE controls the microprocessor mode. All control and status registers and data and connection memory accesses are controlled through this interface. All accesses are indirect, following the pin descriptions in Table 1 and Table 2. Programming examples and a more detailed discussion of the indirect accesses can be found in Section 3 Using the T8100.

2 Architecture and Functional Description (continued)

2.5 Interface Section (continued)

2.5.2 General-Purpose Register

A simple, general-purpose I/O register is available. The GPR has eight dedicated pins to the T8100. A write to the register forces it to operate as an output. It remains as an output until a read from the register is performed (which 3-states the output). The register powers up in the input state with a cleared register. The GPR corresponds with I/O pins GP[0:7]. GP6 and GP7 are unavailable if bit 5 of register CKN is low (see Section 2.4.6 Clock Control Register Definitions).

2.5.3 Framing Groups

Two groups of frame pulses are available. Each frame group consists of 12 lines which are enabled sequentially after a programmed starting point. They are denoted as group A and group B. This section describes framing group A. Framing group B is made up of similar registers. Each frame group is controlled by a pair of registers: FRHA and FRLA control the spacing of the 12 frame pulses, their pulse width, polarity, and the offset of the first pulse from the frame boundary.

Table 45. FRHA, Frame Group A High Address and Control, 0x21

REG	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FRHA	—	Rate		Type		FAI	Hi Start		

Symbol	Bit	Name/Description
Rate	7—6	Rate = 00, Frame group disabled, 3-state Rate = 01, 2.048 Mbits/s Rate = 10, 4.096 Mbits/s Rate = 11, 8.192 Mbits/s
Type	5—4	Type = 00, Bit-wide pulse Type = 01, Double bit-wide pulse Type = 10, Byte-wide pulse Type = 11, Double byte-wide pulse
FAI	3	FAI = 0, Normal pulse FAI = 1, Inverted pulse
Hi Start	2—0	Hi Start = Upper 3 bits of group start address or programmed output

Table 46. FRHB, Frame Group B High Address and Control, 0x23

REG	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FRHB	—	Rate		Type		FAI	Hi Start		

Symbol	Bit	Name/Description
Rate	7—6	Rate = 00, Frame group disabled, 3-state Rate = 01, 2.048 Mbits/s Rate = 10, 4.096 Mbits/s Rate = 11, 8.192 Mbits/s
Type	5—4	Type = 00, Bit-wide pulse Type = 01, Double bit-wide pulse Type = 10, Byte-wide pulse Type = 11, Double byte-wide pulse
FAI	3	FAI = 0, Normal pulse FAI = 1, Inverted pulse
Hi Start	2—0	Hi Start = Upper 3 bits of group start address

2 Architecture and Functional Description (continued)

2.5 Interface Section (continued)

2.5.3 Framing Groups (continued)

The 12 outputs of the frame group are pulsed in sequence, one every 8 bit times, where the bit time is set by the rate option. Thus, the rate option controls the spacing between output pulses. The pulse width is set by the type option, and the pulse polarity is set by the FAI bit. Note that double byte-wide types will produce overlapping pulses.

The remaining bits (3 hi-start bits in FRHA and 8 bits of FRHB) make up an 11-bit start address that sets the offset of the group's first output (pin FGA0) relative to the frame boundary. The offset is in increments of 61 ns (1/16.384 MHz). Thus, 2^{11} values corresponding to the 11-bit start address allow programming offsets from 0 ns to 125 µs. Notice that the resolution is less than 1 bit. For example, if the frame group clock is programmed to 2.048 MHz, the resolution is 0.125 of a bit.

The frame boundary, shown in Figure 19 through Figure 21, is the point where /CT_FRAME is low and CT_C8 is starting its low-to-high transition.

At zero offset, the rising edge of the first frame group output is coincident with the rising edge of the 8 MHz, 4 MHz, and 2 MHz of the L_SC[3:0] clocks that occur in the center of the CT_FRAME. This defines the start of the frame, and the start of the first bit of the first time slot on both the CT bus and local input and local output buses.

In addition to sequenced pulses, the frame groups can be used as simple programmed output registers. When group A is used as a programmed output, the bits are sent from the FRLA [0x20] and FRHA [0x21] registers. Bits [0:7] of the programmed output come from bits [0:7] of FRLA [0x20]. Bits [8:10] of the programmed output come from the high start (bits [0:2]) of FRHA [0x21], and bit 11 of the programmed output comes from the FAI bit (bit 3) of FRHA [0x21]. When group B is used as a programmed output, bits 0:7 of the output come from bits 0:7 of separate register FRPL [0x24], and bits [8:11] of the output come from bits 0:3 of another register FRPH [0x25]. The upper nibble of FRPH [0x25] also has output routing functions associated with it. Register FRPH [0x25] is illustrated below; see Figure 14 for a diagram of the selection options.

Table 47. FRPH: Frame Group B, Programmed Output, High, 0x25

REG	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FRPH	—	FAO		X	FBO	Hi Prog			

Symbol	Bit	Name/Description
FAO	7—6	FAO = 00, Frame group A bits [0:11] on output pins [0:11] FAO = 01, Programmed output A bits [0:11] on output pins [0:11] FAO = 10, Frame group A bits [0:5] on output pins [0:5], and frame group B bits [0:5] on output pins [6:11] FAO = 11, Programmed output A bits [0:5] on output pins [0:5], and frame group B bits [0:5] on output pins [6:11]
X	5	X (Reserved)
FBO	4	FBO = 0, Frame group B routed to group B output pins FBO = 1, Programmed output B routed to group B output pins
Hi Prog	3—0	High Prog = Upper 4 bits of programmed output B **Note:** In the programmed output mode, the rate must not equal 00; otherwise, the outputs corresponding to the group bits are 3-stated; the rate will have no effect other than enabling the mode. Type bits have no effect in the programmed modes.

2 Architecture and Functional Description (continued)

2.5 Interface Section (continued)

2.5.3 Framing Groups (continued)

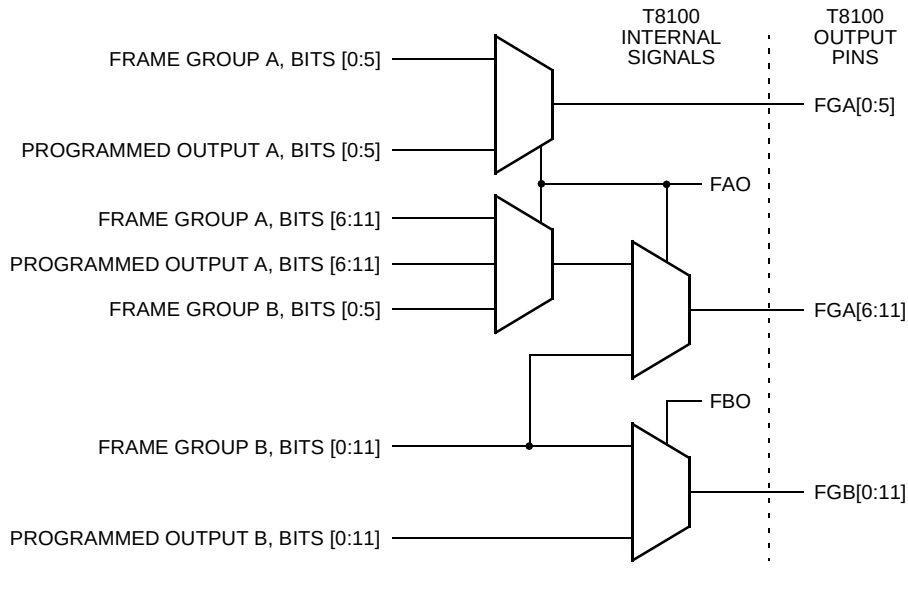


Figure 14. Frame Group Output Options

2 Architecture and Functional Description (continued)

2.6 Error Registers

Four error registers are present in the T8100:

- CLKERR1 [0x28]
- CLKERR2 [0x29]
- CKW [0x2B]
- SYSERR [0x2A]

When programming the clock registers, writing to CKW and CKS should be programmed last.

These are the clock error, watchdog enable, and system error registers. The CLKERR1 register is used to indicate failing clocks, and the CLKERR2 indicates whether the failure is permanent or transient in nature. If the clocks fail, i.e., disappear or momentarily drop out, then corresponding bits in both registers will be set. If the clock is reestablished, i.e., a transient error, then the T bit(s) will clear, but the E bit(s) will remain set. All of the E bits are ORed together and drive the CLKERR pin.

The clocks listed above are sampled by the 16.384 MHz internal clock. Effectively, each clock has a watchdog. If the clock is switching, the watchdog clears. If the clocks stop, then the watchdog sets the appropriate E and T bits. If the clock is reestablished, then the E bits remain stuck, but the T bits clear with the watchdog. Since fallback is triggered on the E bits, a transient clock can force a fallback.

Table 48. CLKERR1 and CLKERR2: Error Indicator and Current Status, 0x28 and 0x29

Table 48 describes both CLKERR1 and CLKERR2:

Name	Bit	Name/Description
CAE CAT	7	CA => Reports failures on CT_C8A or /CT_FRAMEA
CBE CBT	6	CB => Reports failures on CT_C8B or /CT_FRAMEB
CFE CFT	5	CF => Reports failures on /FR_COMP
C16E C16T	4	C16 => Reports failures on /C16+ or /C16–
C42E C42T	3	C42 => Reports failures on /C4 or C2
SCE SCT	2	SC => Reports failures on SCLK
SC2E SC2T	1	SC2 => Reports failures on $\overline{\text{SCLKX2}}$
NRE NRT	0	NR => Reports failures on CT_NETREF

The CKW register works in conjunction with the two registers above and with the clock circuitry. It is used to enable the watchdogs for the clock lines. CKW uses the same mapping as CLKERR1 and CLKERR2, so, for example, a high in bit 7 will enable the watchdogs for CT_C8A and /CT_FRAMEA. CKW functions as a masking register for CLKERR1 and CLKERR2. If the appropriate bit is not set, then a failing clock will not be reported.

The SYSERR register is shown below, the bits are ORed together with the CLKERR1 bits which, in turn, drives the SYSERR pin. The SYSERR bits are sticky as are the CLKERR1 bits so they must be reset by clearing the register by setting a bit in the MCR (Section 2.1 Register/Memory Maps).

Table 49. SYSERR: System Error Register, 0x2A

Table 49 describes SYSERR:

Name	Bit	Name/Description
CUE	7	CUE => Even CAM underflow, set by an unmatched comparison
CUO	6	CUO => Odd CAM underflow, set by an unmatched comparison
CUL	5	CUL => Local CAM underflow, set by an unmatched comparison
COE	4	COE => Even CAM overflow, set by a write to a full CAM
COO	3	COO => Odd CAM overflow, set by a write to a full CAM
COL	2	COL => Local CAM overflow, set by a write to a full CAM
(RES)	1	RES Reserved bit position
FBE	0	FBE => Fallback enabled, status which indicates that a clock error has occurred and fallback operations are in effect*.

* This error bit is selective. It will only flag an error if the clocks that fail correspond to the selected clock mode. For example, if *MVIP* mode is selected (in register CKM), the proper fallback mode has been set (in register CKS), and the *MVIP* clocks are not masked (register CKW, above), then FBE will go high when a failure is detected on /FR_COMPn, C2, or /C4. Thus, unmasked, failing non-*MVIP* clocks will be flagged in the CLKERR1 and CLKERR2 registers but will not set the FBE flag in SYSERR.

2 Architecture and Functional Description (continued)

2.7 The JTAG Test Access Port

2.7.1 Overview of the JTAG Architecture

Tap
A 5-pin test access port, consisting of input pins TCK, TMS, TDI, TDO, and TRST, provides the standard interface to the test logic. TRST is an active-low signal that resets the circuit.

TAP Controller
The TAP controller implements the finite state machine which controls the operation of the test logic as defined by the standard. The TMS input value sampled on the rising edge of TCK controls the state transitions. The state diagram underlying the TAP controller is shown below.

Instruction Register (JIR)
A 3-bit scannable JTAG instruction register that communicates data or commands between the TAP and the T8100 during test or HDS operations.

Boundary-Scan Register (JBSR)
A 211-bit JTAG boundary-scan register containing one scannable register cell for every I/O pin and every 3-state enable signal of the device, as defined by the standard. JBSR can capture from parallel inputs or update into parallel outputs for every cell in the scan path. JBSR may be configured into three standard modes of operation (EXTEST, INTEST, and SAMPLE) by scanning the proper instruction code into the instruction register (JIR). An in-depth treatment of the boundary-scan register, its physical structure, and its different cell types is given in Table 51.

Bypass Register (JBPR)
A 1-bit long JTAG bypass register to bypass the boundary-scan path of nontargeted devices in board environments as defined by the standard.

2.7.2 Overview of the JTAG Instructions

The JTAG block supports the public instructions as shown in the table below.

Table 50. T8100 JTAG Instruction Set

Instruction Mnemonics	Instruction Codes	Public/Private	Mode	Description
EXTEST	000	Public	—	Select B-S register in extest mode
SAMPLE	001	Public	—	Select B-S register in sample mode
Reserved	010	—	—	—
Reserved	011	—	—	—
Reserved	100	—	—	—
Reserved	101	—	—	—
Reserved	110	—	—	—
BYPASS	111	Public	—	Select BYPASS register

2 Architecture and Functional Description (continued)

2.7 The JTAG Test Access Port (continued)

2.7.3 Elements of JTAG Logic

Table 51. T8100 JTAG Scan Register

Cell	Type	Signal Name/Function
66	I	CK_3MHZIN
67	O	SYSERR
68	O	CLKERR
0	CC	Controls cells 67:68
69—76	Bdir	D[0:7]
1	CC	Controls cells 69:76
77	I	RESTN
78	O	RDY
79	I	WRN
80	I	RDN
81	I	CSN
82	I	ALE
83	I	A0
84	I	A1
85—88	O	L_SC[0:3]
44	CC	Controls cells 85:88
89—96	I	L_REF[0:7]
97	I	CK_4MHZIN
98	O	PRIREFOUT
45	CC	Controls cell 98
99	O	TESTOUT1
100	O	REFCLK1O
46	CC	Controls cells 99, 100
101	Bdir	FROMDJAT
43	CC	Controls cell 101
102	Bdir	TODJAT
42	CC	Controls cell 102
103—108	Bdir	GP[5:0]
41	CC	Controls cells 103—108
109—120	O	FGB[11:0]
63	CC	Controls cells 109—120
121—132	O	FGA[11:0]
64	CC	Controls cells 121—132
133	Bdir	C16N_MINUSA
134	Bdir	C16N_PLUSA
135	Bdir	C4N
136	Bdir	C2
5	CC	Controls cells 133—136
137	Bdir	SCLKX2NA
7	CC	Controls cell 137
138	Bdir	SCLKA
6	CC	Controls cell 138
139	Bdir	CT_C8_BA
140	Bdir	CT_FRAME_BNA
3	CC	Controls cells 139—140
141	Bdir	FRN_COMPA
4	CC	Controls cell 141
142	Bdir	CT_NETREF
8	CC	Controls cell 142
143	Bdir	CT_C8_AA
144	Bdir	CT_FRAME_ANA
2	CC	Controls cells 143—144
145—176	Bdir	CT_D[0:31]
9—40	CC	Controls cells 145—176
177—192	O	LDO[0:15]
47—62	CC	Controls cells 177—192
193	O	XCS
0	CC	Controls cell 193
194—209	I	LDI[0:15]
210	O	PMCTCLKO
65	CC	Controls cell 65

2 Architecture and Functional Description (continued)

2.8 Testing and Diagnostics

There are several testing operations available for the T8100:

- JTAG
- Forced output testing
- Onboard diagnostics

During manufacturing, the T8100 is run through standard functional and electrical testing.

2.8.1 Testing Operations

JTAG is used primarily to test the array portion of the T8100. It will not provide coverage for the CAMs, register files, SRAMs, or PLLs. In JTAG, the manufacturer provides a drop-in control block and scan-chain which ties internal points to registers on the periphery of the T8100, which are, in turn, tied to the I/O pins. Serial bit patterns are shifted into the T8100 through the TDI pin, and the results can be observed at the I/O and at a corresponding JTAG serial output, TDO. Since this JTAG conforms to the JTAG standard, the TDI and TDO can be linked to the JTAGs of other devices for systemic testing. The TTS pin must be low for JTAG operations to work. The TTS pin has an internal pull-down resistor that defaults the T8100 to JTAG operations.

In forced output testing, the outputs are set to a particular state to measure their dc parameters. This can also be used in applications for board-level diagnostics. Forced output testing is selected by setting the TTS (test type select) pin high. In this mode, the JTAG clock pin, TCK, will act as an input pin. All outputs will be enabled, and each output provides either an inverting or normal response to the input pin. Adjacent pins alternate inverting and normal function (i.e., a checkerboard pattern).

2.8.2 Diagnostics

The T8100 has onboard diagnostic modes for testing the frame groups, SRAMs and CAMs, and some internal structures. These are intended for testing some of the T8100 resources while it is in an application environment (rather than a manufacturing test environment).

The diagnostics allow critical internal nodes to be output through the frame groups, or to have the frame groups operated in special cyclical manner, or to provide automatic filling of all memories (including CAMs) with one of four selected patterns. The diagnostics are activated and selected using three registers: DIAG1 [0x30], DIAG2 [0x31], or DIAG3 [0x32].

DIAG1 is used to select the frame group pins as either monitors for internal nodes or normal operation (i.e., as frame groups or programmed outputs). DIAG1 is also used to control the memory fill diagnostic.

DIAG2 and DIAG3 modify the normal operation of the frame groups and the main state counter. Normally, the frame groups begin their cascade sequence when the state counter (i.e., the frame-synchronized master counter of the T8100) reaches a value equal to the frame group's starting address. DIAG2 and DIAG3 allow the state counter to be modified for one of two different tests.

2 Architecture and Functional Description (continued)

2.8 Testing and Diagnostics (continued)

2.8.2 Diagnostics (continued)

The three registers are presented in order below:

DFA	DFB	DMF	DMP	DMD

DFC	DSB	DXF	(Res.)	DSE	DSH

DSL

The register fields are interpreted as follows:

DFA—Diagnostics, Frame Pin Selects, Group A:
DFn = 00, Normal operation
DFn = 01, State counter bits [10:0] routed to frame group pins [10:0], pin 11 = L
DFn = 10, Even CAM hit routed to pin 11, pin 10 has odd CAM hit, pins [9:0] have local data memory address
DFn = 11, Pin 11 gets CUE error bit, pin 10 gets CUO error bit, pin 9 gets CUL error bit, pin 8 gets COE error bit, pins [5:0] get page pointers—8 MHz read, 8 MHz write, 4 MHz read, 4 MHz write, 2 MHz read, and 2 MHz write

DFB—Diagnostics, Frame Pin Selects, Group B:
DFn = 00, Normal operation
DFn = 01, State counter bits [10:0] routed to frame group pins [10:0], pin 11 = L
DFn = 10, CAM state register [1:0] indicating four substates, routed to pins [11:10], and local connection memory address routed to pins [9:0]
DFn = 11, Pin 11 gets local CAM hit flag, and pins [10:0] get CAM state counter

DMF—Diagnostics, Memory, Fill Test Enable:
DMF = 0, Normal operation
DMF = 1, Fill all memories with the pattern selected by DMP

DMP—Diagnostics, Memory, Fill Test Pattern Select:
DMP = 00, Checkerboard 0—even locations get 0x55, odd locations get 0xAA
DMP = 01, Checkerboard 1—even locations get 0xAA, odd locations get 0x55
DMP = 10, Data locations equal address bits [7:0] (CAMs are filled with their physical address)
DMP = 11, Data locations equal inverted address bits [7:0]

DMD—Diagnostics, Memory, Done Indicator:
This is a status bit which indicates that the chosen memory pattern has been written to all locations. Additional writes to the memory are disabled and reads are enabled. This condition remains until the user clears this bit.

DFC—Diagnostics, Frame Groups Cycle Test Mode:
DFC = 0, Normal operation
DFC = 1, Cycle test mode enabled; forces the frame groups to constantly cycle without waiting for a frame signal to synchronize the start.

DSB—Diagnostics, State Counter, Break Carry Bits:
DSB = 0, Normal operation
DSB = 1, Breaks the carry bits between the subsections of the state counter so that the state counter is operating as three counters running in parallel. (This can be viewed on the frame pins using the DFn = 01 selection described above.) Status counter bits [0:3] and [4:7] run as modulo-16 counters, and bits [8:10] run as a modulo-8 counter.

DXF—Diagnostics, External Frame Input:
DXF = 0, Normal operation
DXF = 1, Forces /FR_COMP to act as a direct input signal for T8100 framing. This effectively bypasses the internally generated frame signal. The user is again cautioned since the external frame can operate asynchronously to the generated clocks if care is not taken.

DSE—Diagnostics, State Counter, Enable Parallel Load:
DSE = 0, Normal operation
DSE = 1, Forces the state counter to load the value held in DSH and DSL and continuously cycle as a modulo-n counter where the n value is determined by (DSH and DSL). With the DSE pin high, the state counter is no longer synchronized to the frame signal.

DSH—Diagnostics, State Counter, High Bits of Parallel Load:
DSH = State counter bits [10:8]

DSL—Diagnostics, State Counter, Low Bits of Parallel Load:
DSL = State counter bits [7:0]

3 Using the T8100

3.1 Resets

3.1.1 Hardware Reset

A hardware reset utilizes the (active-low) $\overline{\text{RESET}}$ pin. On activation, it immediately places all outputs into 3-state. Individual output sections must be reenabled by setting the appropriate bits high in the MCR register. Internally, the local memory is in an undefined state, all CAM empty bits are set, all state machines are reset, and all registers are cleared to zero.

3.1.2 Software Reset

This is accomplished by setting the MSB of the master control and status register (see Section 2.1.2 Master Control and Status Register). The local and H-Bus connections are rendered invalid, all registers are cleared except MCR, CLKERR1, CLKERR2, and SYSERR (these registers are cleared with separate MCR control bits); the state machines are also reset. Applying the value 0xE0 to the MCR is a full software reset. Applying 0x0E enables all pin groups (though individual pins still require setup). This soft reset is clocked by the crystal oscillator.

3.1.3 Power-On Reset

No power-on reset is available. It is expected that the host microprocessor or applications board will provide an external control to the $\overline{\text{RESET}}$ pin for performing a hardware reset. The PLLs must not be enabled prior to establishing a stable supply voltage. There are two methods to accomplish this:

- Tie the En1 and En2 pins to the same line that drives the $\overline{\text{RESET}}$ which forces the PLLs into an off condition while the T8100 resets asynchronously.
- Add external capacitors from En1 to ground and from En2 to ground. (The values of the capacitors should be 1 µF or greater.) The capacitors will form RC circuits with the En1 and En2 internal pull-ups and will charge up to enable the PLLs after several milliseconds. The RC circuit affects the power-on reset for the PLLs. The long rise time provides some delay.

3.2 Basic Connections

At a minimum, the T8100 requires power, ground, and a 16.384 MHz crystal (or 16.384 MHz crystal oscillator). It is also recommended that the internal PLLs be treated as other analog circuits are, so the user should provide the appropriate filtering between the PLL1V_{DD} and V_{DD} pins (as well as PLL2V_{DD} and V_{DD} pins). The RDY pin is operated as an open collector output. It is actively driven low or into 3-state. The user should apply a pull-up (e.g., 10 kΩ) to maintain standard microprocessor interfacing. It is recommended that the 10 kΩ be tied to 3.3 V (since the T8100's nominal V_{OH} is 3.3 V), but the resistor may also be tied up to 5 V without damaging the device. PLL connections are shown in Figure 15. The H.100/H.110 clock signals, CT_C8_A, CT_C8_B, /CT_FRAME_A, /CT_FRAME_B, and CT_NETREF each require an individual external pull-up of 100 kΩ to 5 V or 50 kΩ to 3.3 V.

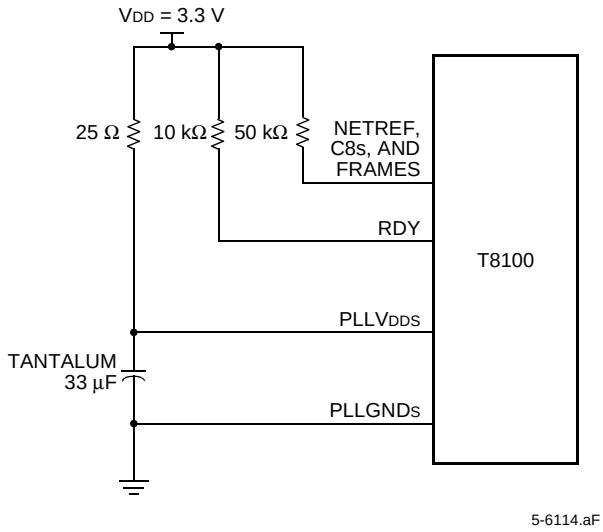


Figure 15. External Connection to PLLs

3 Using the T8100 (continued)

3.2 Basic Connections (continued)

3.2.1 Physical Connections for H.110

Figure 16 shows the T8100 physical connections required for use in an H.110 environment. There are electrical differences between H.100 and H.110. For H.110, external components are required to meet specifications. Figure 16 shows the T8100 NETREF terminations and the required terminations for CT_C8A, CT_FRAMEA, CT_C8B, and CT_FRAMEB. Each signal has a mechanism to short the 33 Ω series resistor and, in addition, a 10 kΩ pulldown resistor. The 50 kΩ internal pull-ups on the CT data bus are used for H.100. For H.110, the DPUE pin should be tied low, disabling these internal pull-ups. H.110 requires the CT data bus to have pull-ups of 18 kΩ to 0.7 V. The control leads of the FET switches would typically go to the microprocessor.

3.2.2 H.100 Data Pin Series Termination

All data bus lines must have a 24 Ω series resistor, even if only data lines 16—31 are used at 8.192 Mbits/s.

3.2.3 PC Board Considerations

There are no special requirements for the thermal balls on the BGA package when designing a printed-circuit board.

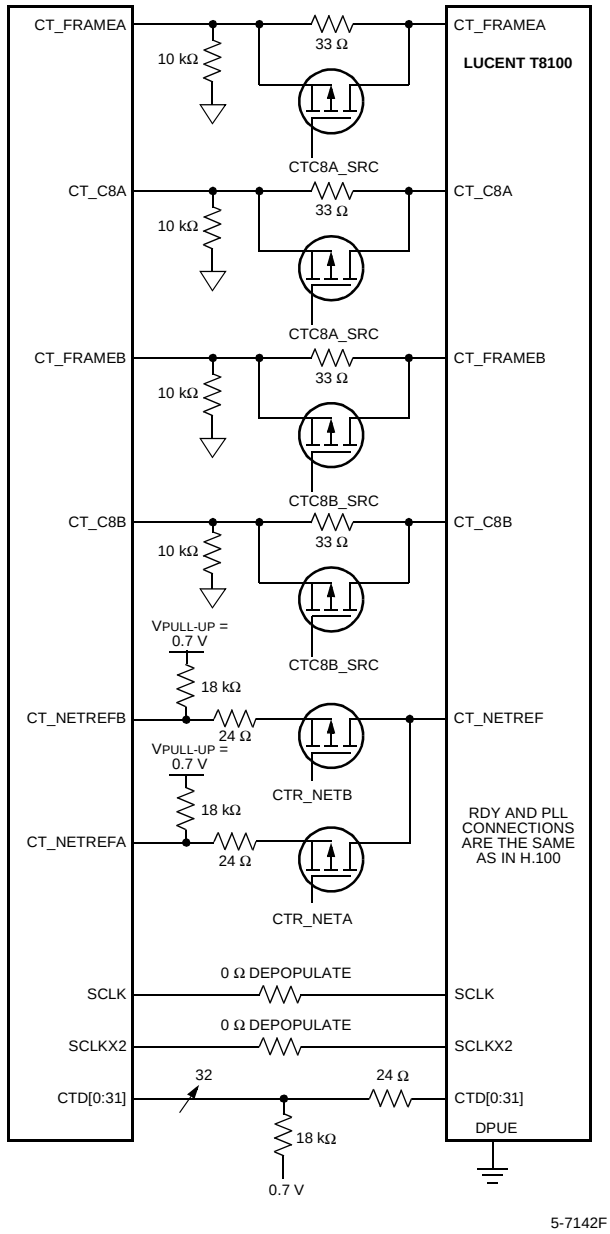


Figure 16. Physical Connections for H.110

3 Using the T8100 (continued)

3.3 Using the LAR, AMR, and IDR for Connections

3.3.1 Setting Up Local Connections

Local connections require a physical location in the local connection memory corresponding to the output stream and time slot. The location contains a pointer to a local data memory location which holds the actual data that has come in or will be sent out. The local memories are based on 1024 locations, so 10 bits are required to specify the physical memory location where a connection is placed or where data is stored. To simplify the programming, the user supplies 11 bits in a stream and time-slot format, which is converted by the T8100 to the appropriate physical location. Relative to describing a connection, a data memory location corresponds with the FROM stream and time slot, and a connection memory location corresponds with the TO stream and time slot. To program a connection, the user loads the data memory location into the connection memory location, effectively identifying where the data resides.

The user programs 7 bits of the LAR for the time-slot value (or 8 bits for pattern mode) and the lowest 4 bits of the AMR for the stream value; these will then be converted to the physical memory address. The upper bits of the AMR select which field in the connection memory is being written into. Since the connection information itself is 15 bits, two transfers (i.e., two fields) must be made to the address in the connection memory.

In each case, the transfer is an indirect write of data to the indirect data register, the IDR: The first transfer is the lowest 7 bits (time-slot address) of the desired data memory location. It is placed in the IDR after the LAR and AMR have been set up with the appropriate connection address.

Table 52 illustrates the decoding of the time-slot bits (address value in the table refers to the hex value of the 7 bits comprising time slot).

When programming the registers for fallback, the CKS and CKW registers should be programmed last.

Table 52. Time-Slot Bit Decoding

Address Value	2 Mbits/s Time Slot	4 Mbits/s Time Slot	8 Mbits/s Time Slot
0x00	0	0	0
0x01	1	1	1
0x02	2	2	2
0x03	3	3	3
0x04	4	4	4
0x05	5	5	5
0x06	6	6	6
0x07	7	7	7
0x08	8	8	8
0x09	9	9	9
0x0A	10	10	10
0x0B	11	11	11
0x0C	12	12	12
0x0D	13	13	13
0x0E	14	14	14
0x0F	15	15	15
0x10	16	16	16
0x11	17	17	17
:	:	:	:
0x1E	30	30	30
0x1F	31	31	31
0x20	NA	32	32
:	:	:	:
0x3E	NA	62	62
0x3F	NA	63	63
0x40	NA	NA	64
:	:	:	:
0x7E	NA	NA	126
0x7F	NA	NA	127

3 Using the T8100 (continued)

3.3 Using the LAR, AMR, and IDR for Connections (continued)

3.3.1 Setting Up Local Connections (continued)

Table 53. IDR: Indirect Data Register, Local Connections Only

The second transfer requires that data in the IDR be defined as follows:

REG	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IDR	—	Control				Address			
		XCS	PME	FME	CHE	—	—	—	—

Symbol	Bit	Name/Description
XCS	7	A programmable bit which is routed to the XCS pin one time slot prior to the data to which it relates.
PME	6	A high enables the pattern mode; the lower 8 bits of the connection address (time slot and stream LSB) is routed to the time slot instead of data.
FME	5	A high enables the use of the alternate data buffer; refer to Appendix B for minimum and constant delay settings.
CHE	4	Enables the time-slot connection; a low in this bit forces 3-state during the time slot.
Address	3—0	All 4 bits are used for the stream address of the desired data memory location.

After the second transfer is made, the entire 15 bits will be loaded into the connection memory; i.e., the second transfer triggers the actual memory access. Figure 17 shows how the connections are made from the perspective of the registers and memory contents.

If the user wishes to set up a pattern mode connection, then the first transfer is a full 8 bits (i.e., the pattern), rather than the 7-bit time-slot value. This pattern byte will be stored in the lowest 8 bits of the selected connection memory location. The pattern byte will be sent instead of a byte from local data memory during the output stream and time slot which corresponds to the connection memory location.

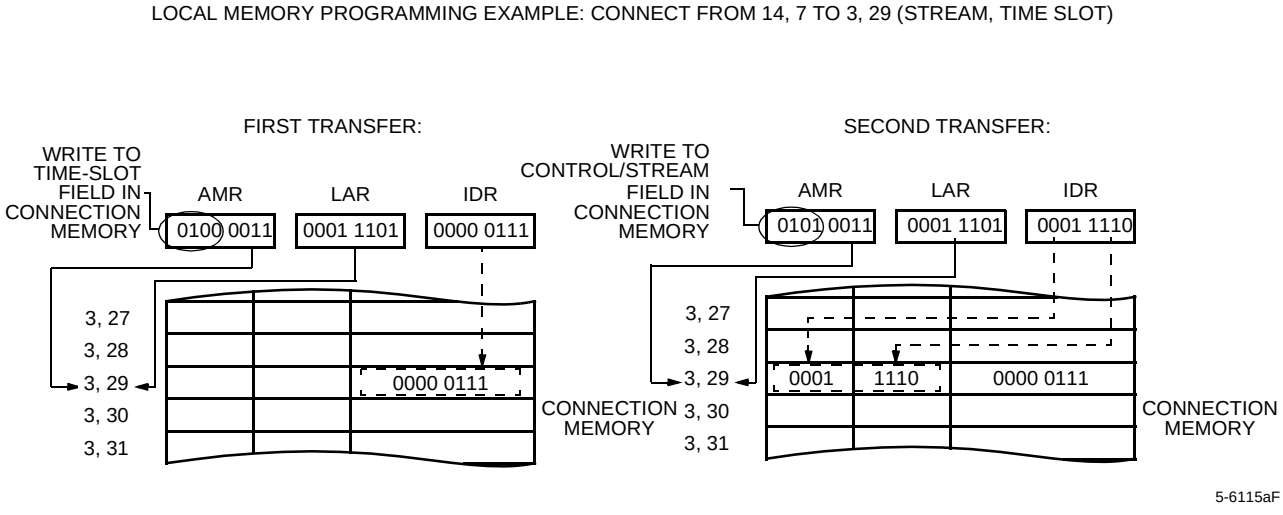


Figure 17. Local-to-Local Connection Programming

3 Using the T8100 (continued)

3.3 Using the LAR, AMR, and IDR for Connections (continued)

3.3.2 Setting Up H-Bus Connections

Table 54. IDR: Indirect Data Register, H-Bus Connections Only

REG	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IDR	—	Control			Address				
		$\overline{R/W}$	PME	FME	—	—	—	—	—

Symbol	Bit	Name/Description
$\overline{R/W}$	7	Refers to the direction in the CAM data memory. A read sends data to the bus; a write loads data from the bus.
PME	6	Pattern mode enable, similar to above, except the tag byte is output instead of the lower address bits.
FME	5	Data buffer selection for setting delay type. (Refer to Appendix B for minimum and constant delay setting.)
Address	4—0	All 5 bits are used for the stream address of the desired data memory location.

The CAM blocks are 256 locations each and the operations for the CAM blocks are selected by AMR (see Section 2.1.3 Address Mode Register and Section 2.3.2 CAM Operation and Commands). Since the block address is carried in the AMR, this reduces the number of bits which are necessary to establish a connection. Eleven (11) address bits, i.e., bits for stream and time-slot identification, the 8-bit tag (pointer to the H-Bus data memory), and 3 control bits all need to be written into the selected CAM block for setting up a connection. (The empty bit is a status bit that is changed internally as a result of operations on the CAM.) Three transfers, indirect writes through the IDR, are required to set up a connection in the CAM, though the method of transfer is different than with the local memory. Since a specific physical address is not always necessary, the CAM will automatically fill the first available slot. Thus, the LAR is not required for setting up the connection. (See the notes below.) The first transfer after programming the AMR requires that the 7 bits which identify the time-slot number (refer to Section 2.3.5 H-Bus Rate Selection and Connection Address Format for the proper format) be loaded into the IDR. The second transfer uses a similar field description for the IDR as presented for local connections (Section 3.3.1 Setting Up Local Connections above). The address field contains the stream number (5 bits), and the control field contains only three control bits.

The third (and final) transfer for CAM connection setup is the transfer of the 8-bit tag field. The tag is loaded into the IDR. The connection for the CAM is actually set up, i.e., the memory access takes place, using a fourth write. It is an indirect write to the AMR (again through the IDR) which corresponds with the specific command and blocks the user requests. All CAM commands require that the IDR be loaded with the same command value as the AMR rather than a don't care or dummy value.

Notes: If an address is to be matched, such as the break connection command, then only the first two transfers are required. The tag is unnecessary for identifying a connection.

The LAR is only used to read or query a specific location (i.e., 0—255) in a particular CAM block. Refer to Section 2.1.3 Address Mode Register and Section 2.3.2 CAM Operation and Commands for details on these commands.

For the CAMs, pattern mode is a 1/2 connection. Only the intended output to the H-Bus (or to the local pins) needs to be specified. The setup is the same as described above, three transfers to the holding registers followed by the make connection command to the appropriate CAM block. When the address is matched, the tag value (from the pipeline SRAM) will be sent as output to the bus.

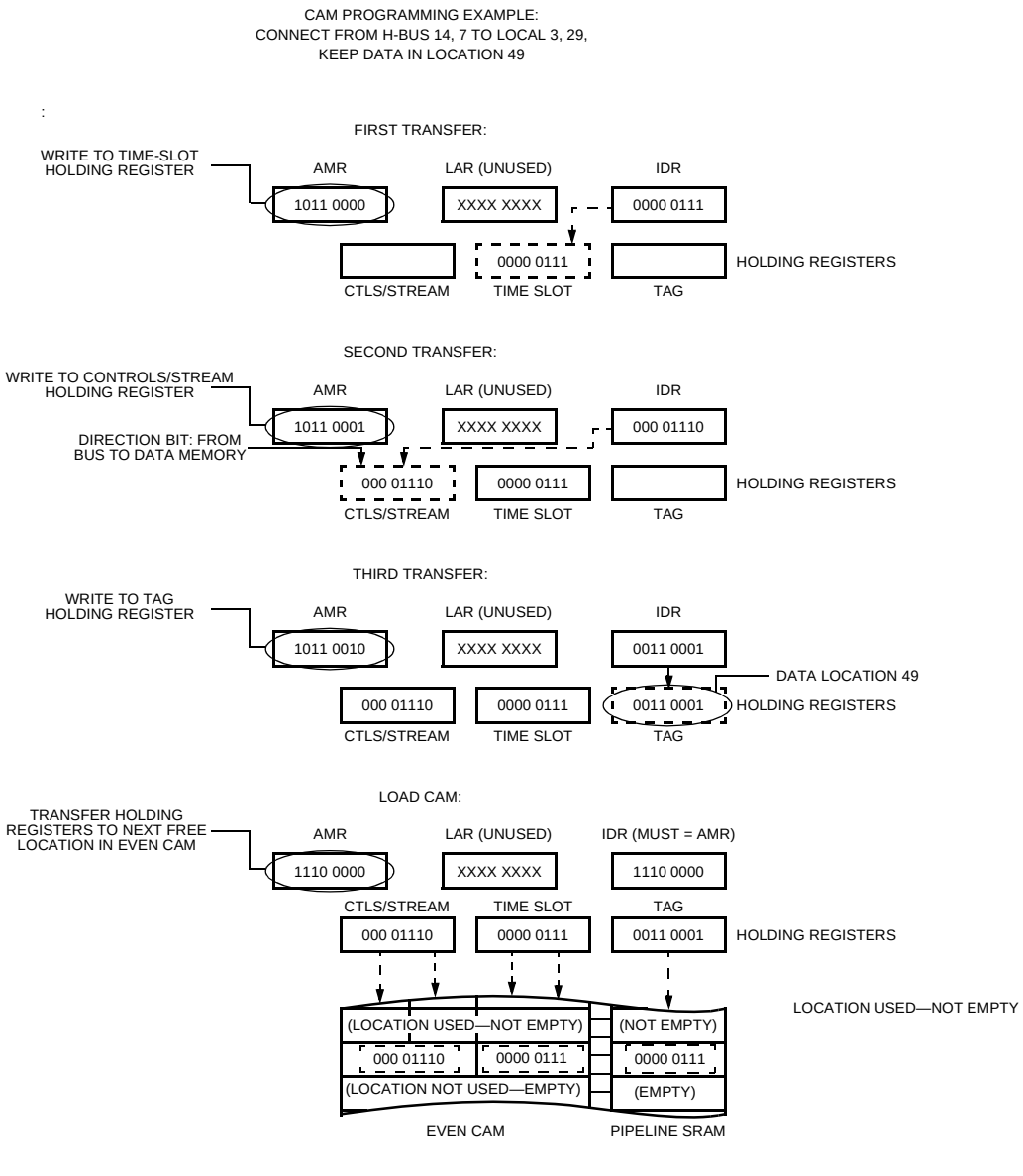
Figure 18 illustrates how a CAM connection is made from the perspective of registers and the memory locations. Note that each half of the connection, that is the FROM and the TO, requires a separate setup, though each half will point to the same location in the H-Bus data memory.

Following Figure 18, some simple programming examples are shown using pseudoassembler code. The local-to-local and H-Bus-to-local switching examples from Figure 17 and Figure 18 are reused in code examples #2 and #3. The connections are referred to in stream, time-slot format.

3 Using the T8100 (continued)

3.3 Using the LAR, AMR, and IDR for Connections (continued)

3.3.2 Setting Up H-Bus Connections (continued)



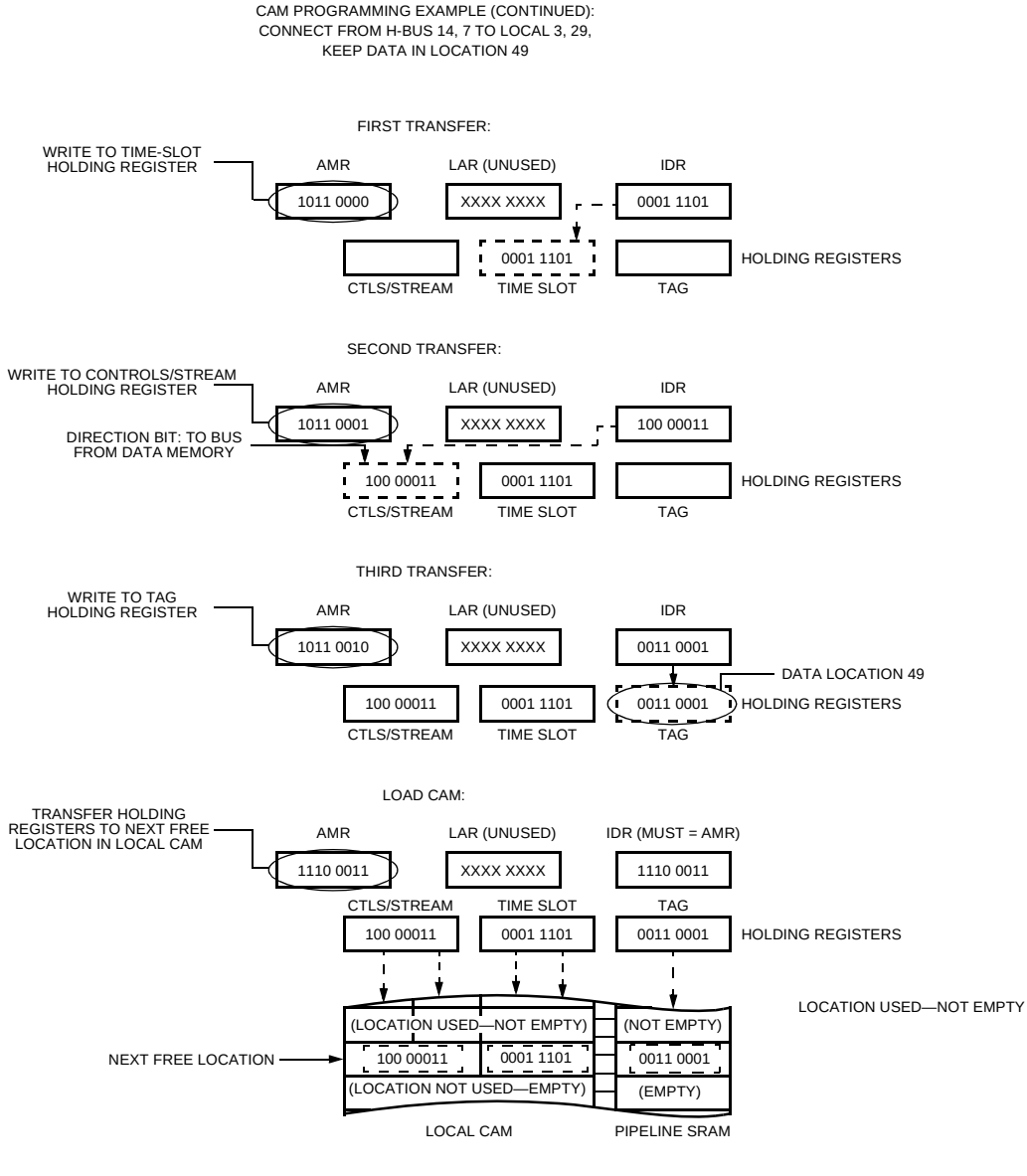
A. First Half of Connection, H-Bus Side

Figure 18. CAM Programming, H-Bus-to-Local Connection

3 Using the T8100 (continued)

3.3 Using the LAR, AMR, and IDR for Connections (continued)

3.3.2 Setting Up H-Bus Connections (continued)



B. Second Half of Connection, Local Side

Figure 18. CAM Programming, H-Bus-to-Local Connection (continued)

3 Using the T8100 (continued)

3.3 Using the LAR, AMR, and IDR for Connections (continued)

3.3.3 Programming Examples

```
;All programming examples included are in a pseudoassembler format.
;The basic commands used are the “move direct” and “move indirect.”
;A move direct command is indicated by the letters “MD” followed by
;the register name, then the data. Similarly, a move indirect command
;is indicated by the letters “MI” followed by the register name, then by
;data or another register reference (the register may not be indirect).
;The semicolon delineates comments. Direct data is followed by the
;letter “h” for Hex and “b” for binary.

;*******EXAMPLE #1 - Set Up Clocks, Local Bus, H-Bus, and Framers
;
;*******Misc. Stuff
;
MD,AMR,00h              ;Define control space
                        ;all specific register names are equivalent
                        ;to the LAR addresses (from Table 11)
;
;
;*******Set up Clocks
                        ;**Main Clock Register
MD,IDR,0C2h             ;Load IDR with values for bit slider on, slave mode,
                        ;and synced to ECTF Bus A Clocks
MI,CKM,IDR              ;The data in IDR is moved into CKM via the LAR register.
;
;**NETREF Registers
MD,IDR,88h              ;Set up NETREF from Local Reference 0, 2.048 MHz bit clock
                         in, divided value
                        ;value out (i.e., 8 kHz), enable the DJAT connections
MI,CKN,IDR              ;Move the data to CKN
MD,IDR,0FFh             ;Set up NETREF divider with divide-by-256
MI,CKND,IDR             ;Move the data to CKND
;
;**Programmable Clocks
MD,IDR,26h              ;This selects the oscillator for the TCLKO, A Clock
                         outputs off, and
                        ;driving ECTF B Clocks
MI,CKP,IDR              ;Move the data
;
;**Clock Resources
MD,IDR,40h              ;Synced to bus so select Resource divider, x16 on PLL #1 &
                         x8 PLL #2, SC Clocks off
MI,CKR,IDR              ;Make it so
MD,IDR,01h              ;Set up Resource divider with divide-by-2 for 4 MHz signal
                         into PLL #1
MI,CKRD,IDR             ;Move the data to divider
;
```

3 Using the T8100 (continued)

3.3 Using the LAR, AMR, and IDR for Connections (continued)

3.3.3 Programming Examples (continued)

```
;**Secondary Controls (Fallback)
MD,IDR,35h              ;Enable ECTF Fallback: Become the new A Clock master on A
                         Clock failure,
                        ;synchronizes to a bit clock on local reference 1, but
                         requires the main divider
                        ;with external input (assumes a CLAD is between the
                         divider and 4MHzIn).
MI,CKS,IDR              ;Move the data to CKS
MD,IDR,0FFh             ;Set up Main divider with divide-by-256
MI,CKMD,IDR             ;Move the data to divider
                        ;
;**Local Clocks
MD,IDR,0E4h             ;Local Selected Clock 3 gets inverted 8.192 MHz, LSC2 gets
                         2.048 MHz
MI,CK32,IDR             ;Move it to CK32
MD,IDR,80h              ;LSC1 is high & LSC0 is low
MI,CK10,IDR             ;Move it to CK10
;
;*******Set up Local Streams
;
MD,IDR,30h              ;8 Streams at 8 Mbits/s
MI,LBS,IDR              ;Define input streams per IDR
;
;*******Set up H Bus Streams
;
MD,IDR,0AAh             ;Define H-Bus Streams 0 - 15 for 4 Mbits/s
MI,HSL,IDR              ;Do it
;
MD,IDR,0FFh             ;Define H-Bus Streams 16-31 for 8 Mbits/s
MI,HSH,IDR              ;Engage

;*******Set up Framers
;
MD,IDR,00h              ;This sequence sets up Group A
MI,FRLA,IDR             ;           to start coincident
MI,FRLB,IDR             ;           with the Frame
MI,FRPH,IDR             ;           boundary and Group B
MD,IDR,0F0h             ;           to start halfway through
MI,FRHA,IDR             ;           the Frame. The Groups
MD,IDR,0F4h             ;           operate in normal framing mode
MI,FRHB,IDR             ;           at 8 Mbits/s and are Double Byte wide.
                        ;Note: FRPH sets up the correct routing.
;
;*******Connect the T8100 to the outside world
;
MD,MCR,0Eh              ;           Enable H-Bus Streams & Clock, Local Streams,
                                    local
                        ;           Clocks including Framers
;
;*******END OF EXAMPLE #1
```

3 Using the T8100 (continued)

3.3 Using the LAR, AMR, and IDR for Connections (continued)

3.3.3 Programming Examples (continued)

```
;*******EXAMPLE #2 - Setting up Local Connections
;
;           Use 8 Mbits/s rate set up from Example #1...
;           Send data from Stream 7/Time Slot 60 to Stream 0/Time Slot 2
;           The data is coming from Data Location Stream 07h, Time Slot 3Ch, and is
;           being accessed by Connection Memory Location Stream 00h, Time Slot 02h
;           in the next frame (unframed operation).
;
MD,LAR,1Dh              ;Set up lower address, i.e., Time Slot 29
MD,AMR,43h              ;           Set up upper address bits (Stream 3), and
                                    point to the
                        ;           the Time Slot field of the connection memory
MI,IDR,07h              ;Put a “7” in the Time Slot field of connection location
                         3,29
;
;Syntactically, “MI,IDR,data” is a special case since IDR is not the final recipient
of the data
;
MD,AMR,53h              ;Maintain the same upper address, but get ready to load the
                        ;           remaining connection info (upper bits +
                                    control)
MI,IDR,0001_1110b       ;This decodes as follows: XCS bit low, pattern mode off
                        ;           (not set), frame bit low, time slot enabled,
                                    and stream = 1110b (14)
;
;*******END OF EXAMPLE #2
;*******EXAMPLE #3 - Setting up H-Bus Connections
;
; Use rate set up from Example #1...
; Send data from Stream 14/Time Slot 7 of the H.100 bus to Stream 3/Time Slot 29
; on the Local side. The data is coming in at 4 Mbits/s from E-CAM, and is sent
; out at 8 Mbits/s to through L-CAM. We’re using Data Memory location 49 to hold
; the actual data. LAR is not used for the CAM connection setups; it is used for
; reading specific CAM locations or writing and reading the associated Data
; Memory Locations.
;
;******Set up the “from” connection
;
MD,AMR,0B0h           ;Point to the Time-Slot holding register
MI,IDR,07h            ;This is the Time-Slot value (7) for the H-Bus address
MD,AMR,0B1h           ;Point to the upper bits of the connection
MI,IDR,000_01110b     :Set up a write into data memory from ECTF bus,
                      ;           disable pattern mode, minimum delay,
                      ;           and set stream number equal to 01110b (14).
MD,AMR,0B2h           ;Point to tag field
MI,IDR,31h            ;Use location 49 of the associated Data RAM to store the data
;
MD,AMR,0E0h           ;Write to next free location in the Even CAM
MI,IDR,0E0h           ;The command is executed with the indirect to IDR which
                      ;uses the same command value as in the AMR.
```

3 Using the T8100 (continued)

3.3 Using the LAR, AMR, and IDR for Connections (continued)

3.3.3 Programming Examples (continued)

```
;
;**Optional: Test CAM Busy bit**
TEST:
MD,ACC,MCR           ;Move MCR contents into (host's) accumulator (for example)
AND,01h              ;Logical AND, i.e., mask off all but LSB of the MCR register
JNZ TEST             ;If the LSB is zero (not busy), continue, else jump back and
                     ;retest
;
CONTINUE:
;
;******Set up the "to" connection
;
MD,AMR,0B0h          ;Point to the Time-Slot holding register
MI,IDR,1Dh           ;This is the Time-Slot value (29) for the Local address
MD,AMR,0B1h          ;Point to the upper bits of the connection
MI,IDR,100_00011b    :Set up a read from data memory to Local pins,
                     ;              disable pattern mode, minimum delay, and set
                     ;              stream number equal to 00011b (3).
MD,AMR,0C2h          ;Point to tag field
MI,IDR,31h           ;Use location 49 of the associated Data RAM to store the data
;
MD,AMR,0E3h          ;Write to next free location in the Local CAM
MI,IDR,0E3h          ;The command is executed with the indirect to IDR
;
;
;
;**CAM Busy bit can be tested here**
;
;
;*******END OF EXAMPLE #3
```

3.2.4 Miscellaneous Commands

These commands (i.e., 0x70, 0xF8, all reset commands in the AMR register) require two writes: first the value is written to the AMR register; then the same value is written to the IDR register. After writing to the IDR register, the command will be executed.

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Description	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	—	3.6	V
XTALIN and XTALOUT Pins	—	V_{SS}	V_{DD}	V
Voltage Applied to I/O Pins	—	V_{SS} – 0.5	V_{DD} + 3.4	V
Operating Temperature: 208-pin SQFP 217-pin BGA	 — —	 0 –40	 70 85	 °C °C
Storage Temperature	T_{stg}	–55	125	°C

4.2 Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Lucent employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. No industry-wide standard has been adopted for CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and therefore can be used for comparison purposes. The HBM ESD threshold presented here was obtained by using these circuit parameters:

HBM ESD Threshold Voltage	
Device	**Rating**
T8100	2500 V

4 Electrical Characteristics (continued)

4.3 Crystal Oscillator

Table 55. Crystal Oscillator

The T8100 requires a 16.384 MHz clock source. To supply this, a 16.384 MHz crystal can be connected between the RCLK and XTALOUT pins. External 18 pF, 5% capacitors must be connected from XTALIN and XTALOUT to V_{SS}. Crystal specifications are shown below. The ±32 ppm tolerance is the suggested value if either the DPLL is used or fallback to the oscillator is enabled while mastering the bus. Otherwise, a crystal with a lesser tolerance can be used.

Parameter	Value
Frequency	16.384 MHz
Oscillation Mode	Fundamental, Parallel Resonant
Effective Series Resistance	40 Ω maximum
Load Capacitance	14 pF
Shunt Capacitance	7 pF maximum
Frequency Tolerance and Stability	32 ppm

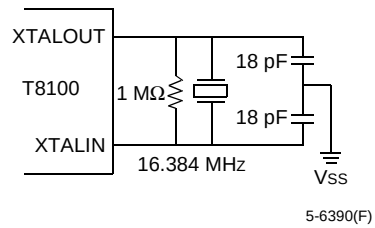


Table 56. Alternative to Crystal Oscillator

When XTALIN is driven by a CMOS signal instead of an oscillator, it must meet the requirements shown below:

Parameter	Value	
Frequency	16.384 MHz	
Maximum Rise or Fall Time	5 ns	
Minimum Pulse Width	**Low**	**High**
	20 ns	20 ns

4.4 dc Electrical Characteristics, H-Bus (ECTF H.100 Spec., Rev. 1.0)

4.4.1 Electrical Drive Specifications—CT_C8 and /CT_FRAME

Table 57. Electrical Drive Specifications—CT_C8 and /CT_FRAME

V_{DD} = 3.3 and V_{SS} = 0.0 unless otherwise specified.

Parameter	Symbol	Condition	Min	Max	Unit
Output High Voltage	V_{OH}	I_{OUT} = –24 mA	2.4	3.3	V
Output Low Voltage	V_{OL}	I_{OUT} = 24 mA	–0.25	0.4	V
Positive-going Threshold	Vt+	—	1.2	2.0	V
Negative-going Threshold	Vt–	—	0.6	1.6	V
Hysteresis (Vt+ – Vt–)	V_{HYS}	—	0.4	—	V
Input Pin Capacitance	C_{IN}	—	—	10	pF

PCI-compliant data line I/O cells are used for the CT bus data lines. (See PCI Specification, Rev. 2.1, Chapter 4.)

/C16, /C4, C2, SCLK, $\overline{\text{SCLKX2}}$, and /FR_COMP all use the same driver/receiver pairs as those specified for the CT_C8 and /CT_FRAME signals, though this is not explicitly stated as a part of the H.100 Specification.

4 Electrical Characteristics (continued)

4.5 dc Electrical Characteristics, All Other Pins

Table 58. dc Electrical Characteristics, All Other Pins

V_{DD} = 3.3 and V_{SS} = 0.0 unless otherwise specified.

Description	Symbol	Min	Typ	Max	Condition	Unit
Supply Current	I_{DD}	—	270	450*	—	mA
Supply Voltage	V_{DD}	3.0	—	3.6	—	V
Input High Voltage	V_{IL}	—	—	0.8	—	V
Input Low Voltage	V_{IH}	2.0	—	—	—	V
Input Current	I_I	—	—	1	—	µA
Input Capacitance (input only)	C_I	—	—	5	—	pF
Input Capacitance (I/O pins)	C_{IO}	—	—	10	—	pF
Input Clamp Voltage	V_C	—	—	–1.0	—	V
Output High Voltage	V_{OH}	2.4	—	—	—	V
Output Low Voltage	V_{OL}	—	—	0.4	—	V
Output Short-circuit Current	I_{OS}	—	—	100	V_{OH} tied to GND	mA

* Circuit simulation indicates a worst-case current of 450 mA. This parameter is not tested in production.

4 Electrical Characteristics (continued)

4.6 H-Bus Timing (Extract from H.100 Spec., Rev. 1.0)

4.6.1 Clock Alignment

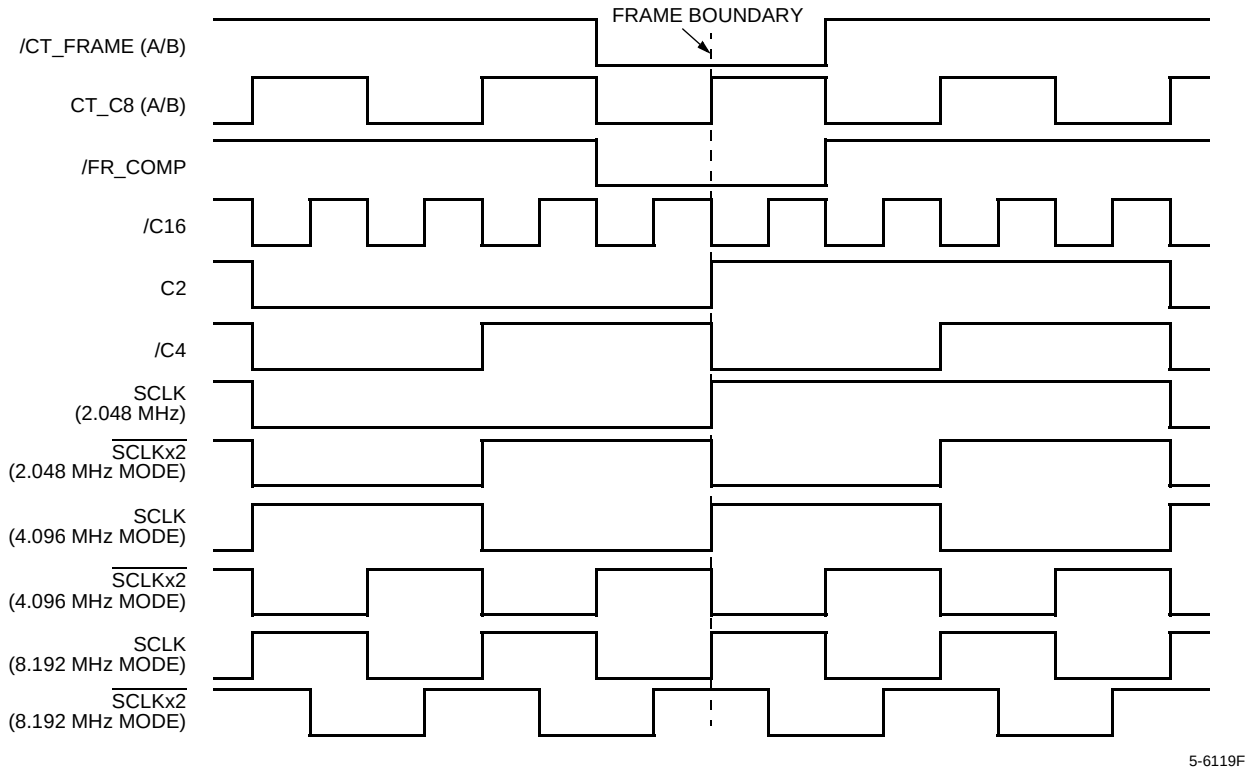
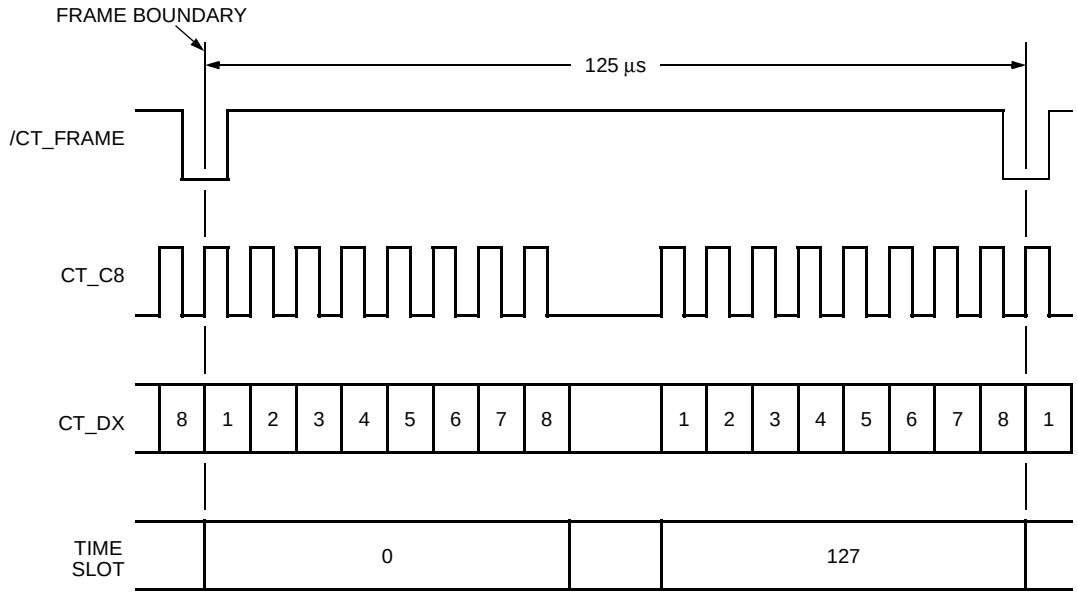


Figure 19. Clock Alignment

4 Electrical Characteristics (continued)

4.6 H-Bus Timing (Extract from H.100 Spec., Rev. 1.0) (continued)

4.6.2 Frame Diagram



Note: Bit 1 is the MSB. Bit 8 is the LSB. MSB is always transmitted first in all transfers.

Figure 20. Frame Diagram

4 Electrical Characteristics (continued)

4.6 H-Bus Timing (Extract from H.100 Spec., Rev. 1.0) (continued)

4.6.3 Detailed Timing Diagram

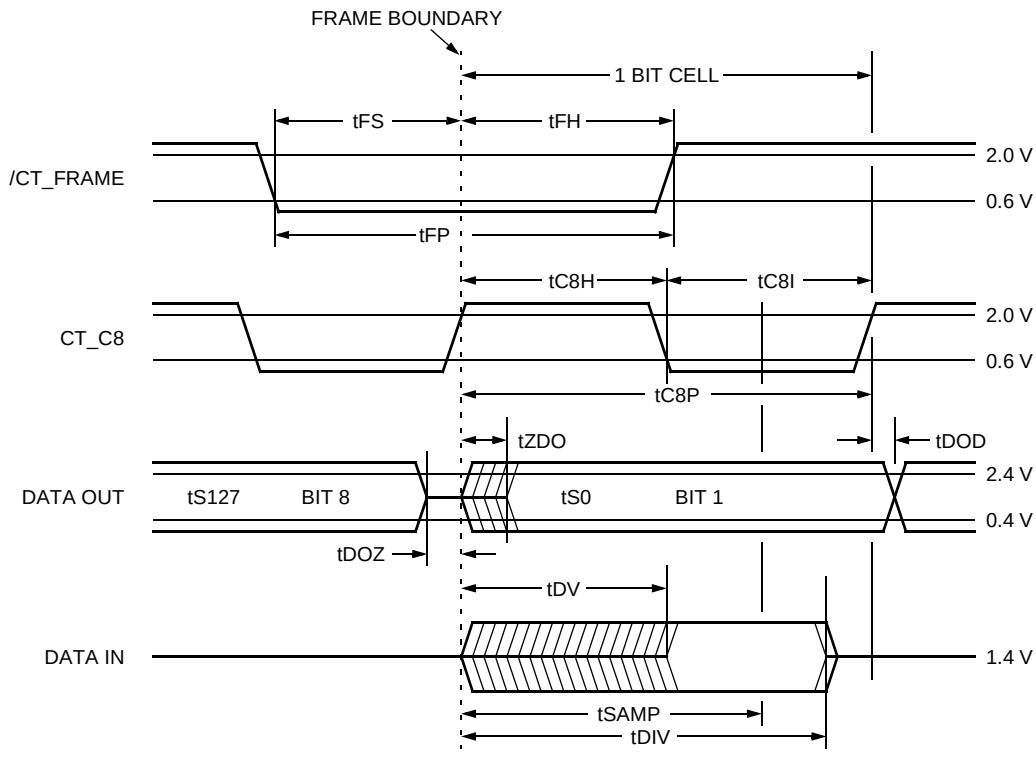


Figure 21. Detailed Timing Diagram

4 Electrical Characteristics (continued)

4.6 H-Bus Timing (Extract from H.100 Spec., Rev. 1.0) (continued)

4.6.4 ac Electrical Characteristics, Timing, H-Bus (H.100, Spec., Rev. 1.0)

Table 59. ac Electrical Characteristics, Timing, H-Bus (H.100, Spec., Rev. 1.0)

Symbol	Parameter	Min	Typ	Max	Unit	Notes
—	Clock Edge Rate (all clocks)	0.25	—	2	V/ns	1, 2, 4
tC8P	Clock CT_C8 Period	122.066 – Φ	—	122.074 + Φ	ns	2, 4, 5
tC8H	Clock CT_C8 High Time	49 – Φ	—	73 + Φ	ns	2, 4, 6
tC8L	Clock CT_C8 Low Time	49 – Φ	—	73 + Φ	ns	2, 4, 6
tSAMP	Data Sample Point	—	90	—	ns	2, 4, 9
tDOZ	Data Output to HiZ Time	–20	—	0	ns	2, 3, 4, 7, 11
tZDO	Data HiZ to Output Time	0	—	22	ns	2, 3, 4, 7, 11
tDOD	Data Output Delay Time	0	—	22	ns	2, 3, 4, 7
tDV	Data Valid Time	0	—	69	ns	2, 3, 4, 8, 10
tDIV	Data Invalid Time	102	—	112	ns	2, 4
tFP	/CT_FRAME Width	90	122	180	ns	2, 4
tFS	/CT_FRAME Setup Time	45	—	90	ns	2, 4
tFH	/CT_FRAME Hold Time	45	—	90	ns	2, 4
Φ	Phase Correction	0	—	10	ns	12

1. The rise and fall times are determined by the edge rate in V/ns. A maximum edge rate is the fastest rate at which a clock transitions. CT_NETREF has a separate requirement. (See Section 2.4 Clocking Section.)
2. Measuring conditions, data lines: V_{TH} (threshold voltage) = 1.4 V, V_{HI} (test high voltage) = 2.4 V, V_{LO} (test low voltage) = 0.4 V, input signal edge rate = 1 V/ns measuring conditions, clock and frame lines: Vt+ (test high voltage) = 2.0 V, Vt– (test low voltage) = 0.6 V, input signal edge rate = 1 V/ns.
3. Test load—200 pF.
4. When RESET is active, every output driver is 3-stated.
5. tC8P minimum and maximum are under free-run conditions assuming ±32 ppm clock accuracy.
6. Noncumulative, tC8P requirements still need to be met.
7. Measured at the transmitter.
8. Measured at the receiver.
9. For reference only.
10. tDV = maximum clock cable delay + max. data cable delay + max. data HiZ to output time = 12 ns + 35 ns + 22 ns = 69 ns. Max. clock cable delay and maximum data cable delay are worst-case numbers based on electrical simulation.
11. tDOZ and tZDO apply at every time-slot boundary.
12. F (phase correction) results from PLL timing corrections.

4 Electrical Characteristics (continued)

4.6 H-Bus Timing (Extract from H.100 Spec., Rev. 1.0) (continued)

4.6.5 Detailed Clock Skew Diagram

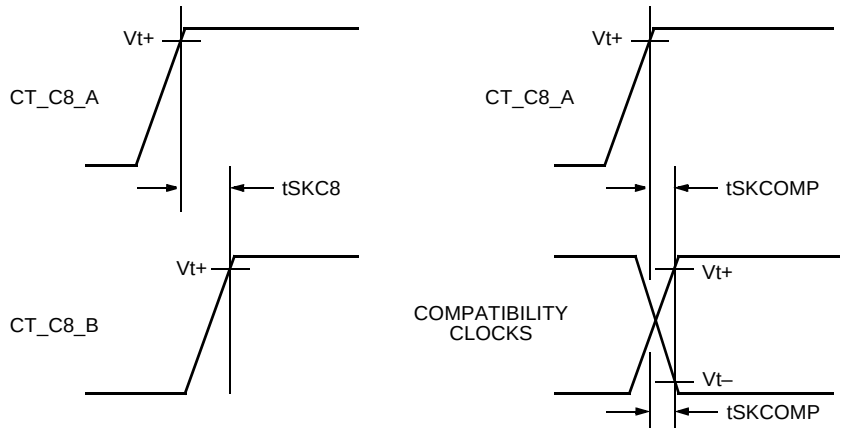


Figure 22. Detailed Clock Skew Diagram

4.3.6 ac Electrical Characteristics, Skew Timing, H-Bus (H.100, Spec., Rev. 1.0)

Table 60. ac Electrical Characteristics, Skew Timing, H-Bus (H.100, Spec., Rev. 1.0)

Symbol	Parameter	Min	Typ	Max	Unit	Notes
tSKC8	Max Skew Between CT_C8 A and B	—	—	±10 ±Φ	ns	1, 2, 3, 4
tSKCOMP	Max Skew Between CT_C8_A and Any Compatibility Clock	—	—	±5	ns	1

1. Test load—200 pF.
2. Assumes A and B masters in adjacent slots.
3. When static skew is 10 ns and, in the same clock cycle, each clock performs a 10 ns phase correction in opposite directions, a maximum skew of 30 ns will occur during that clock cycle.
4. Meeting the skew requirements in Table 10 and the requirements of Section 2.3 H-Bus Section could require the PLLs generating CT_C8 to have different time constants when acting as primary and secondary clock masters.

4.6.7 Reset and Power On

Table 61. Reset and Power On

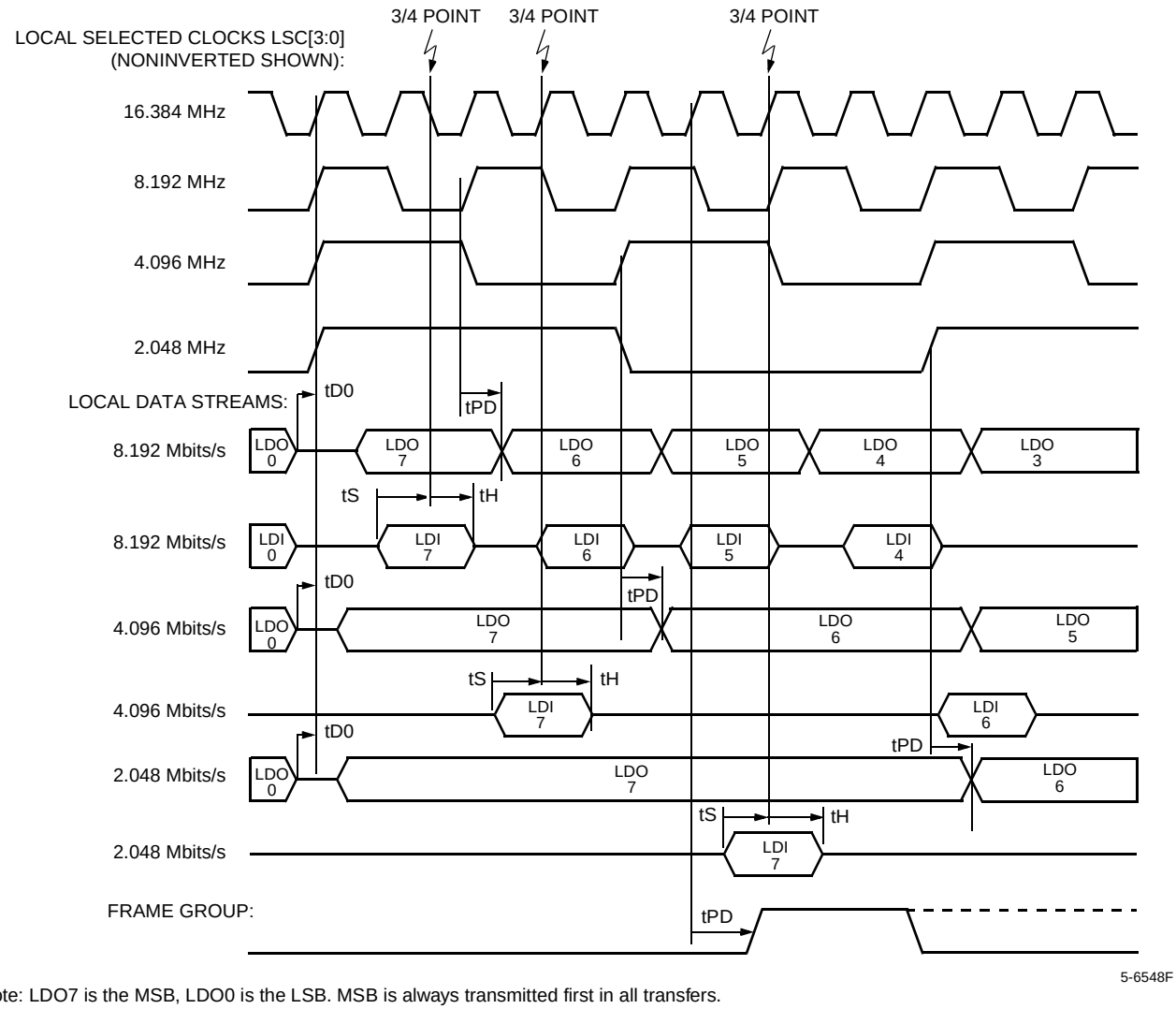
Symbol	Parameter	Min	Typ	Max	Unit
tRD	Output Float Delay from Reset Active	—	—	1	µs
tRS	Reset Active from Power Good	—	5	—	µs

4 Electrical Characteristics (continued)

4.7 ac Electrical Characteristics, Local Streams, and Frames

Table 62. ac Electrical Characteristics, Local Streams, and Frames

Symbol	Description	Min	Max	Condition	Unit
tPD	Data Propagation Delay	0	20	Load = 50 pF	ns
tS	Data Setup Time	10	—	—	ns
tH	Data Hold Time	5	—	—	ns
tOFF	Data 3-state Off Time	—	20	—	ns
tD0	Data Bit 0 3-state	–20	0	—	ns



Note: LDO7 is the MSB, LDO0 is the LSB. MSB is always transmitted first in all transfers.

Figure 23. ac Electrical Characteristics, Local Streams, and Frames

4 Electrical Characteristics (continued)

4.8 ac Electrical Characteristics, Microprocessor Timing

4.8.1 Microprocessor Access *Intel* Multiplexed Write and Read Cycles

For *Intel* write and read cycles, when RDY is low, wait-states are inserted. RDY is brought high when tIACC is met. This is true for both read and write cycles.

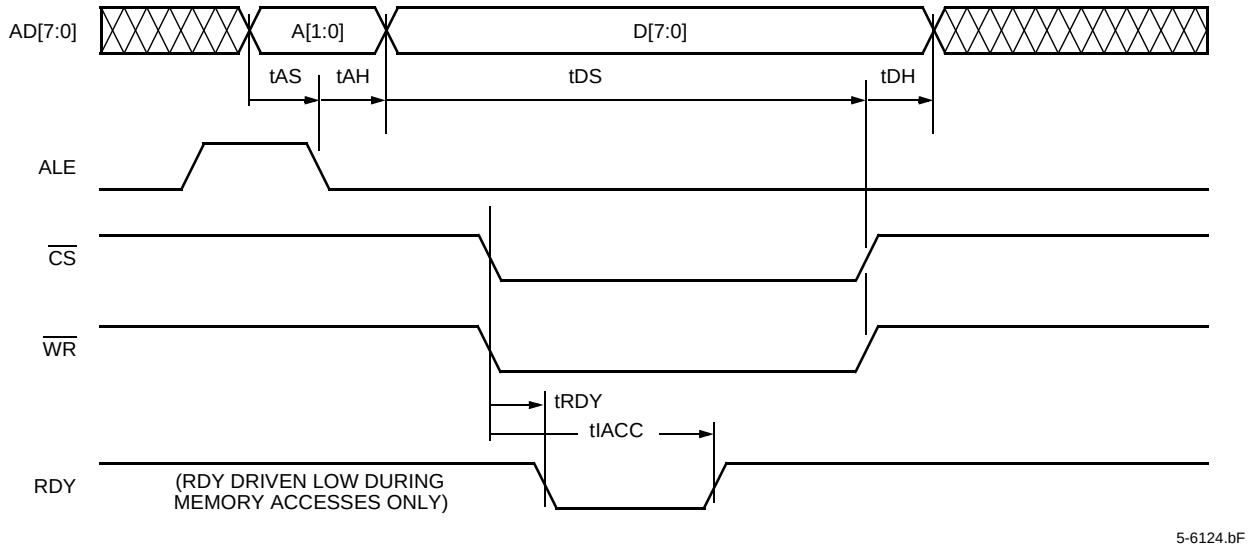


Figure 24. Microprocessor Access *Intel* Multiplexed Write Cycle

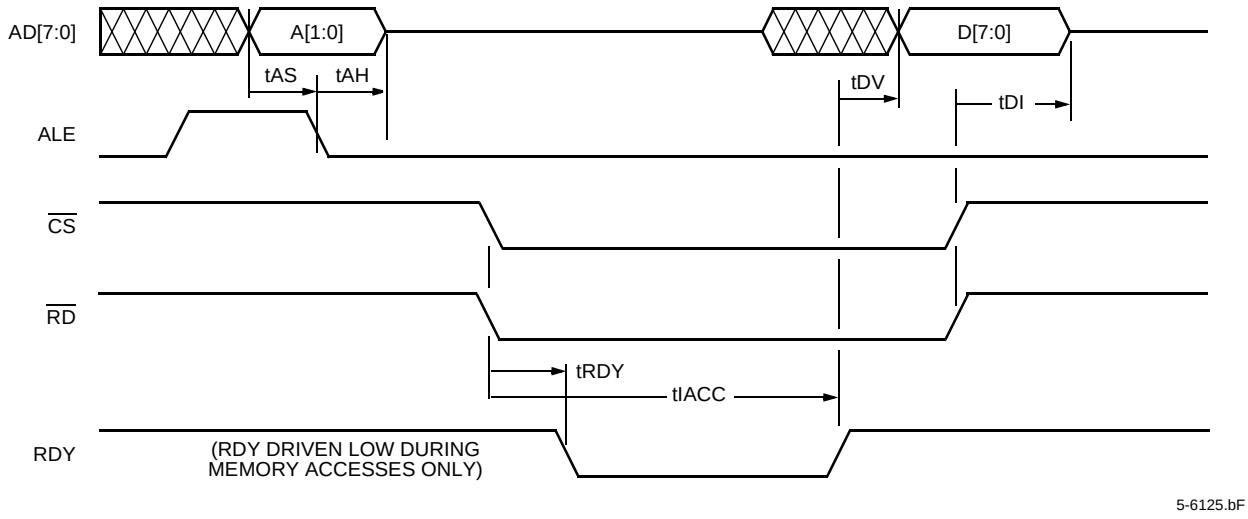


Figure 25. Microprocessor Access *Intel* Multiplexed Read Cycle

4 Electrical Characteristics (continued)

4.8 ac Electrical Characteristics, Microprocessor Timing (continued)

4.8.2 Microprocessor Access *Motorola* Write and Read Cycles

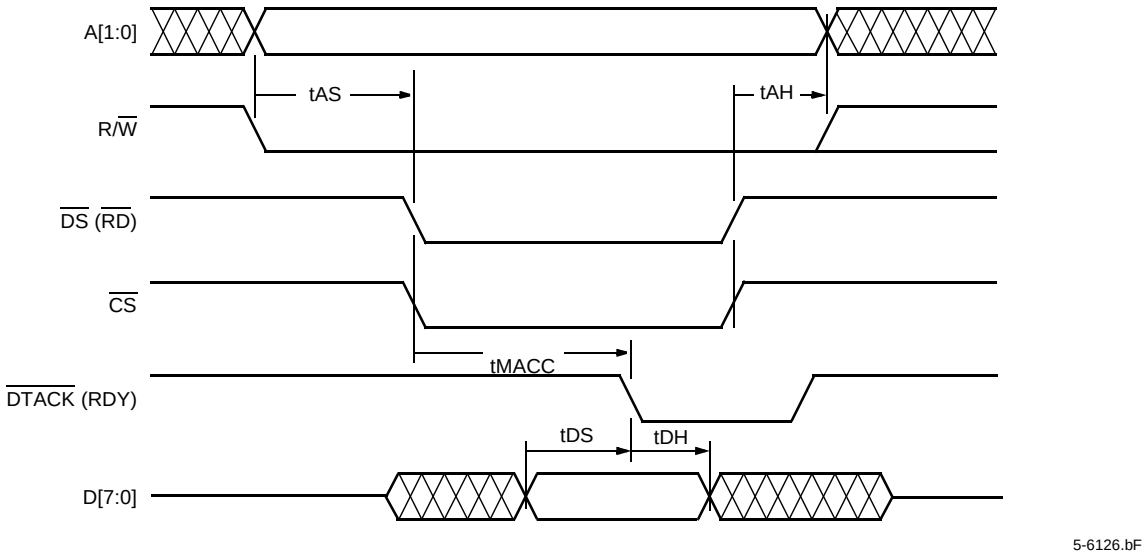


Figure 26. Microprocessor Access *Motorola* Write Cycle

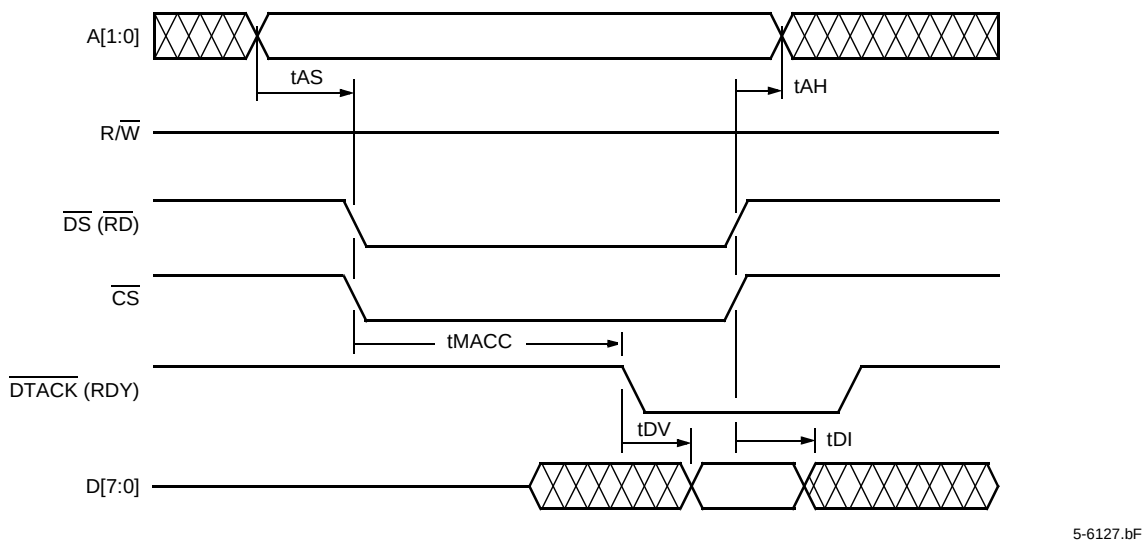


Figure 27. Microprocessor Access *Motorola* Read Cycle

4 Electrical Characteristics (continued)

4.8 ac Electrical Characteristics, Microprocessor Timing (continued)

4.8.3 Microprocessor Access *Intel* Demultiplexed Write Cycle

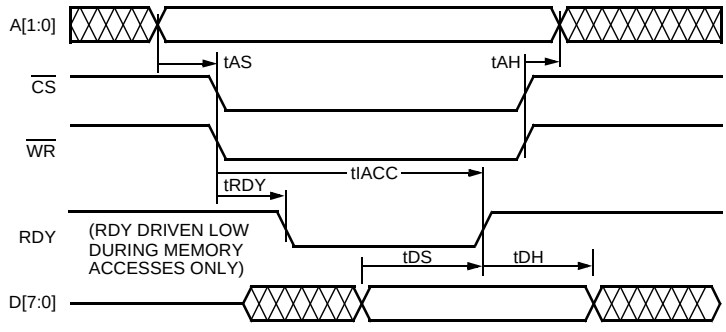


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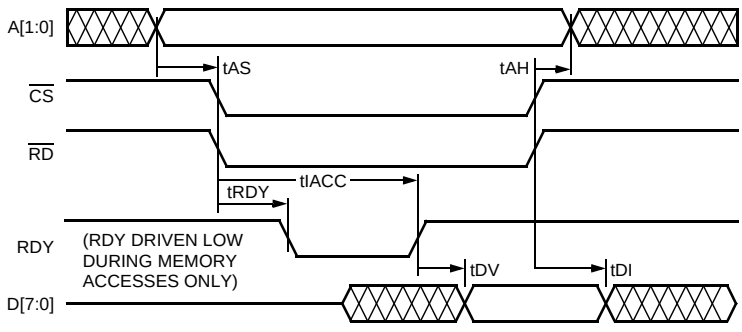
Figure 28. Microprocessor Access *Intel* Demultiplexed Write Cycle



5-6128.bF

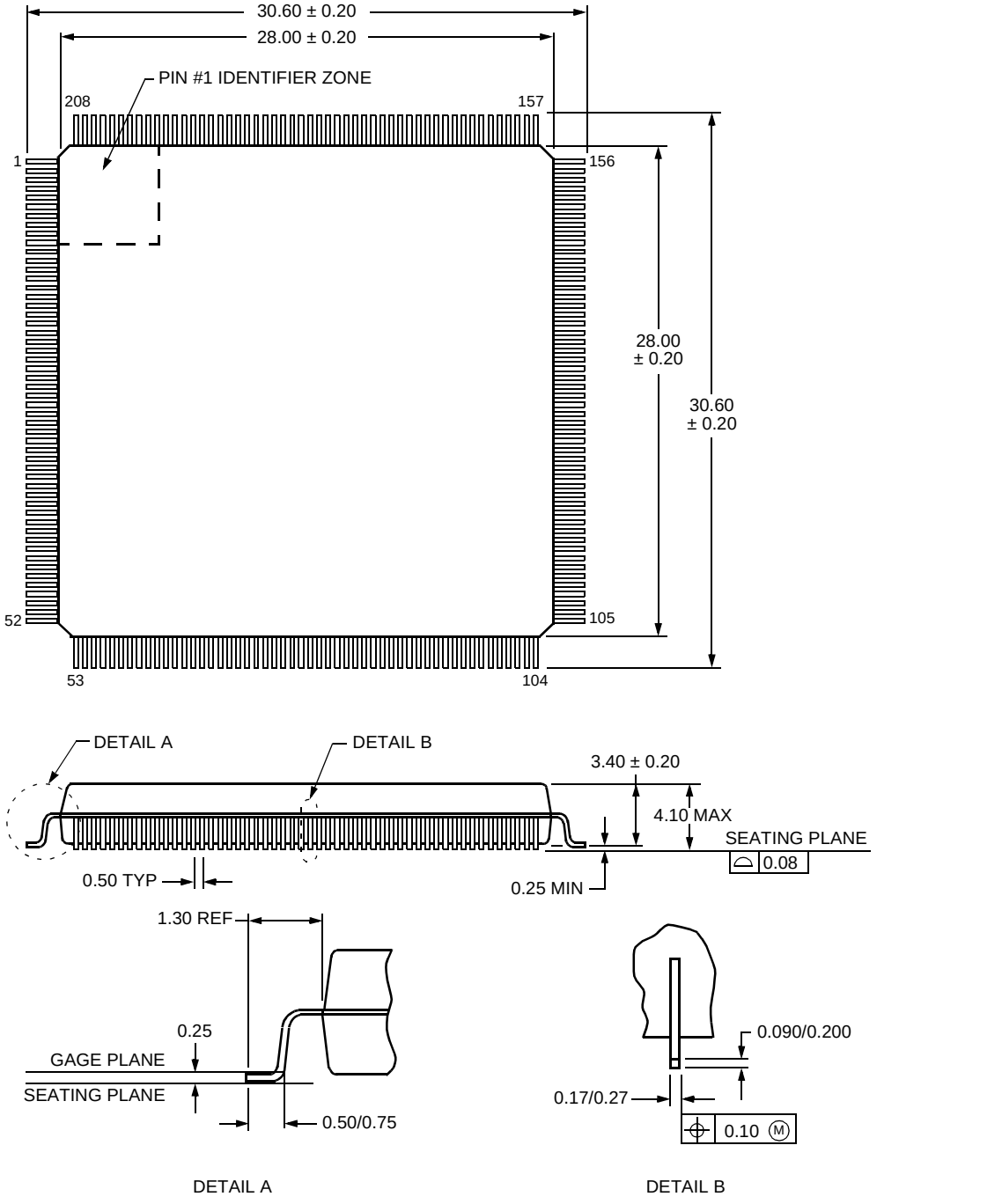
Figure 29. Microprocessor Access *Intel* Demultiplexed Read Cycle

Table 63. Microprocessor Access Timing (See Figure 24 through Figure 29.)

Symbol	Description	Min	Max	Condition	Unit
tAS	Address Setup Time	7	—	Load = 100 pF	ns
tAH	Address Hold Time	0	—	—	ns
tDV	Data Valid	—	13	—	ns
tDI	Data Invalid	0	11	—	ns
tRDY	Active to Ready Low (*Intel*)	—	14	Memory Access	ns
tIACC	Active to Ready High (*Intel*)	145	255	Memory Access	ns
tMACC	Active to $\overline{\text{DTACK}}$ Low (*Motorola*)	— 145	14 255	Register Access Memory Access	ns
tDS	Data Setup Time	8	—	—	ns
tDH	Data Hold Time	0	—	—	ns

5 Outline Diagram

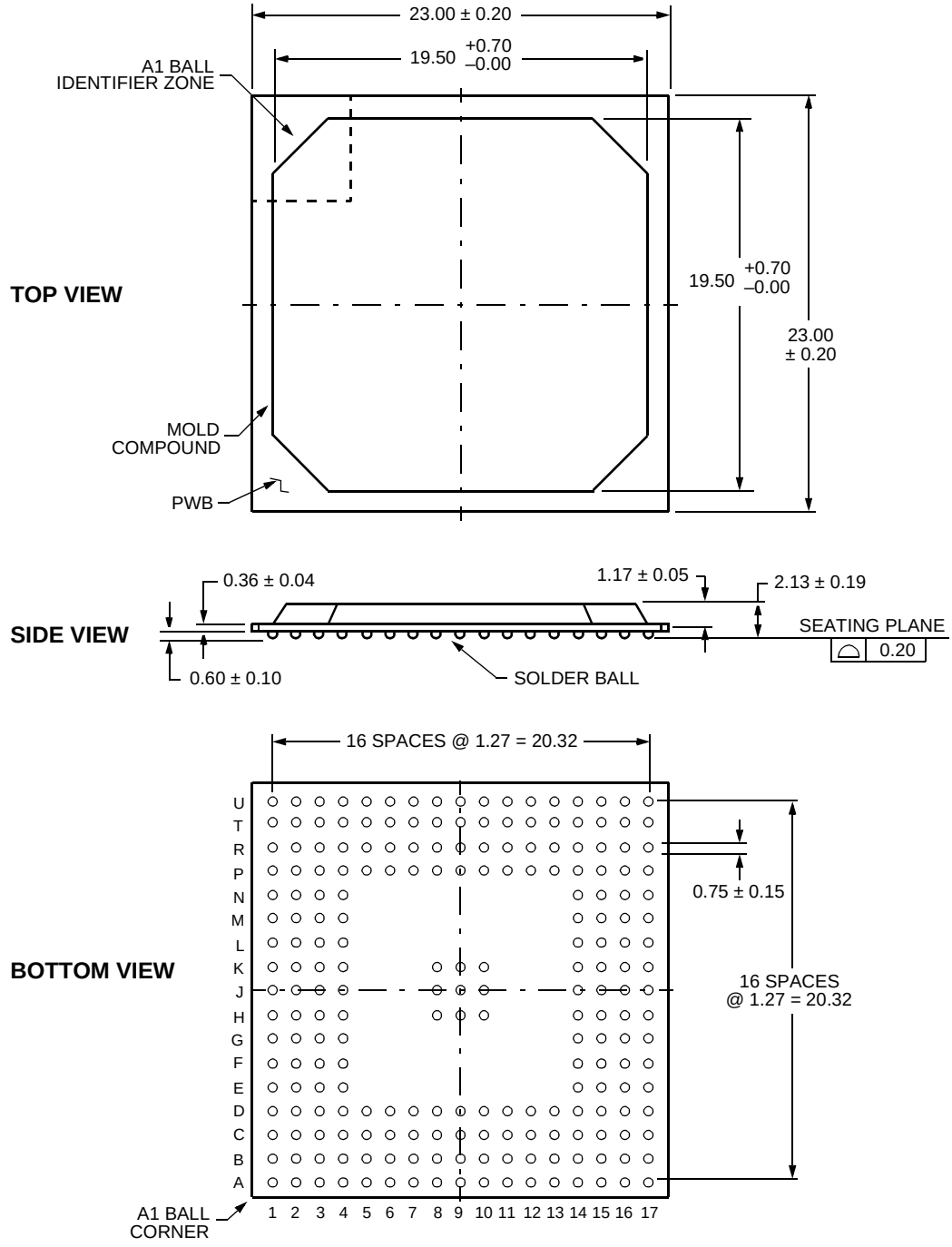
5.1 208-Pin Square Quad Flat Package (SQFP)



Note: The dimensions in this outline diagram are intended for informational purposes only. For detailed schematics to assist your design efforts, please contact your Lucent Technologies Microelectronics Group Account Manager.

5 Outline Diagram (continued)

5.2 217-Pin Ball Grid Array (PBGA)



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6 Ordering Information

Device Part No.	Description	Package	Comcode
T8100- - -SC	*Ambassador* H.100 Interface	208-Pin SQFP	108125873
T8100- - -BAL	*Ambassador* H.100 Interface	217-Pin BGA	108194184

Appendix A. Application of Clock Modes

In the diagrams that follow, four clock modes are illustrated using Figure 12, the T8100 clocking diagram, as the basis of each illustration. The key signal paths are shown in solid lines, and unused paths with narrow dashes. Two examples also indicate fallback paths. A register profile (programming values) for all four examples is on the last page of the appendix.

In Figure 30, the T8100 is operating as a bus master, so it must link to either an 8 kHz recovered frame reference or 2.048 MHz recovered bit clock reference from the E1 framers. In addition, the T8100 can provide one of the basic resource clocks to run the framers. In this case, the TCLK is selecting the T8100's 16.384 MHz oscillator. The framers are returning a 2.048 MHz bit clock which is selected through the clock selector. It is not divided, so the main divider is bypassed (divide-by-1), the clock is smoothed through an external DJAT, and the smooth 2.048 MHz signal is routed to PLL #1 through the clock resource selector. PLL #1 multiplies the 2.048 MHz input up to 65.536 MHz which, in turn, runs the rest of the T8100, all bus clocks, and the local clocks (if desired). If the T8100 is not providing NETREF generation, then the NETREF from the bus is routed to the local clocks via the NETREF internal/external selector. Since the NETREF generation resources are not needed here, the TODJAT and FROMDJAT pins are free for use with the general-purpose register as bits GP6 and GP7, respectively.

Figure 31 shows the T1 version of a bus master. In this scenario, a 1.544 MHz recovered bit clock from the framers is routed to a multiclock adapter (with built-in jitter attenuation) which produces smooth 4.096 MHz and 3.088 MHz outputs. The 4.096 MHz is routed up to PLL #1 for a times-16 rate multiplication to 65.536 MHz. This drives the bus clocks and the local clocks. The smooth 3.088 MHz is also rate multiplied times 8. This produces a 24.704 MHz clock. This is divided back down to produce a smooth 12.352 MHz which is fed back to the framers. (PLL outputs produce one tightly bound edge and one with significant phase jitter. Dividing a higher-frequency signal based on its clean edge produces a lower frequency with two clean edges.)

Figure 32 shows an H-*MVIP* slave arrangement for E1. In this example, the C16 differential clocks provide the main source for PLL #1. The 16.384 MHz signal is divided down to 4.096 MHz and then rate multiplied up to 65.536 MHz for driving the rest of the T8100. The frame sync for the state machines is derived from the /FRAME and C16 inputs as well as the state information provided by C2 and /C4.

Note: The bit slider is enabled for a smooth phase alignment between the internal frame and the frame sync.

The bus clocks are not driven, but the local clocks are available. A path for NETREF is shown as well, also based on a 2.048 MHz input. The signal is smoothed and then divided down to an 8 kHz signal via the NETREF divider. The internal oscillator is again chosen for routing to the framers via TCLK.

Figure 33 shows an H-*MVIP* slave for T1. This is identical to the E1 case with regard to slaving, and a NETREF path is illustrated in this example, too. The NETREF divider has been changed to accommodate the 1.544 MHz bit clock rate. The primary difference is the use of the C16 clock through the main divider to generate a 2.048 MHz signal which can be routed off-chip and adapted to a 1.544 MHz signal using an external device. The 1.544 MHz signal is returned to the T8100 via the 3MHzIN for rate multiplication up to 24.704 MHz and then division to a clean 12.352 MHz signal which is routed to the framers via TCLK.

Appendix A. Application of Clock Modes (continued)

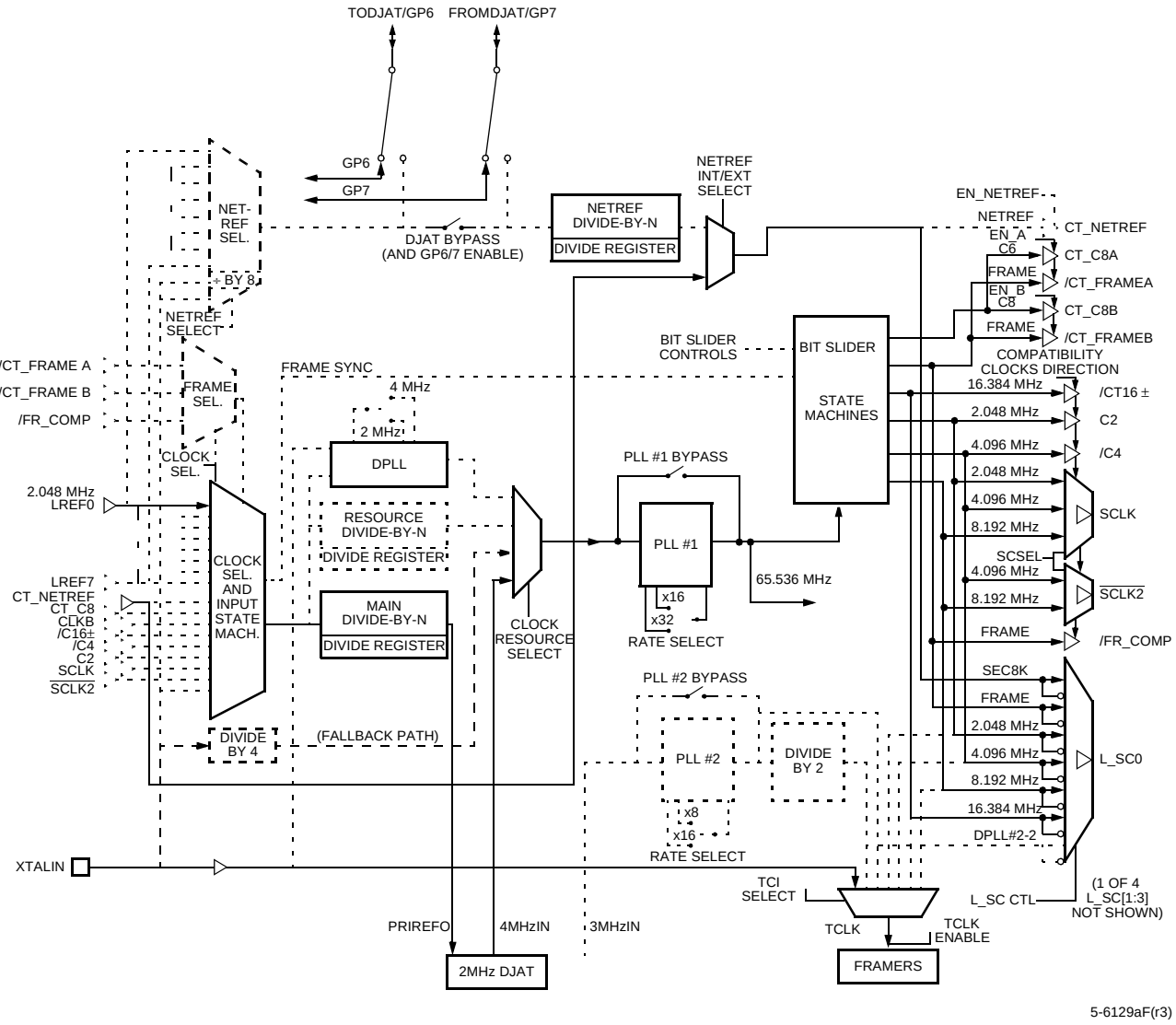


Figure 30. E1, CT Bus Master, Compatibility Clock Master, Clock Source = 2.048 MHz from Trunk

Appendix A. Application of Clock Modes (continued)

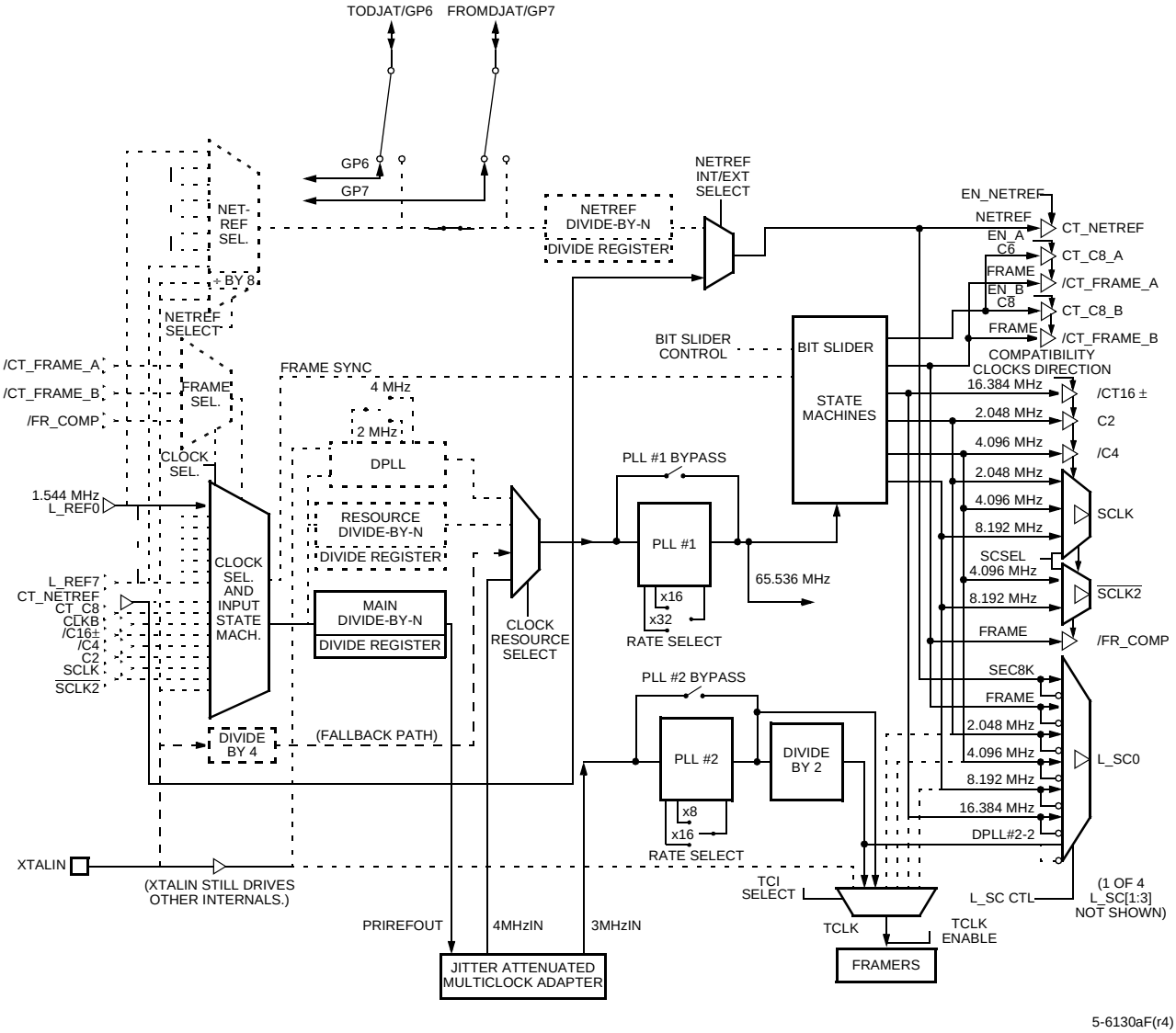


Figure 31. T1, CT Bus Master, Compatibility Clock Master, Clock Source = 1.544 MHz from Trunk

Appendix A. Application of Clock Modes (continued)

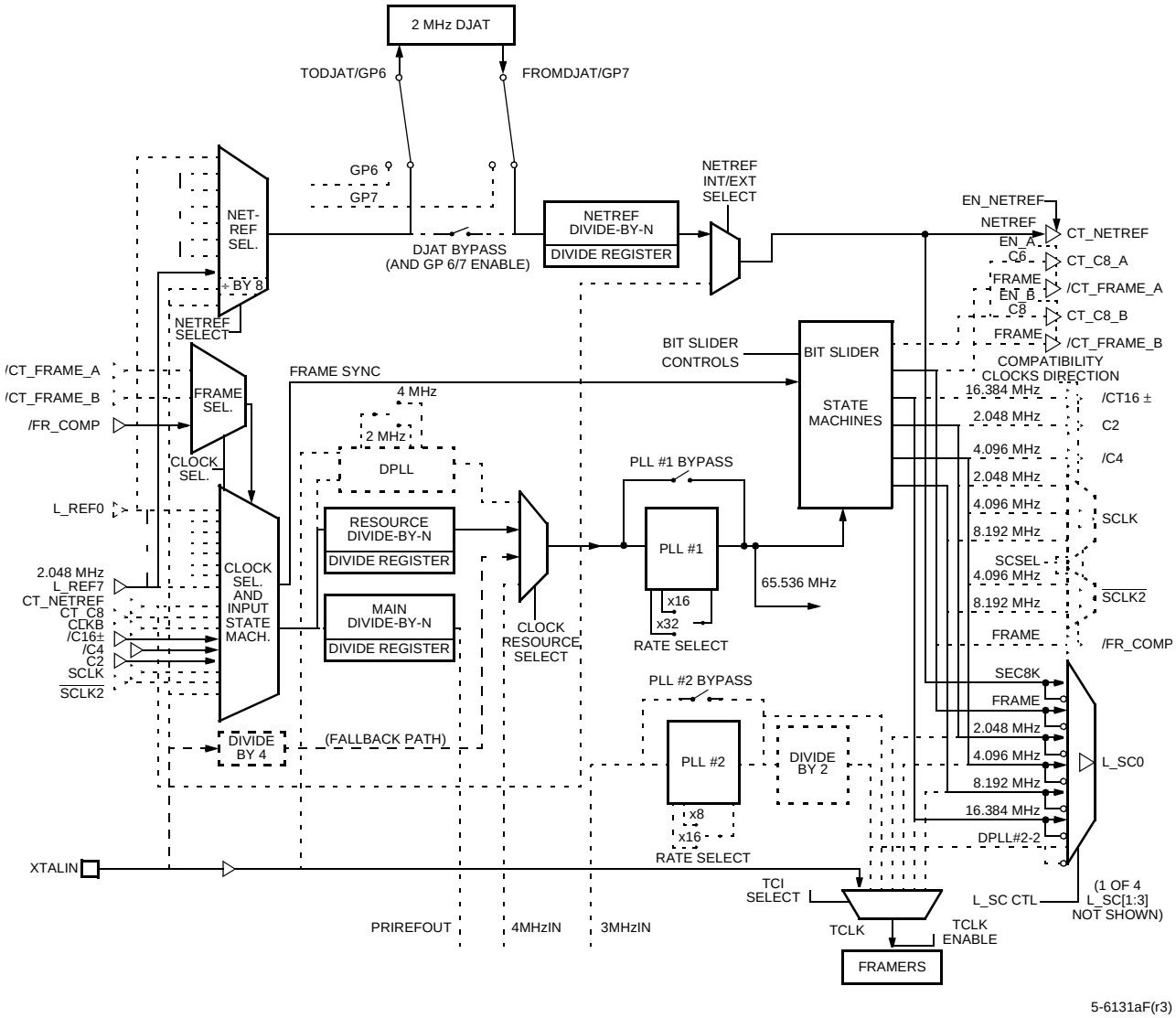


Figure 32. E1, Slave to CT Bus, Clock Source Is Either a 16 MHz or a 4 MHz or a 2 MHz and Frame, NETREF Source = 2.048 MHz from Trunk

Appendix A. Application of Clock Modes (continued)

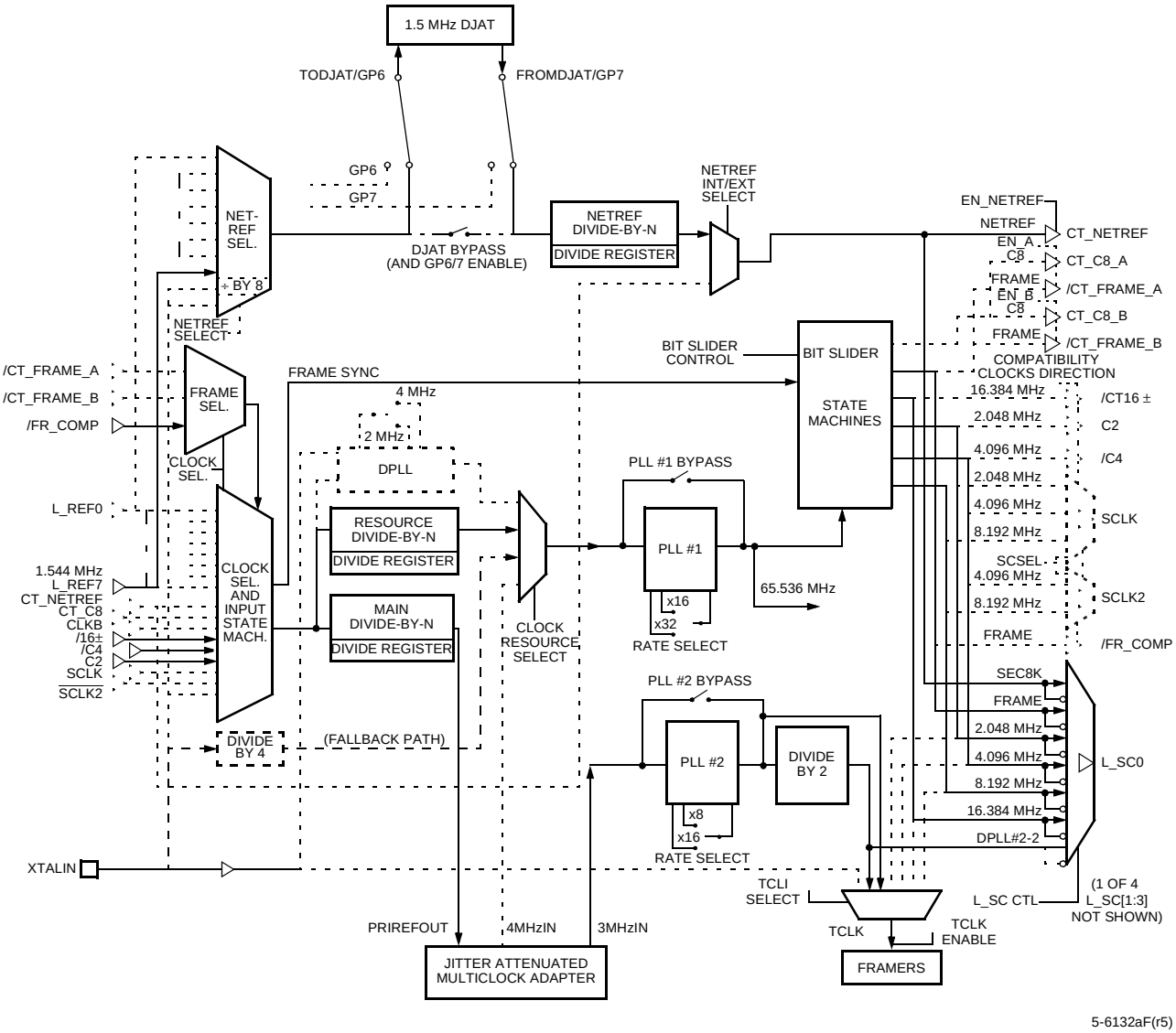


Figure 33. T1, Slave to CT Bus, Clock Source Is Either a 16 MHz or a 4 MHz or a 2 MHz and Frame, NETREF Source = 1.544 MHz from Trunk

Appendix A. Application of Clock Modes (continued)

Table 64. Clock Register Programming Profile for the Four Previous Examples

Register Name	CT Bus Master (E1)	CT Bus Master (T1)	CT Bus Slave (E1)	CT Bus Slave (T1)
CKM	0010_1000b	0010_1000b	1100_0101b	1100_0101b
CKN	0110_0000b	0110_0000b	1000_1111b	1000_1111b
CKP	0010_0001b	0110_0001b	0010_0000b	0110_0000b
CKR	0001_0000b	0000_0000b	0100_0000b	0100_0000b
CKS	0000_0000b	0000_0000b	0000_0000b	0000_0000b
CK32	1001_0100b	1001_0100b	0010_0100b	0010_0100b
CK10	1101_1111b	1101_1111b	1000_0000b	1011_1101b
CKMD	0000_0000b	0000_0000b	0000_0000b	0000_0111b
CKND	0000_0000b	0000_0000b	1111_1111b	1100_0000b
CKRD	0000_0000b	0000_0000b	0000_0011b	0000_0011b
Watchdog: CKW	0011_1001b	0011_1001b	0011_1001b	0011_1001b

The programming displays how similar the four basic modes of operation are. Local outputs (CK32 and CK10) are obviously not constrained by the mode of operation. The primary difference between E1 and T1 is in the use of the PLL #2 (which is optional). The primary difference between master and slave is in the clock path to PLL #1, which is covered by registers CKM, CKR, CKMD, and CKRD.

Note: CKR does include an example of running PLL #1 at X32 for E1 master and X16 for all other cases.

The watchdogs have been set up to monitor all CT Bus signals, though fallback (to the oscillator) is shown as enabled in all examples. It is recommended that the default condition, CKS = 0x00, be used for systems which do not have specific fallback clocking schemes. Also, while programming the T8100 on powerup, it is recommended that the watchdogs are disabled (CKW = 0x00) until the device is fully programmed to prevent false error conditions (uninitialized clocks, for example) from changing the operating mode.

Appendix B. Minimum Delay and Constant Delay Connections

B.1 Connection Definitions

Forward Connection	A forward connection is defined as one in which the output (**to**) time slot has a greater value than the input (**from**) time slot, or put another way, the delta between them is positive.
Reverse Connection	A reverse connection is defined as one in which the input (**from**) time slot has a lesser value than the output (**to**) time slot, and the delta between them is negative.

So, for example, going from TS(1) to TS(38) is a forward connection, and the TSΔ is +37, but going from TS(38) to TS(1) is a reverse connection, with a TSΔ of –37:

where TSΔ = TS(**to**) – TS(**from**).

Similarly, a delta can be introduced for streams which will have a bearing in certain exceptions (discussed later):

STRΔ = STR(**to**) – STR(**from**)

There is only one combination which forms a TSΔ of +127 or –127:

TSΔ = TS(127) – TS(0) = +127, and
TSΔ = TS(0) – TS(127) = –127,

but there are two combinations which form TSΔs of +126 or –126:

TSΔ = TS(127) – TS(1) = TS(126) – TS(0) = +126, and
TSΔ = TS(1) – TS(127) = TS(0) – TS(126) = –126,

there are three combinations which yield +125 or –125, and so on.

The user can utilize the TSΔ to control the latency of the resulting connection. In some cases, the latency must be minimized. In other cases, such as a block of connections which must maintain some relative integrity while crossing a frame boundary, the required latency of some of the connections may exceed one frame (>128 time slots) to maintain the integrity of this virtual frame.

The T8100 contains several bits for controlling latency. Each connection has a bit which is used for selecting one of two alternating data buffers. These bits are set in the local connection memory for local switching or in the tag register files of the CAM section for H-Bus switching. There are also 2 bits in the CON register, address 0x0E, which can control the buffer selection on a chip-wide basis. Bit 1 of the register overrides the individual FME bits. Bit 0 becomes the global, chip-wide, FME setting.

Appendix B. Minimum Delay and Constant Delay Connections (continued)

B.2 Delay Type Definitions

Constant Delay In the T8100, this is a well-defined, predictable, and linear region of latency in which the **to** time slot is at least 128 time slots after the **from** time slot, but no more than 256 time slots after the **from** time slot.

Mathematically, constant delay latency is described as follows*, with L denoting latency, and FME set to the value indicated:

Forward Connections, FME = 1: $L = 128 + TS\Delta$ ($0 \le TS\Delta \le 127$)

Reverse Connections, FME = 0: $L = 256 + TS\Delta$ ($-127 \le TS\Delta \le 0$)

Example: Switching from TS(37) to TS(1) as a constant delay, the delta is –36, so FME is set to 0 and the resulting latency is 256 – 36 = 220 time slots. Thus, the connection will be made from TS(37) of Frame(n) to TS(1) of Frame(n + 2).

Simple Summary: Use constant delay for latencies of 128 to 256 time slots, set FME = 1 for forward connections, set FME = 0 for reverse connections.

* Since $TS\Delta = TS(to) - TS(from)$, the user can modify the equations to solve for either TS(to) or TS(from).

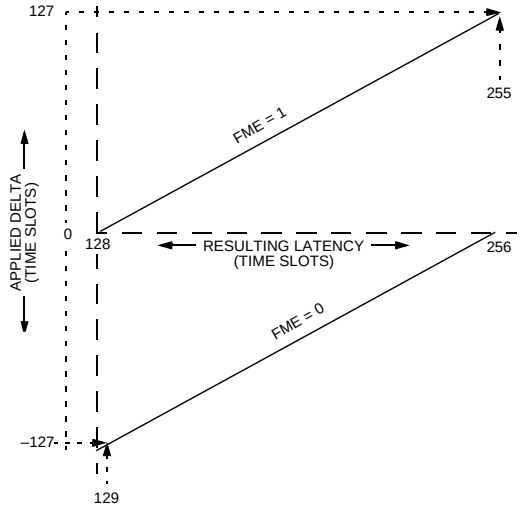
Minimum Delay This is the most common type of switching, but has a shorter range than constant delay, and the user must be aware of exceptions caused by interactions between the T8100's internal pipeline and the dual buffering. The **to** time slot is at least three time slots after the **from** time slot, but no more than 128 time slots after the **from** time slot. Exceptions exist at $TS\Delta$s of +1, +2, –126, and –127.

Forward Connections, FME = 0: $L = TS\Delta$ ($3 \le TS\Delta \le 127$)

Reverse Connections, FME = 1: $L = 128 + TS\Delta$ ($-125 \le TS\Delta \le 0$)

Example: Using the same switching from the example above, TS(37) to TS(1), the delta is –36, so FME is set to 1 to effect the minimum delay (setting to 0 effects constant delay), and the resulting latency is 128 – 36 = 92 time slots. The relative positions of the end time slots are the same in both minimum and constant delay (i.e., they both switch to TS[1]), but the actual data is delayed by an additional frame in the constant delay case.

Simple Summary: Use minimum delay for latencies of 3 to 128 time slots, set FME = 0 for forward connections, set FME = 1 for reverse connections.



5-6223 (F)

Figure 34. Constant Delay Connections, CON[1:0] = 0X

Appendix B. Minimum Delay and Constant Delay Connections (continued)

B.2 Delay Type Definitions (continued)

B.2.1 Exceptions to Minimum Delay

Up until this point in the discussion, the STRDs have not been discussed because the **to** and **from** streams have been irrelevant in the switching process*. Rather than try to list the exceptions mathematically, a table is provided. The latencies in these cases may exceed two frames due to the interaction of the intrinsic pipeline delays with the double buffering.

Table 65. Table of Special Cases (Exceptions)

FME Value	TSΔ	Latency for STRΔ < 0	Latency for STRΔ ≥ 0
0	+1	257	257
0	+2	258	2
1	–126	258	2
1	–127	257	257

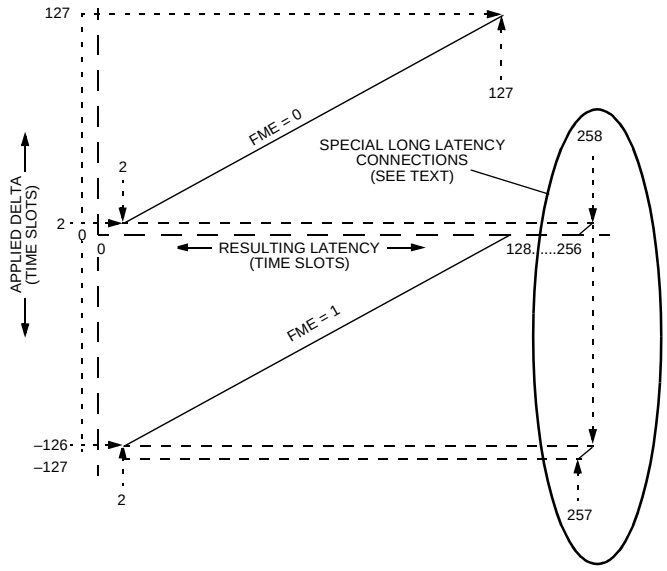
Graphically, the minimum delay latency equations are illustrated below. The exceptions to the minimum delay have been included in the diagram, connected to the main function by dashed lines.

B.2.2 Lower Stream Rates

The discussion has centered on 128 time-slot frames which correspond to 8.192 Mbits/s data rates. How does one make similar predictions for lower stream rates?

For 4.096 Mbits/s, multiply the **to** and **from** time-slot values by two, i.e., time slot 0 at 4.096 Mbits/s corresponds to time slot 0 at 8.192 Mbits/s, and time slot 63 at 4.096 Mbits/s corresponds to time slot 126 at 8.192 Mbits/s. Similarly, multiply values by four to convert 2.048 Mbits/s values. The latency equations can then be applied directly.

* The one universally disallowed connection on the T8100 is a TSΔ of 0 and a STRΔ of 0. This is a stream and time-slot switching to itself. Loopback on the local bus, e.g., LDO_0 to LDI_0 is permissible.



5-6224(F)

Figure 35. Minimum Delay Connections, CON[1:0] = 0X

Appendix B. Minimum Delay and Constant Delay Connections (continued)

B.2 Delay Type Definitions (continued)

B.2.3 Mixed Minimum/Constant Delay

An interesting mix of delays occurs when the individual FME bits are overridden and a chip-wide selection for FME is used. In short, when the T8100 is placed in this mode, and when register bits CON[1:0] = 10, forward connections provide minimum delay, reverse connections provide constant delay. When CON[1:0] = 11, reverse connections provide minimum delay, forward connections provide constant delay. The latter is interesting because, graphically, the TSΔ to latency mapping appears as a linear monotonic function covering 255 time slots. (Graphs are in the section which follows.) The latency equations follow:

CON[1:0] = 10:

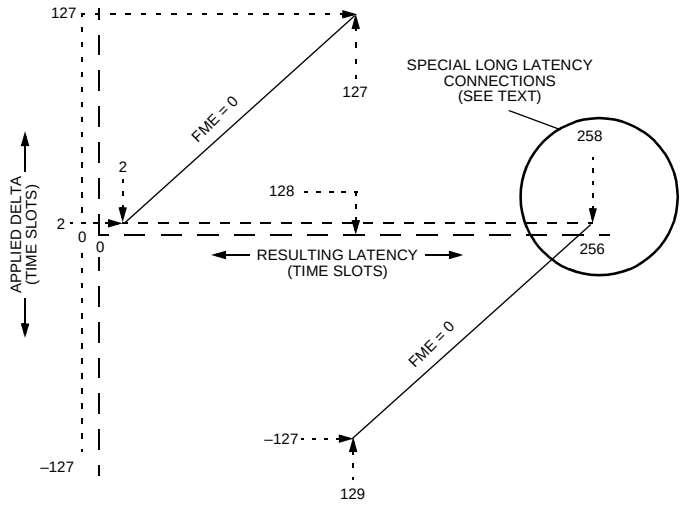
Forward Connections: L = TSΔ (3 ≤ TSΔ ≤ 127).

Reverse Connections: L = 256 + TSΔ (–127 ≤ TSΔ ≤ 0).

CON[1:0] = 11:

Forward and Reverse: L = 128 + TSΔ (–125 ≤ TSΔ ≤ 127).

Table 65, Table of Special Cases (Exceptions), applies to the mixed delays in a similar manner. Simply use bit 0 of CON for the FME value in Table 65.



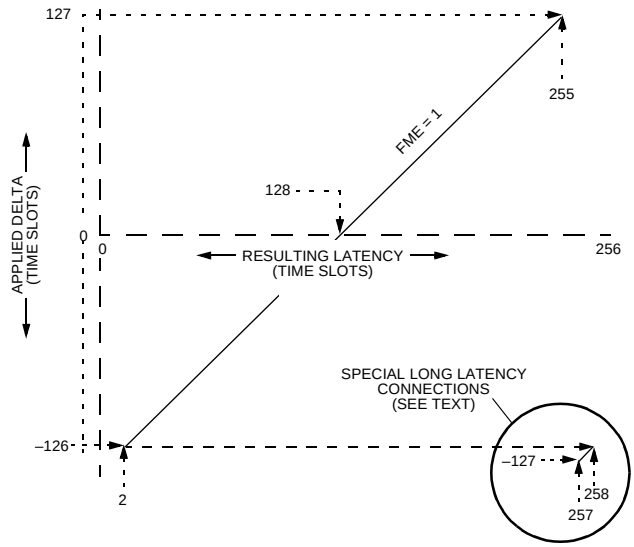
5-6225(F)

Figure 36. Mixed Minimum/Constant Delay Connections, CON[1:0 = 10]

Appendix B. Minimum Delay and Constant Delay Connections (continued)

B.2 Delay Type Definitions (continued)

B.2.3 Mixed Minimum/Constant Delay (continued)



5-6226(F)

Figure 37. Extended Linear (Mixed Minimum/Constant) Delay, CON[1:0] = 11

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