



T7115A Synchronous Protocol Data Formatter

Features

Serial Port Interface

- 32-channel (full-duplex), multiplexed, serial input/output HDLC processing
- Support for T1/DS1 24-channel and CEPT/E1 32-channel modes
- Automatic flag transmission and detection
- Flag stuffing up to 2,047 flags
- Flag adjustment for synchronous rate adaption
- Full, partial, or no CRC generation and checking
- Zero-bit insertion and deletion
- Abort/idle detection and transmission
- Long-frame detection
- 2 Mbits/s continuous serial data rate
- Transparent mode (no protocol) supports ECMA 102 and ITU-T I.463 RA2 rate adaption standards

- Dynamic channel allocation (or channel concatenation) supports DS0, H0, H11, and H12 channels and other channel rates
- Bit-rate control on each channel
- Channel inversion
- Loopback mode
- DMA CRC for relay mode

Microprocessor Interface

- Compatibility with 16-bit or 32-bit microprocessor systems
- On-chip, 64-channel, DMA memory address generator and buffer manager
- Interrupt queue (up to 4,096 interrupts)
- Nonmultiplexed 16-bit data and 24-bit address (8 Mwords) buses
- Transmit and receive buffers accessible through memory-mapped look-up tables

Description

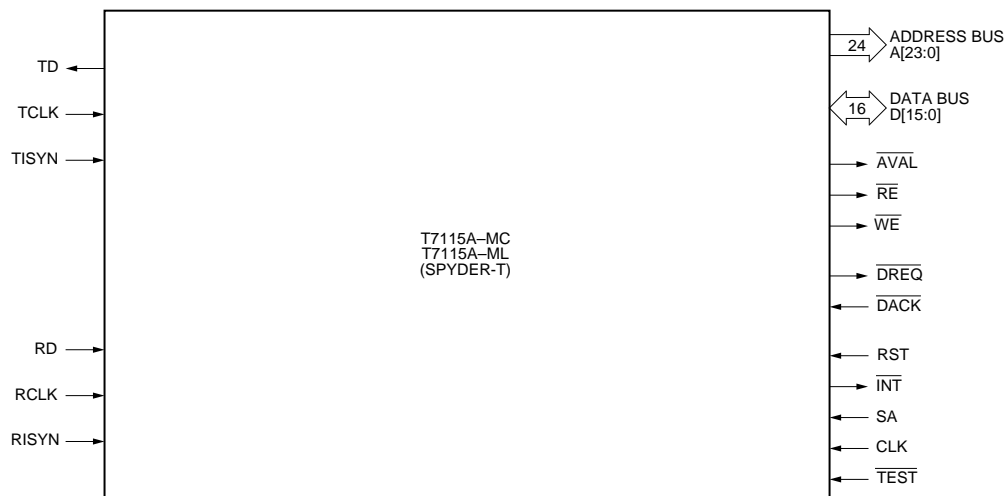
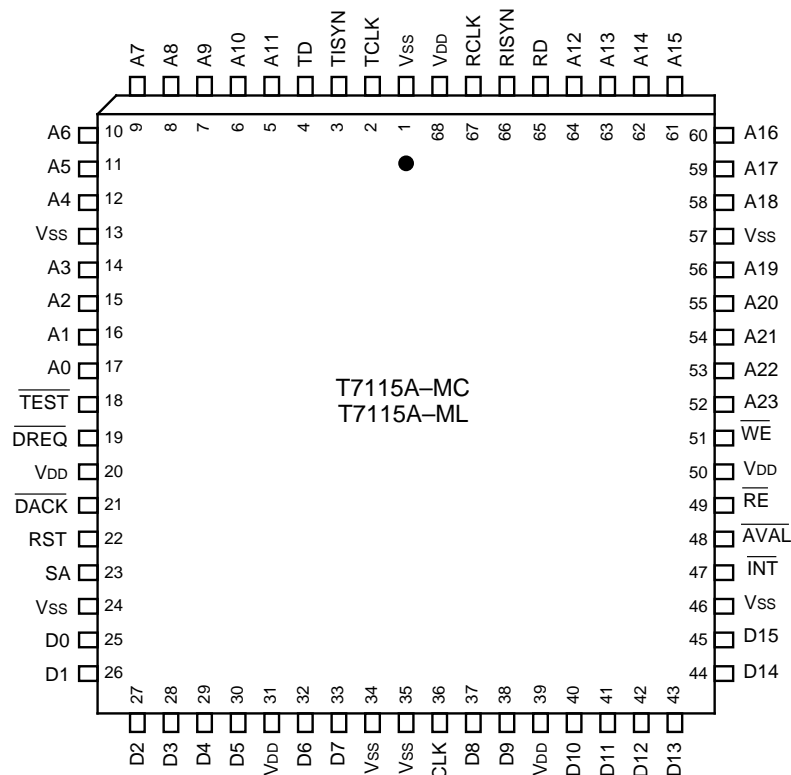


Figure 1. Simplified Block Diagram

Description (continued)

The Lucent Technologies Microelectronics Group T7115A Synchronous Protocol Data Formatter (SPYDER-T) integrated circuit is an extremely flexible 32-channel HDLC/DMA controller. The device can be used in a variety of data and signaling applications to provide cost-effective DS1/E1 line termination or multiple D-channel termination. All inputs and outputs of the T7115A SPYDER-T are TTL compatible. The device is fabricated by using CMOS technology, requires a single 5 V supply, and is available in a 68-pin, plastic leaded chip carrier.

Pin Information



5-2307(C)

Figure 2. Pin Diagram Industry-Standard Numbering Convention

For additional information, contact your Microelectronics Group Account Manager or the following:

INTERNET: <http://www.lucent.com/micro>

U.S.A.: Microelectronics Group, Lucent Technologies Inc., 555 Union Boulevard, Room 30L-15P-BA, Allentown, PA 18103

1-800-372-2447, FAX 610-712-4106 (In CANADA: **1-800-553-2448**, FAX 610-712-4106), e-mail docmaster@micro.lucent.com

ASIA PACIFIC: Microelectronics Group, Lucent Technologies Singapore Pte. Ltd., 77 Science Park Drive, #03-18 Cintech III, Singapore 118256

Tel. (65) 778 8833, FAX (65) 777 7495

JAPAN: Microelectronics Group, Lucent Technologies Japan Ltd., 7-18, Higashi-Gotanda 2-chome, Shinagawa-ku, Tokyo 141, Japan

Tel. (81) 3 5421 1600, FAX (81) 3 5421 1700

For data requests in Europe:

MICROELECTRONICS GROUP DATALINE: **Tel. (44) 1734 324 299**, FAX (44) 1734 328 148

For technical inquiries in Europe:

CENTRAL EUROPE: **(49) 89 95086 0** (Munich), NORTHERN EUROPE: **(44) 1344 865 900** (Bracknell UK),

FRANCE: **(33) 1 41 45 77 00** (Paris), SOUTHERN EUROPE: **(39) 2 6601 1800** (Milan) or **(34) 1 807 1700** (Madrid)

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