LITE-ON SEMICONDUCTOR

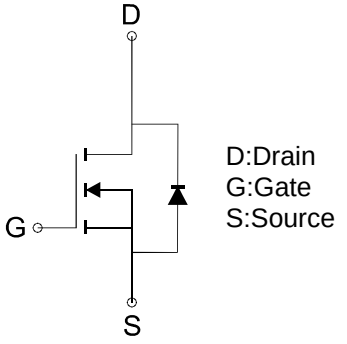
S2TB200N65R

N-Channel 650V Enhancement Mode Power MOSFET

General Description

S2TB200N65R provide low $R_{DS(ON)}$, low gate charge, fast switching and excellent avalanche characteristics. This device is suitable for active power factor correction and switching mode power supply applications.

$V_{DS,Tj(max)}$=700V ,
$R_{DS(ON)}$ ≦200mΩ@V_{GS}=10V
$I_{D,pulse}$= 60A

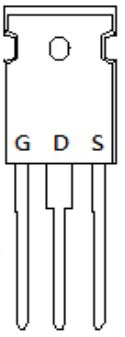


N-Channel MOSFET

Features

- Low $R_{DS(ON)}$ & FOM
- Extremely low switching loss
- Excellent stability and uniformity
- Easy to drive
- Marking: S2TB200N65R
- Weight: 6.1 g
- RoHS Compliant
- Qualified according to JEDEC

(TO-247)
Top View



Application

- Lighting
- Hard switching PWM
- Server power supply
- Charger

Absolute Maximum Ratings (T_A=25°C Unless Otherwise Noted)

PARAMETER		SYMBOL	VALUE	UNIT
Drain-Source Voltage		V_{DS}	650	V
Gate-Source Voltage		V_{GS}	±30	V
Continuous Drain Current[1]	T_c=25°C	I_D	20	A
Pulsed Drain Current[2]		I_{DM}	60	A
Power Dissipation[3]	T_c=25°C	P_D	179	W
Single pulsed avalanche energy[5]		E_{AS}	600	mJ
Reverse diode dv/dt, V_{DS}=0…400 V, I_{SD}≤I_D		dv/dt	6.3	V/nS
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to150	°C

Thermal Characteristics

PARAMETER	SYMBOL	TYP	UNIT
Thermal Resistance Junction-to-Case	R_{thJC}	0.7	°C /W
Thermal Resistance Junction-to-Ambient[4]	R_{thJA}	4	

N-Channel 650V Enhancement Mode Power MOSFET

Electrical Characteristics (T_A =25°C Unless Otherwise Specified)

PARAMETER	TEST CONDITION	SYMBOL	MIN	TYP	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	V_{GS}=0V,I_D=250uA	$V_{(BR)DSS}$	650	--	--	V
	V_{GS}=0V,I_D=250uA,TJ=150°C		700	--	--	
Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250uA	$V_{GS(th)}$	2.0	--	4.0	V
Gate-Source Leakage	V_{DS}=0V, V_{GS}=±30V	I_{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V_{DS}=650V,V_{GS}=0V	I_{DSS}	--	--	1	uA
Drain-Source On-Resistance	V_{GS}=10V,I_D=10A	$R_{DS(ON)}$	--	--	0.2	Ω
DYNAMIC						
Total Gate Charge	V_{GS}=10V,V_{DS}=520V, I_D=20A	Q_g	--	25	--	nC
Gate-Source Charge		Q_{gs}	--	10.1	--	
Gate-Drain Charge		Q_{gd}	--	6.4	--	
Gate plateau voltage		$V_{plateau}$	--	6.3	--	V
Input Capacitance	V_{GS}=0V,V_{DS}=50V, F=1MHz	C_{iss}	--	1556.1	--	pF
Output Capacitance		C_{oss}	--	107.5	--	
Reverse Transfer Capacitance		C_{rss}	--	19	--	
Gate Resistance	V_{GS}=0V,V_{DS}=0V, F=1MHz	R_g	--	18.1	--	Ω
Turn-On Delay Time	V_{GS} = 10V, V_{DS} = 520V, R_G = 22Ω, I_D=20A	$t_{d(on)}$	--	42.5	--	nS
Turn-On Rise Time		t_r	--	68.2	--	
Turn-Off Delay Time		$t_{d(off)}$	--	69.1	--	
Turn-Off Fall Time		t_f	--	57.1	--	
Source-Drain Diode						
Diode forward current	V_{GS}<V_{th}	I_S	--	--	20	A
Pulsed source current		I_{SP}	--	--	60	
Diode forward voltage	I_S=20A, V_{GS}=0 V	V_{SD}	--	--	1.4	V
Reverse recovery time	V_R=400 V, I_S=20A, dI/dt=100 A/μs	t_{rr}	--	365.5	--	nS
Reverse recovery charge		Q_{rr}	--	5.3	--	uC
Peak reverse recovery current		I_{rrm}	--	30.9	--	A

Notes:

(1). Calculated continuous current based on maximum allowable junction temperature.
(2). Repetitive rating; pulse width limited by max. junction temperature.
(3). Pd is based on max. junction temperature, using junction-case thermal resistance.
(4). The value of $R_{\theta JC}$ is measured with the device mounted on fin-type heatsink 100mm x 75mm x 27mm, in a still air environment with T_a=25 °C.
(5). V_{DD}=150 V, R_G=25 Ω, L=15mH, starting T_j=25 °C.
(6). LiteON Semiconductor reserves the right to improve product design, functions and reliability without notice.

N-Channel 650V Enhancement Mode Power MOSFET

FIG.1- On-Region Characteristics

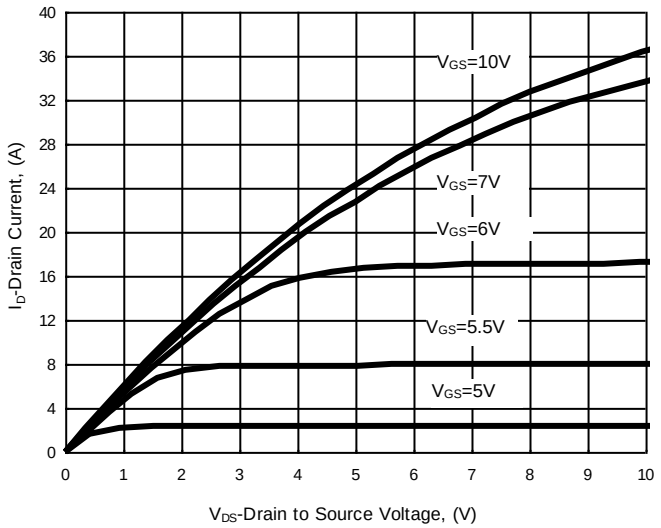


FIG.2- Transfer Characteristics

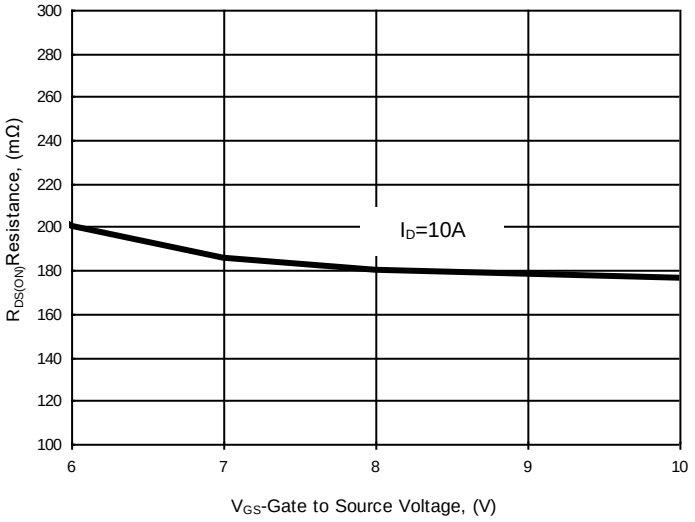


FIG.3- On-Resistance Characteristics

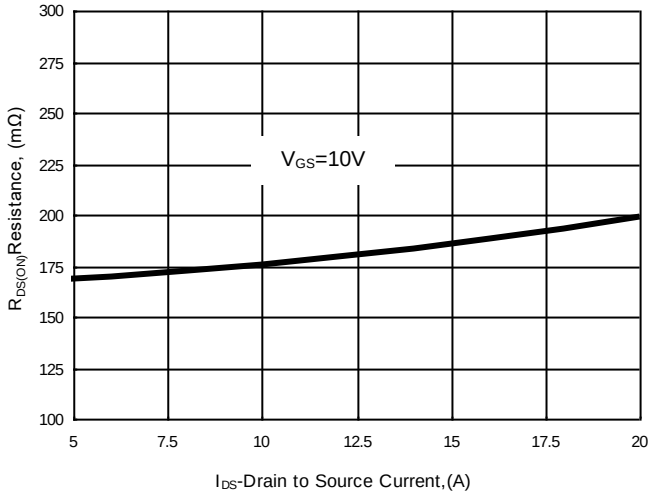


FIG.4- Source - Drain Diode Forward

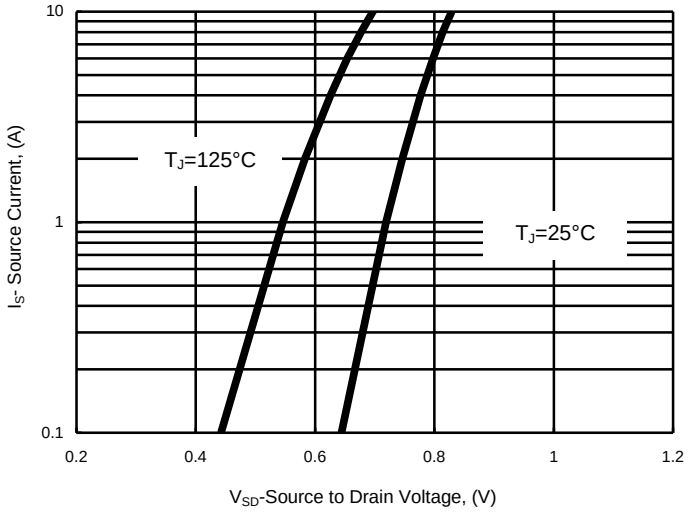


FIG.5- On-Resistance VS Junction Temp

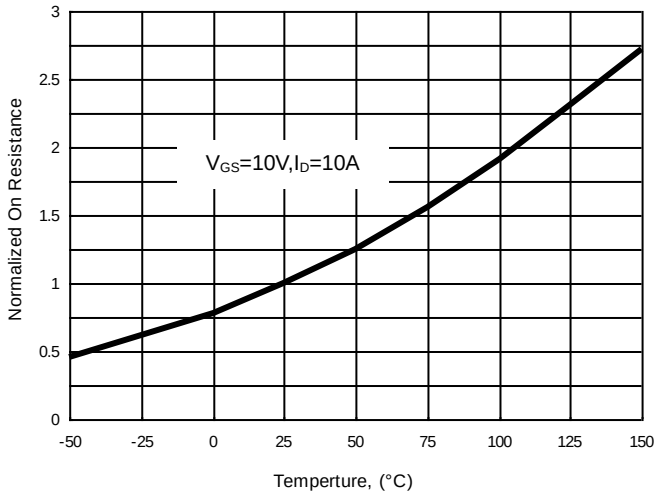


FIG.6- Threshold VS Junction Temp

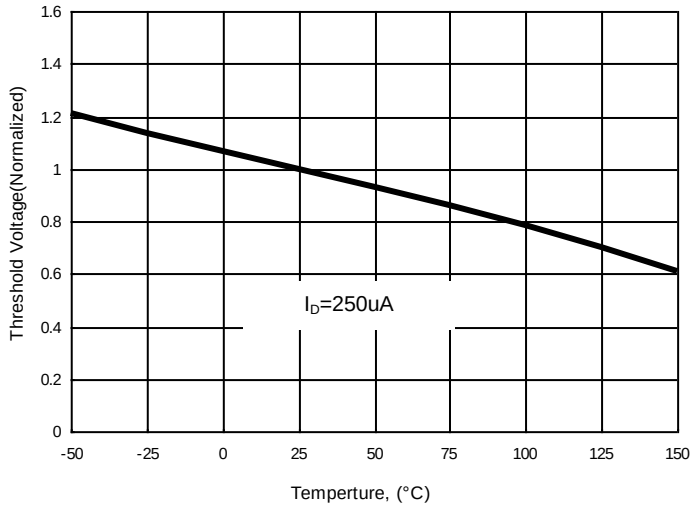


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FIG.7- Drain Current

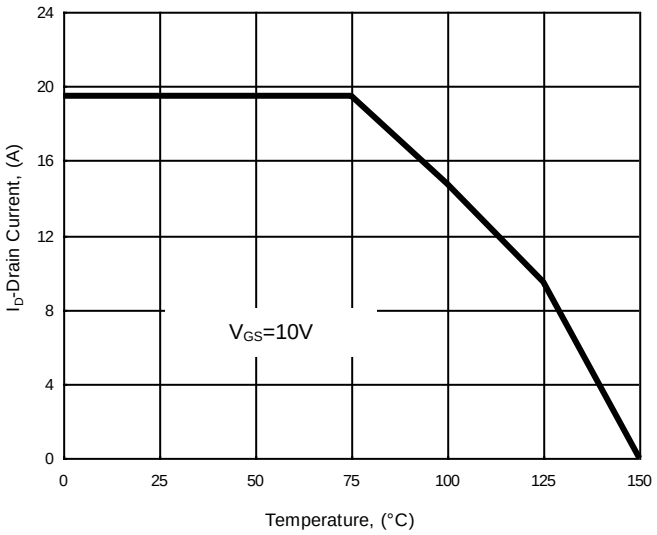


FIG.8- Power Dissipation

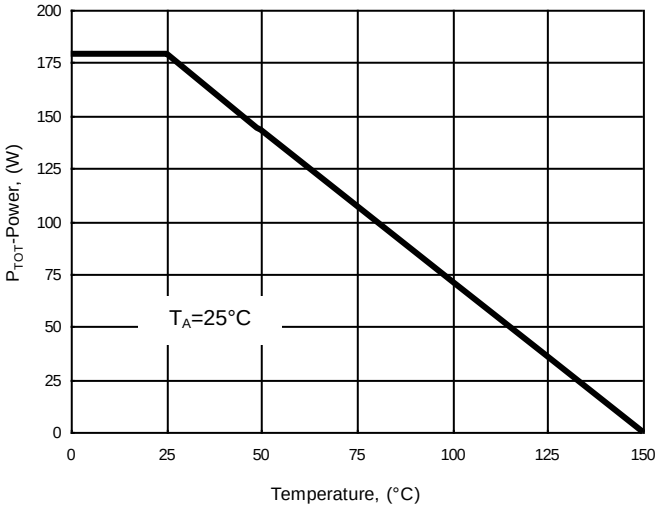


FIG.9- Gate Charge

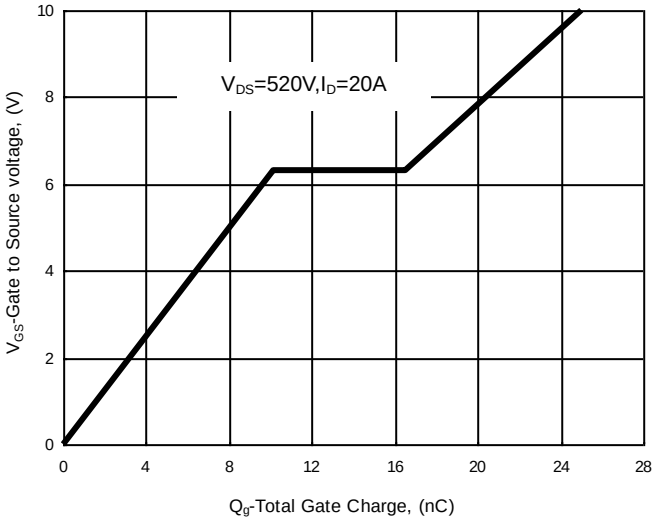


FIG.10- Capacitance

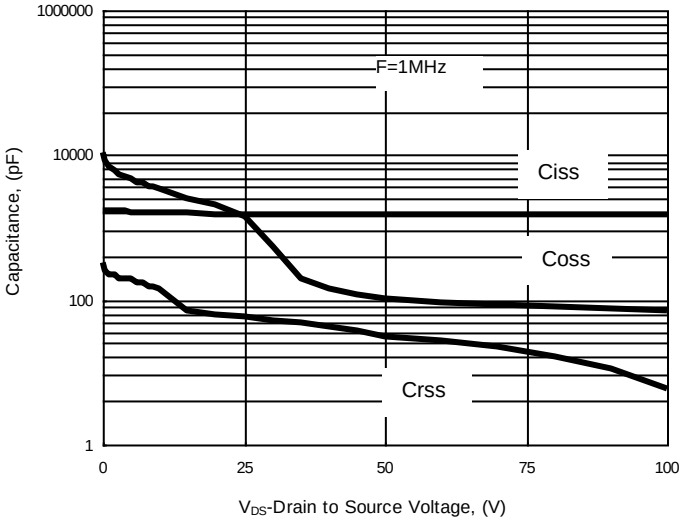


FIG.11- Safe Operation Area

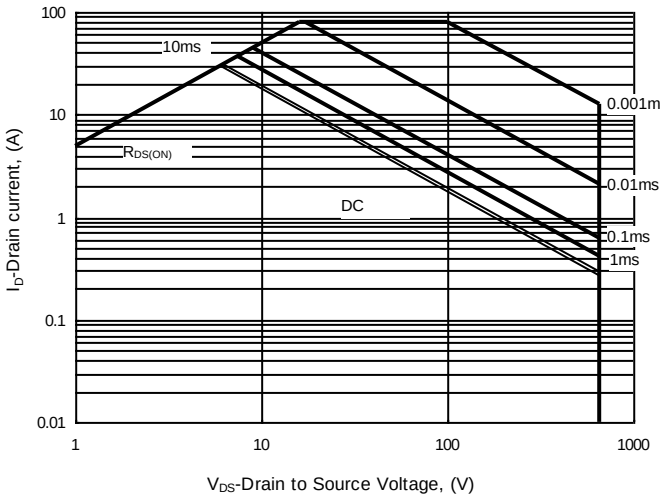
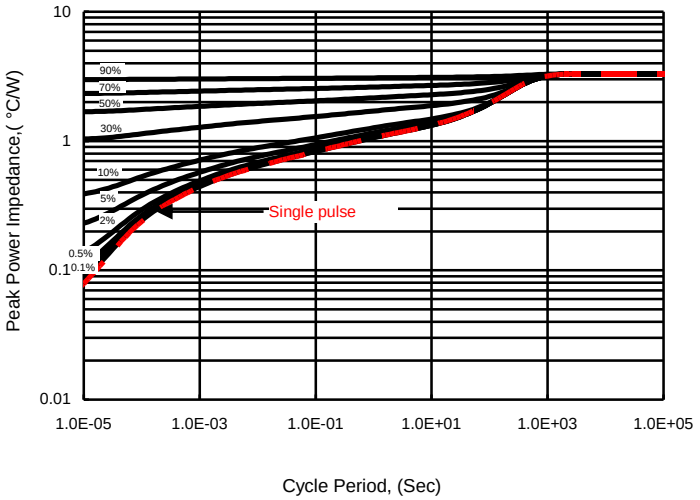


FIG.12- Thermal Transient Impedance



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Test circuit and waveforms

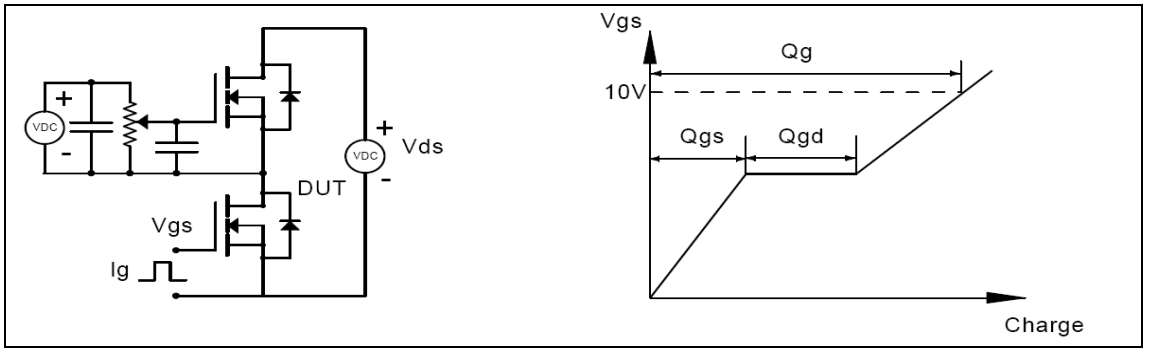

Figure 1, Gate charge test circuit & waveform

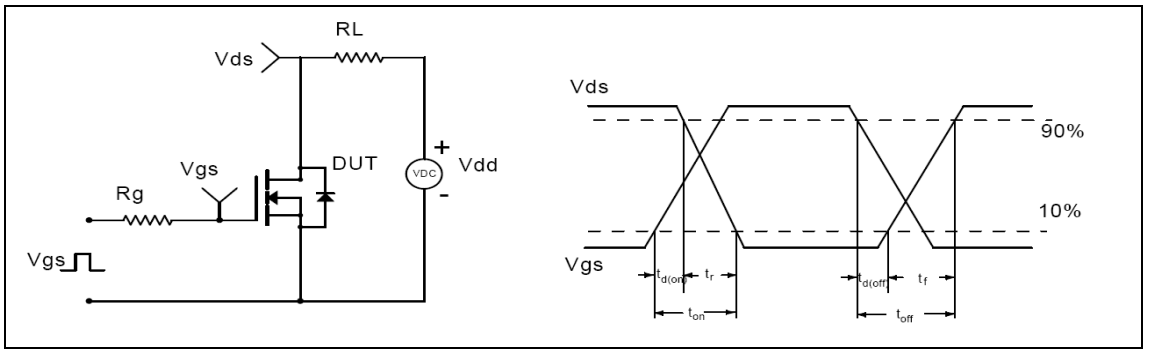

Figure 2, Switching time test circuit & waveforms

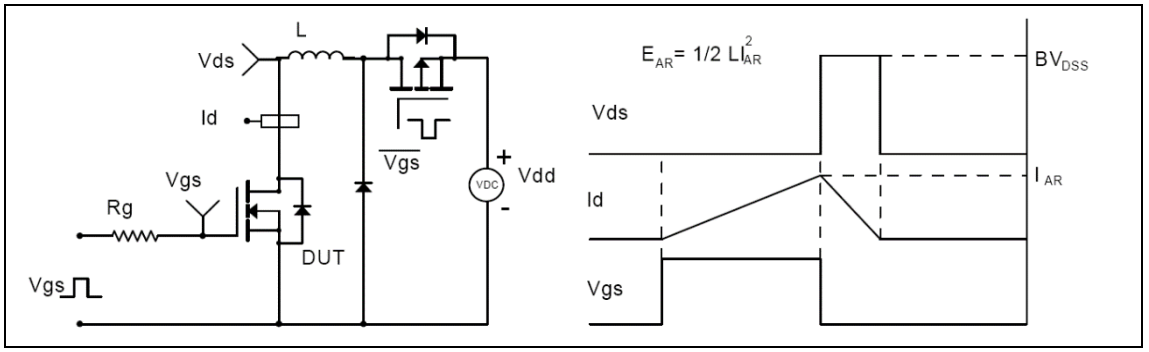

Figure 3, Unclamped inductive switching (UIS) test circuit & waveforms

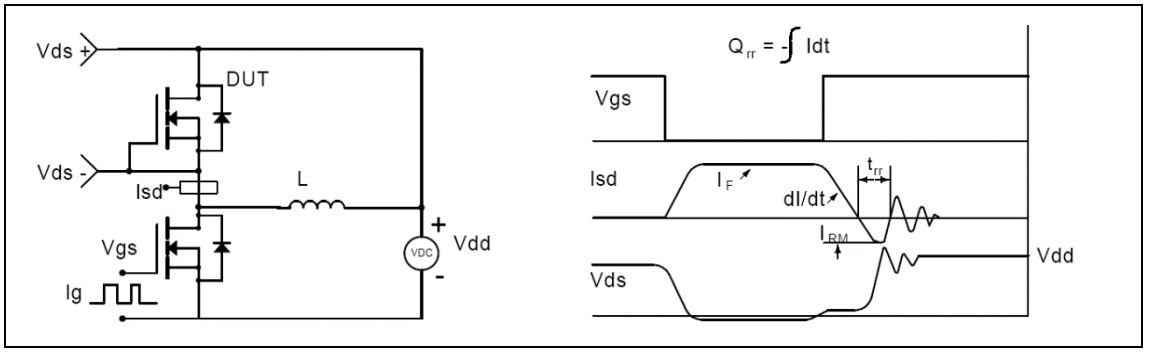

Figure 4, Diode reverse recovery test circuit & waveforms

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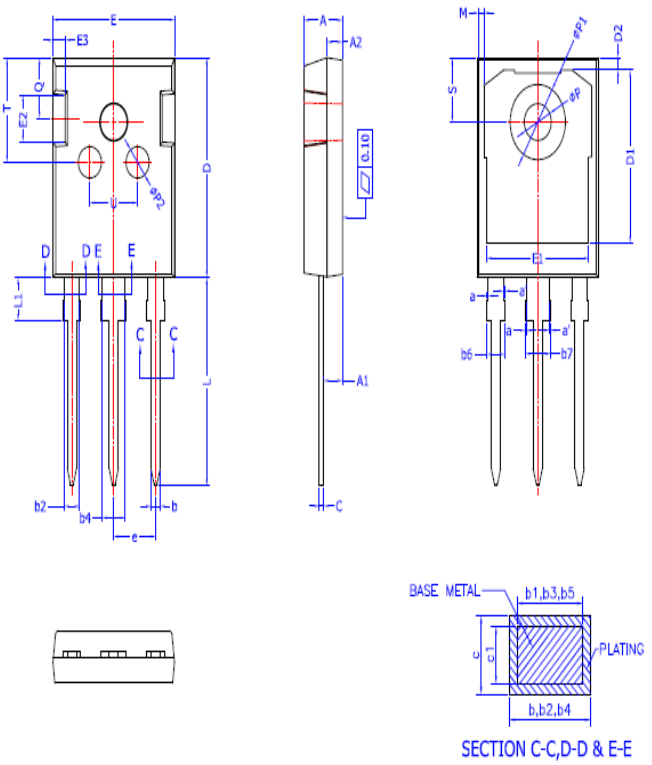
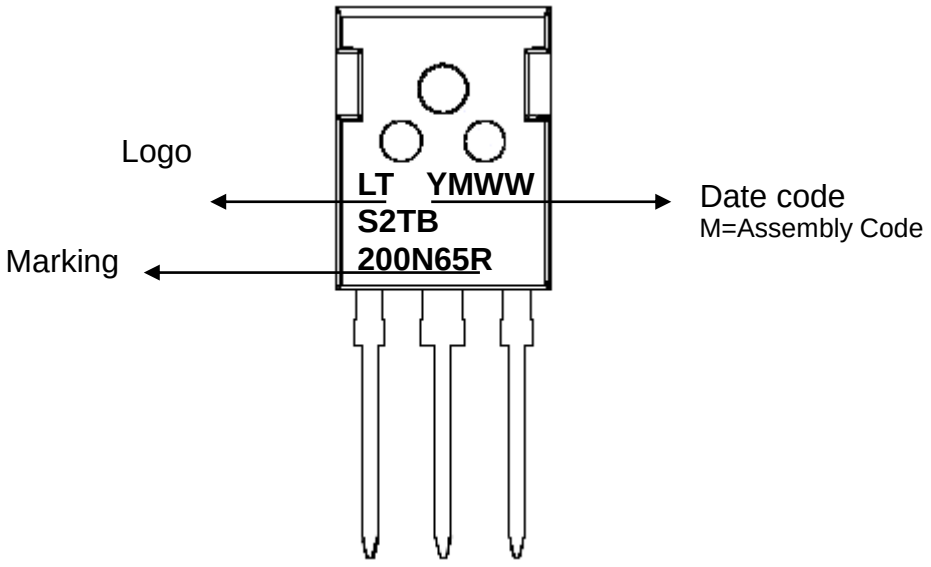
Package Outline Dimension

TO-247(Q type)



TO-247 (Q type)							
DIM	MIN	MON	MAX	DIM	MIN	MON	MAX
A	4.90	5.00	5.10	E1	13.10	13.30	13.50
A1	2.31	2.41	2.51	E2	4.40	4.50	4.60
A2	1.90	2.00	2.10	E3	2.40	2.50	2.60
a	0	--	0.15	e	5.436 BSC		
a'	0	--	0.15	L	19.80	19.92	20.10
b	1.16	--	1.26	L1	--	--	4.30
b1	1.15	1.20	1.22	M	0.35	--	0.95
b2	1.96	--	2.06	P1	7.00	--	7.40
b3	1.95	2.00	2.02	P2	2.40	2.50	2.60
b4	2.96	--	3.06	Q	5.60	--	6.00
b5	2.96	3.00	3.02	S	6.05	6.15	6.25
b6	--	--	2.25	T	9.80	--	10.20
b7	--	--	3.25	U	6.00	--	6.40
c	0.59	--	0.66				
c1	0.58	0.60	0.62				
D1	16.25	16.55	16.85				
D2	1.05	1.17	1.35				
E	15.70	15.80	15.90				
All Dimensions in millimeter							

Marking information



N-Channel 650V Enhancement Mode Power MOSFET

Packaging Information

PACKAGE	Units / Tube	Tubes / Inner Box	Box size (mm)	Units / Inner Box	Inner Box / Carton Box	Carton size (mm)	Units / Carton Box
TO-247 (Q type)	30	20	565X170X53	600	5	580X285X187	3K

N-Channel 650V Enhancement Mode Power MOSFET

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