Power Supply Tracking Controller

FEATURES

- **Flexible Power Supply Tracking**
- **Tracks Both Up and Down**
- **Power Supply Sequencing**
- **Supply Stability is Not Affected**
- Controls Two Supplies Without Series FETs
- Controls a Third Supply With a Series FET
- Adjustable Ramp Rates
- Electronic Circuit Breaker
- Available in 10-Lead MS and 12-Lead (4mm × 3mm × 0.8mm) DFN Packages

APPLICATIONS

- V_{CORE} and $V_{I/O}$ Supply Tracking
- Microprocessor, DSP and FPGA Supplies
- Servers
- Communication Systems

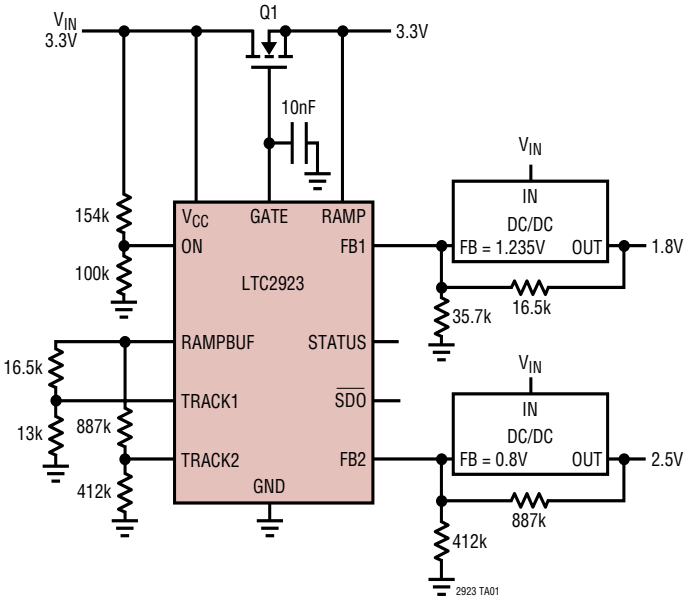
DESCRIPTION

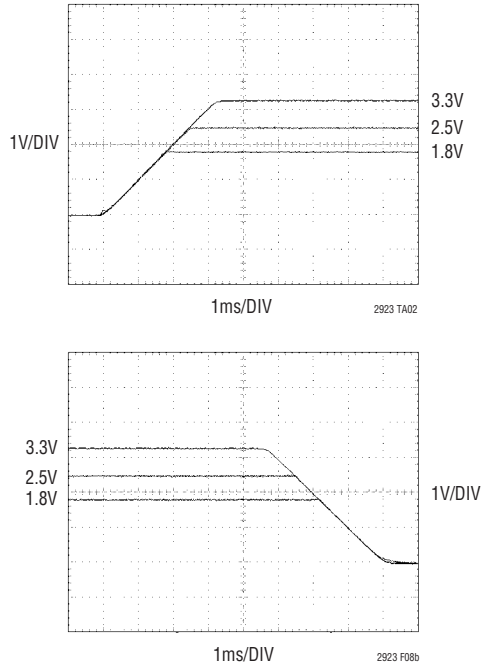
The LTC®2923 provides a simple solution to power supply tracking and sequencing requirements. By selecting a few resistors, the supplies can be configured to ramp-up and ramp-down together or with voltage offsets, time delays or differing ramp rates.

By introducing currents into the feedback nodes of two independent supplies, the LTC2923 causes their outputs to track without inserting any pass element losses. Because the currents are controlled in an open-loop manner, the LTC2923 does not affect the transient response or stability of the supplies. Furthermore, it presents a high impedance when power-up is complete, effectively removing it from the DC/DC circuit.

For systems that require a third supply, or when a supply does not allow direct access to its feedback resistors, one supply can be controlled with a series FET. When the FET is used, an electronic circuit breaker provides protection from short-circuit conditions.

TYPICAL APPLICATION

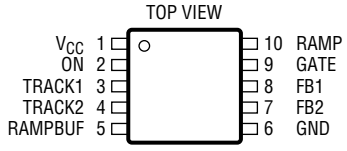




ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V_{CC}) ..... –0.3V to 10V
Input Voltages
  ON ..... –0.3V to 10V
  TRACK1, TRACK2 ..... –0.3V to V_{CC} + 0.3V
  RAMP ..... –0.3V to V_{CC} + 1V
Output Voltages
  FB1, FB2, $\overline{SDO}$, STATUS ..... –0.3V to 10V
  RAMPBUF ..... –0.3V to V_{CC} + 0.3V
  GATE (Note 2) ..... –0.3V to 11.5V
Average Current
  TRACK1, TRACK2 ..... 5mA
  FB1, FB2 ..... 5mA
  RAMPBUF 5mA
Operating Temperature Range
  LTC2923C ..... 0°C to 70°C
  LTC2923I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

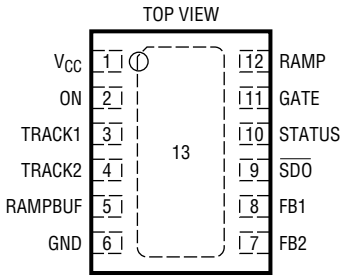
PACKAGE/ORDER INFORMATION



MS PACKAGE
10-LEAD PLASTIC MSOP

T_{JMAX} = 125°C, θ_{JA} = 120°C/W

ORDER PART NUMBER
LTC2923CMS LTC2923IMS
MS PART MARKING
LTAED LTAEE



DE12 PACKAGE
12-LEAD (4mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W

EXPOSED PAD (PIN 13) INTERNALLY CONNECTED TO GND
(PCB CONNECTION OPTIONAL)

ORDER PART NUMBER
LTC2923CDE LTC2923IDE
DE PART MARKING
2923

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. 2.9V < V_{CC} < 5.5V unless otherwise noted (Note 3).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Input Supply Range		●	2.9		5.5	V
I_{CC}	Input Supply Current	I_{FBx} = 0, I_{TRACKx} = 0 I_{FBx} = –1mA, I_{TRACKx} = –1mA, $I_{RAMPBUF}$ = –2mA	● ●	 5	1.3 7	3 10	mA mA
$V_{CC(UVL)}$	Input Supply Undervoltage Lockout	V_{CC} Rising	●	2.2	2.5	2.7	V
$\Delta V_{CC(UVLHYST)}$	Input Supply Undervoltage Lockout Hysteresis				25		mV
ΔV_{GATE}	External N-Channel Gate Drive (V_{GATE} – V_{CC})	I_{GATE} = –1µA	●	5	5.5	6	V
I_{GATE}	GATE Pin Current	Gate On, V_{GATE} = 0V, No Faults Gate Off, V_{GATE} = 5V, No Faults Gate Off, V_{GATE} = 5V, Short-Circuit Fault	● ● ●	–7 7 5	–10 10 20	–13 13 50	µA µA mA
$V_{ON(TH)}$	ON Pin Threshold Voltage	V_{ON} Rising	●	1.212	1.230	1.248	V
$\Delta V_{ON(HYST)}$	ON Pin Hysteresis		●	30	75	150	mV
$V_{ON(FC)}$	ON Pin Fault Clear Threshold Voltage		●	0.3	0.4	0.5	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. 2.9V < V_{CC} < 5.5V unless otherwise noted (Note 3).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{ON}	ON Pin Input Current	V_{ON} = 1.2V, V_{CC} = 5.5V	●		0	±100	nA
$\Delta V_{DS(TH)}$	FET Drain-Source Overcurrent Voltage Threshold ($V_{CC} - V_{RAMP}$)		●	160	200	240	mV
I_{RAMP}	RAMP Pin Input Current	0V < RAMP < V_{CC}, V_{CC} = 5.5V	●		0	±1	µA
$V_{RAMPBUF(OL)}$	RAMPBUF Low Voltage	$I_{RAMPBUF}$ = 2mA	●		90	150	mV
$V_{RAMPBUF(OH)}$	RAMPBUF High Voltage ($V_{CC} - V_{RAMPBUF}$)	$I_{RAMPBUF}$ = –2mA	●		100	200	mV
V_{OS}	Ramp Buffer Offset ($V_{RAMPBUF} - V_{RAMP}$)	$V_{RAMPBUF}$ = V_{CC}/2, $I_{RAMPBUF}$ = 0A		–30	0	30	mV
$I_{ERROR(\%)}$	I_{FBx} to I_{TRACKx} Current Mismatch $I_{ERROR(\%)} = (I_{FBx} - I_{TRACKx})/I_{TRACKx}$	I_{TRACKx} = –10µA I_{TRACKx} = –1mA	● ●		0 0	±5 ±5	% %
V_{TRACKx}	TRACK Pin Voltage	I_{TRACKx} = –10µA I_{TRACKx} = –1mA	● ●	0.776 0.776	0.8 0.8	0.824 0.824	V V
$I_{FB(LEAK)}$	I_{FB} Leakage Current	V_{FB} = 1.5V, V_{CC} = 5.5V	●		±1	±100	nA
$V_{FB(CLAMP)}$	V_{FB} Clamp Voltage	1µA < I_{FB} < 1mA	●	1.5	1.7	2	V
$V_{\overline{SDO}(OL)}$	$\overline{SDO}$ Output Low Voltage	$I_{\overline{SDO}}$ = 3mA	●		0.2	0.4	V
$V_{STATUS(OL)}$	STATUS Output Low Voltage	I_{STATUS} = 3mA	●		0.2	0.4	V
t_{PSC}	Short-Circuit Propagation Delay V_{DS} High to GATE Low	V_{DS} = V_{CC}, V_{CC} = 2.9V			10	20	µs

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

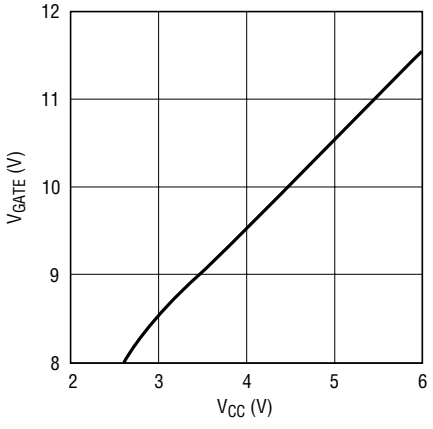
Note 2: The GATE pin is internally limited to a minimum of 11.5V. Driving this pin to voltages beyond the clamp may damage the part.

Note 3: All currents into the device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

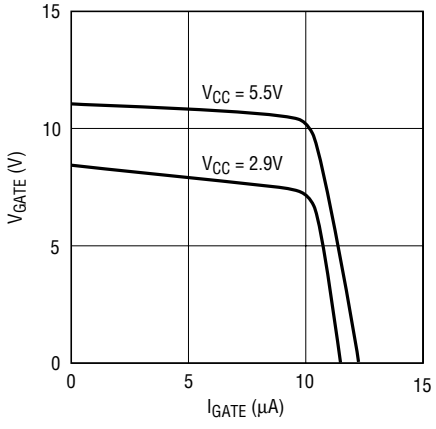
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at T_A = 25°C unless otherwise noted.

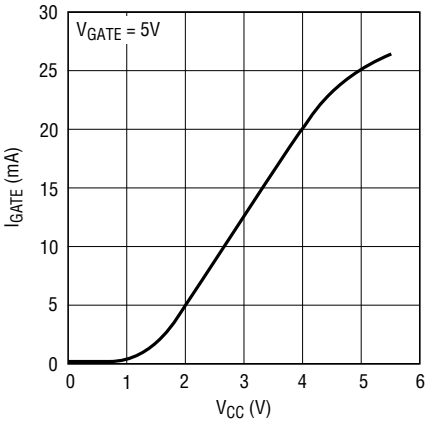
V_{GATE} vs V_{CC}



V_{GATE} vs I_{GATE}



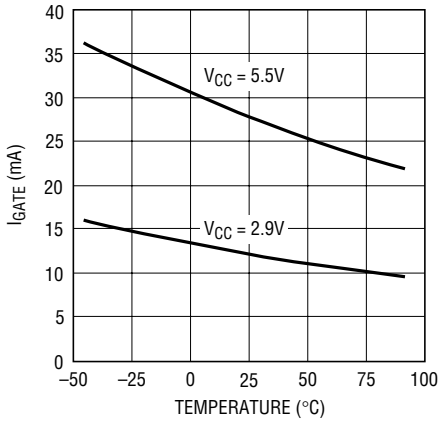
I_{GATE} vs V_{CC} Fast Pull-Down



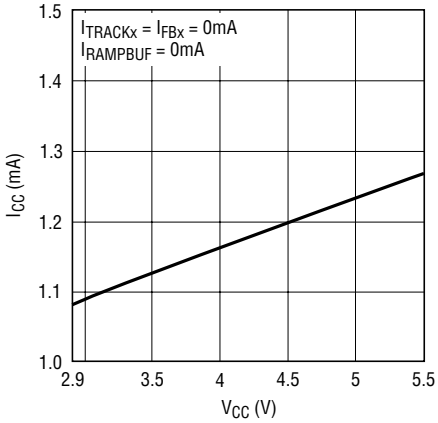
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at T_A = 25°C unless otherwise noted.

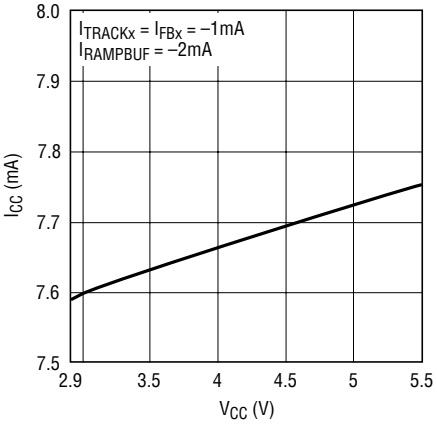
I_{GATE} Fast Pull-Down vs Temperature



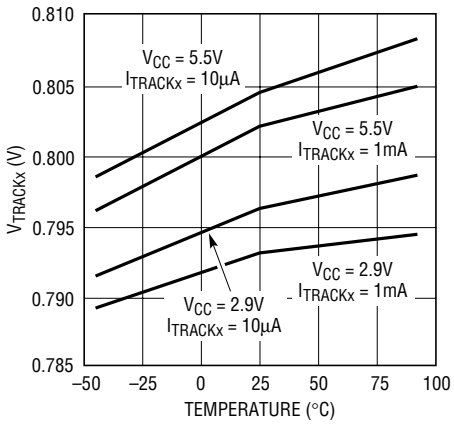
I_{CC} vs V_{CC}



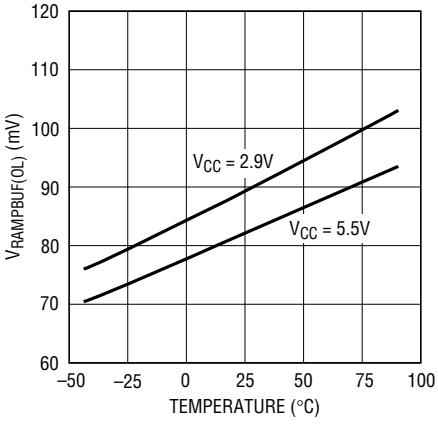
I_{CC} vs V_{CC}



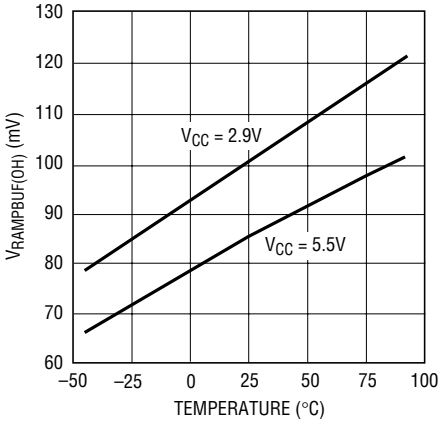
V_{TRACKx} vs Temperature



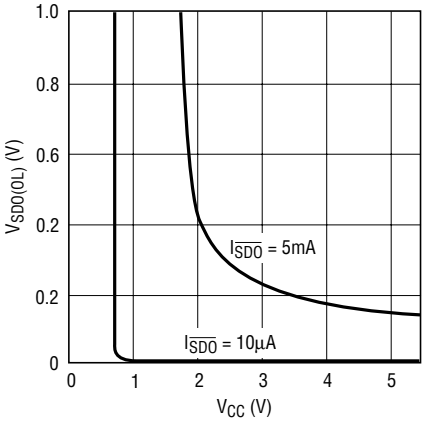
$V_{RAMPBUF(OL)}$ vs Temperature



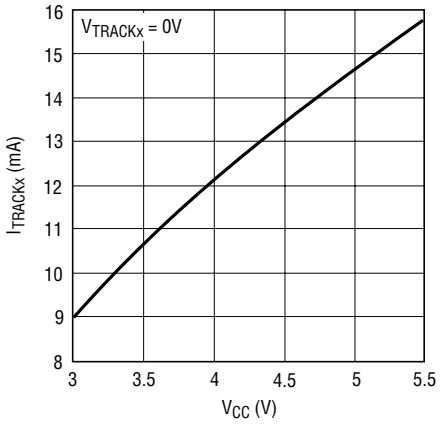
$V_{RAMPBUF(OH)}$ vs Temperature



$V_{\overline{SDO}(OL)}$ vs V_{CC}



I_{TRACKx} vs V_{CC}



PIN FUNCTIONS MS/DE Packages

V_{CC} (Pin 1): Positive Supply Input Pin. The operating supply input range is 2.9V to 5.5V. An undervoltage lockout circuit resets the part when the supply is below 2.5V. V_{CC} should be bypassed to GND with a 0.1µF capacitor.

ON (Pin 2): On Control Input. The ON pin has a threshold of 1.23V with 75mV of hysteresis. An active high will cause 10µA to flow from the GATE pin, ramping up the supplies. An active low pulls 10µA from the GATE pin, ramping the supplies down. Pulling the ON pin below 0.4V resets the electronic circuit breaker in the LTC2923. If a resistive divider connected to V_{CC} drives the ON pin, the supplies will automatically start up when V_{CC} is fully powered.

TRACK1, TRACK2 (Pins 3, 4): Tracking Control Input Pin. A resistive divider between RAMPBUF, TRACKx and GND determines the tracking profile of OUTx (see Applications Information). TRACKx pulls up to 0.8V and the current supplied at TRACKx is mirrored at FBx. The TRACKx pin is capable of supplying at least 1mA when V_{CC} = 2.9V. It may be capable of supplying up to 10mA when the supply is at 5.5V, so care should be taken not to short this pin for extended periods. Limit the capacitance at the TRACKx pin to less than 25pF. Float the TRACK pins if unused.

RAMPBUF (Pin 5): Ramp Buffer Output. Provides a low impedance buffered version of the signal on the RAMP pin. This buffered output drives the resistive dividers that connect to the TRACKx pins. Limit the capacitance at the RAMPBUF pin to less than 100pF.

GND (Pins 6, 13): Circuit Ground.

FB1, FB2 (Pins 8, 7): Feedback Control Output. FBx pulls up on the feedback node of slave supplies. Tracking is achieved by mirroring the current from TRACKx into FBx. If the appropriate resistive divider connects RAMPBUF and TRACKx, the FBx current will force OUTx to track RAMP. To prevent damage to the slave supply, the FBx pin will not force the slave's feedback node above 1.7V. In addition, it will not actively sink current from this node even when the LTC2923 is unpowered. Float the FB pins if unused.

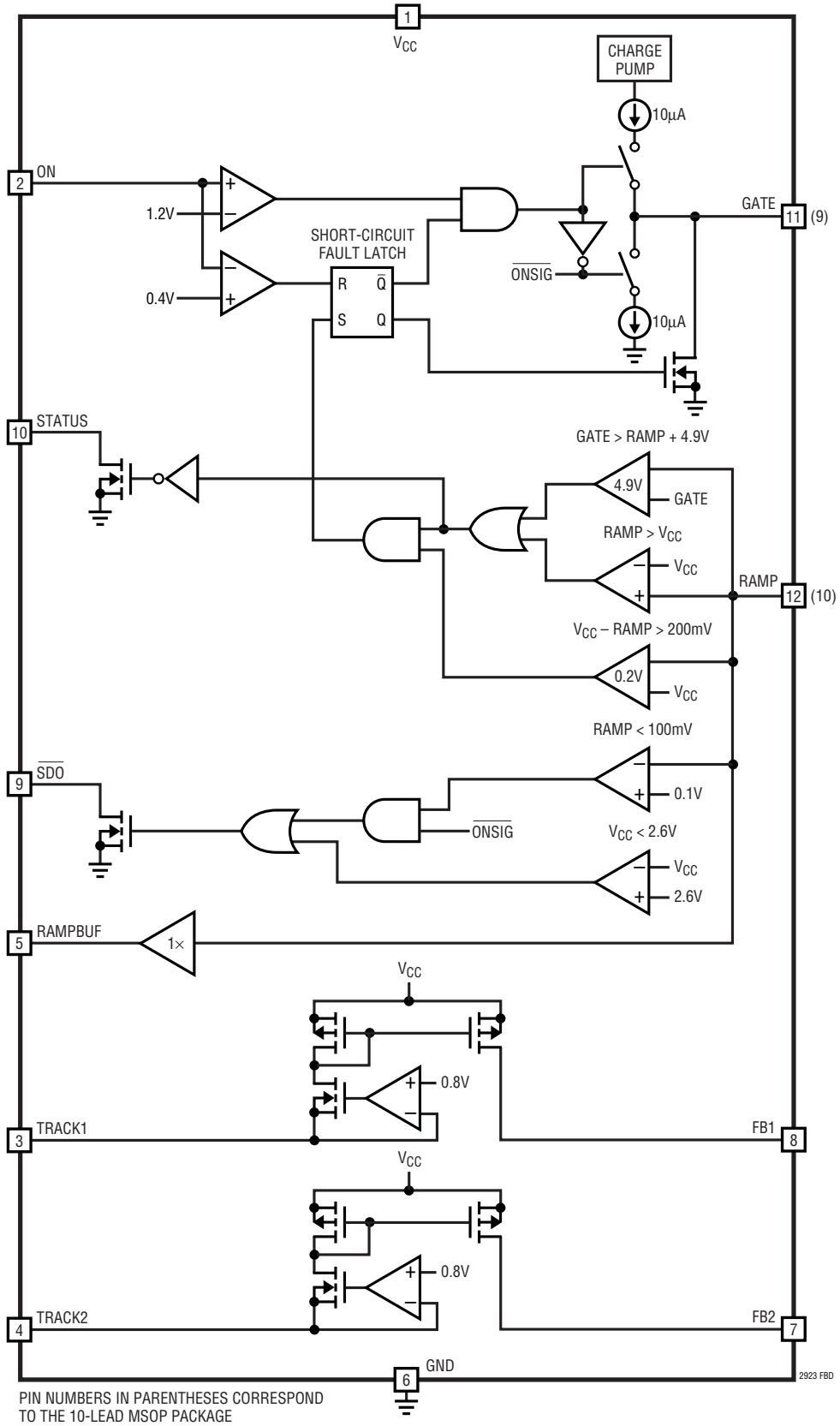
GATE (Pin 9/Pin 11): Gate Drive for External N-Channel FET. When the ON pin is high, an internal 10µA current source charges the gate of the external N-channel MOSFET. A capacitor connected from GATE to GND sets the ramp rate. An internal charge pump guarantees that GATE will pull up to 4.5V above RAMP ensuring that logic level N-channel FETs are fully enhanced. When the ON pin is pulled low, the GATE pin is pulled to GND with a 10µA current source. Under a short-circuit condition, the electronic circuit breaker in the LTC2923 pulls the GATE low immediately with 20mA. Tie GATE to GND if unused. It is a good practice to add a 10Ω resistor between this capacitor and the FET's gate to prevent high frequency FET oscillations.

RAMP (Pin 10/Pin 12): Ramp Buffer Input. When the RAMP pin is connected to the source of the external N-channel FET, the slave supplies track the FET's source as it ramps up and down. If the GATE is fully enhanced (GATE > RAMP + 4.9V) and (V_{CC} – RAMP > 200mV) indicates a shorted output, then the electronic circuit breaker trips and GATE quickly pulls low with 20mA. The GATE will not ramp up again until ON is pulled below 0.4V and then above 1.23V. Alternatively, when no external FET is used, the RAMP pin can be tied directly to the GATE pin. In this configuration, the supplies track the capacitor on the GATE pin as it is charged and discharged by the 10µA current source controlled by the ON pin. RAMP must not be driven above V_{CC} (except by the GATE pin).

$\overline{SDO}$ (Pin 9, DE Package Only): Slave Supply Shutdown Output. $\overline{SDO}$ is an open-drain output that holds the shutdown (RUN/SS) pins of the slave supplies low until the ON pin is pulled above 1.23V. If the slave supply is capable of operating with an input supply that is lower than the LTC2923's minimum operating voltage of 2.9V, the $\overline{SDO}$ pin can be used to hold off the slave supplies. $\overline{SDO}$ will be pulled low again when RAMP < 100mV and ON < 1.23V.

STATUS (Pin 10, DE Package Only): Power Good Status Indicator. The STATUS pin is an open-drain output that pulls low until GATE has been fully charged at which time all supplies will have reached their final operating voltage.

FUNCTIONAL BLOCK DIAGRAM



PIN NUMBERS IN PARENTHESES CORRESPOND TO THE 10-LEAD MSOP PACKAGE

APPLICATIONS INFORMATION

Power Supply Tracking and Sequencing

The LTC2923 handles a variety of power-up profiles to satisfy the requirements of digital logic circuits including FPGAs, PLDs, DSPs and microprocessors. These requirements fall into one of the four general categories illustrated in Figures 1 to 4.

Some applications require that the potential difference between two power supplies must never exceed a specified voltage. This requirement applies during power-up and power-down as well as during steady-state operation, often to prevent destructive latch-up in a dual supply ASIC. Typically, this is achieved by ramping the supplies up and down together (Figure 1). In other applications it is desirable to have the supplies ramp up and down with fixed voltage offsets between them (Figure 2) or to have them ramp up and down ratiometrically (Figure 3).

Certain applications require one supply to come up after another. For example, a system clock may need to start before a block of logic. In this case, the supplies are sequenced as in Figure 4 where the 2.5V supply ramps up after the 1.8V supply is completely powered.

Operation

The LTC2923 provides a simple solution to all of the power supply tracking and sequencing profiles shown in Figures 1 to 4. A single LTC2923 controls up to three supplies with two "slave" supplies that track a "master" signal. With just two resistors, a slave supply is configured to ramp up as a function of the master signal. This master signal can be a third supply that is ramped up through an external FET, whose ramp rate is set with a single capacitor, or it can be a signal generated by tying the GATE and RAMP pins to an external capacitor.

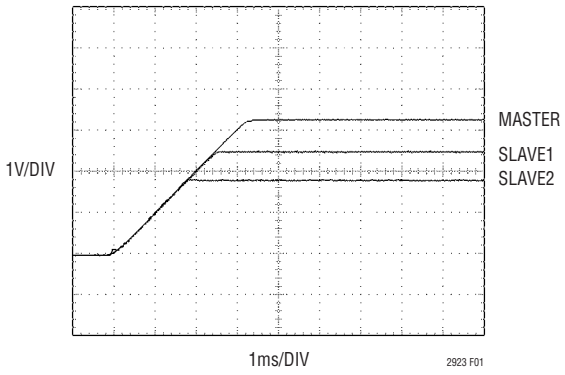


Figure 1. Coincident Tracking

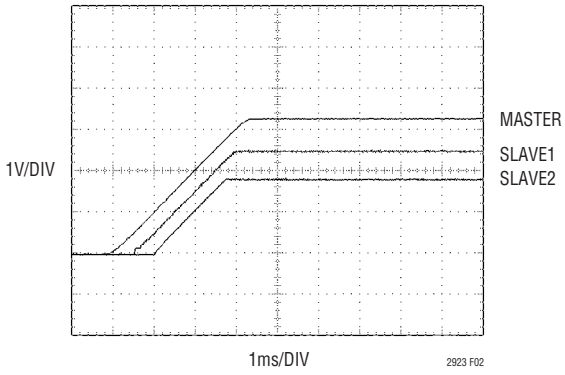


Figure 2. Offset Tracking

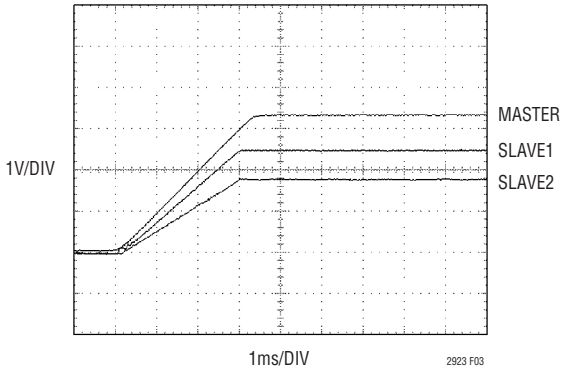


Figure 3. Ratiometric Tracking

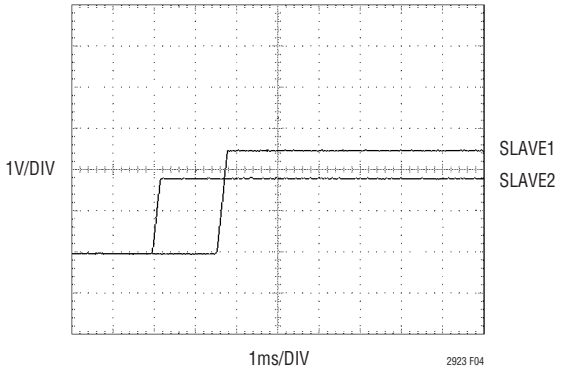


Figure 4. Supply Sequencing

APPLICATIONS INFORMATION

Tracking Cell

The LTC2923's operation is based on the tracking cell shown in Figure 5, which uses a proprietary wide-range current mirror. The tracking cell shown in Figure 5 servos the TRACK pin at 0.8V. The current supplied by the TRACK pin is mirrored at the FB pin to establish a voltage at the output of the slave supply. The slave output voltage varies with the master signal, enabling the slave supply to be controlled as a function of the master signal with terms set by R_{TA} and R_{TB}. By selecting appropriate values of R_{TA} and R_{TB}, it is possible to generate any of the profiles in Figures 1 to 4.

Controlling the Ramp-Up and Ramp-Down Behavior

The operation of the LTC2923 is most easily understood by referring to the simplified functional diagram in Figure 6. When the ON pin is low, the GATE pin is pulled to ground causing the master signal to remain low. Since the currents through R_{TB1} and R_{TB2} are at their maximum when the master signal is low, the currents from FB1 and FB2 are also at their maximum. These currents drive the slaves' outputs to their minimum voltages.

When the ON pin rises above 1.23V, the master signal rises and the slave supplies track the master signal. The ramp rate is set by an external capacitor driven by a 10µA current source from an internal charge pump. If no external FET is used, the ramp rate is set by tying the RAMP and GATE pins together at one terminal of the external capacitor (see the Ratiometric Tracking Example).

In a properly designed system, when the master signal has reached its maximum voltage the current from the TRACKx pin is zero. In this case, there is no current from the FBx pin and the LTC2923 has no effect on the output voltage accuracy, transient response or stability of the slave supply.

When the ON pin falls below $V_{ON(TH)} - \Delta V_{ON(HYST)}$, typically 1.225V, the GATE pin pulls down with 10µA and the master signal and the slave supplies will fall at the same rate as they rose previously.

The ON pin can be controlled by a digital I/O pin or it can be used to monitor an input supply. By connecting a resistive divider from an input supply to the ON pin, the supplies will ramp up only after the monitored supply has reached a preset voltage.

Optional External FET

The Coincident Tracking Example (Figures 8 and 9) illustrates how an optional external N-channel FET can ramp up a single supply that becomes the master signal. When used, the FET's gate is charged by the GATE pin and its source is tied to the RAMP pin. Under normal operation, the GATE pin sources or sinks 10µA to ramp the FET's gate up or down at a rate set by the external capacitor connected to the GATE pin. It is a good practice to add 10Ω between the FET's gate and the external capacitor to prevent high frequency oscillations.

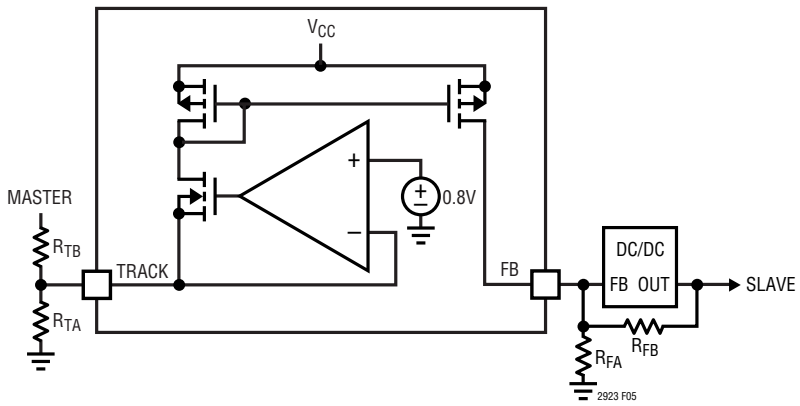


Figure 5. Simplified Tracking Cell

APPLICATIONS INFORMATION

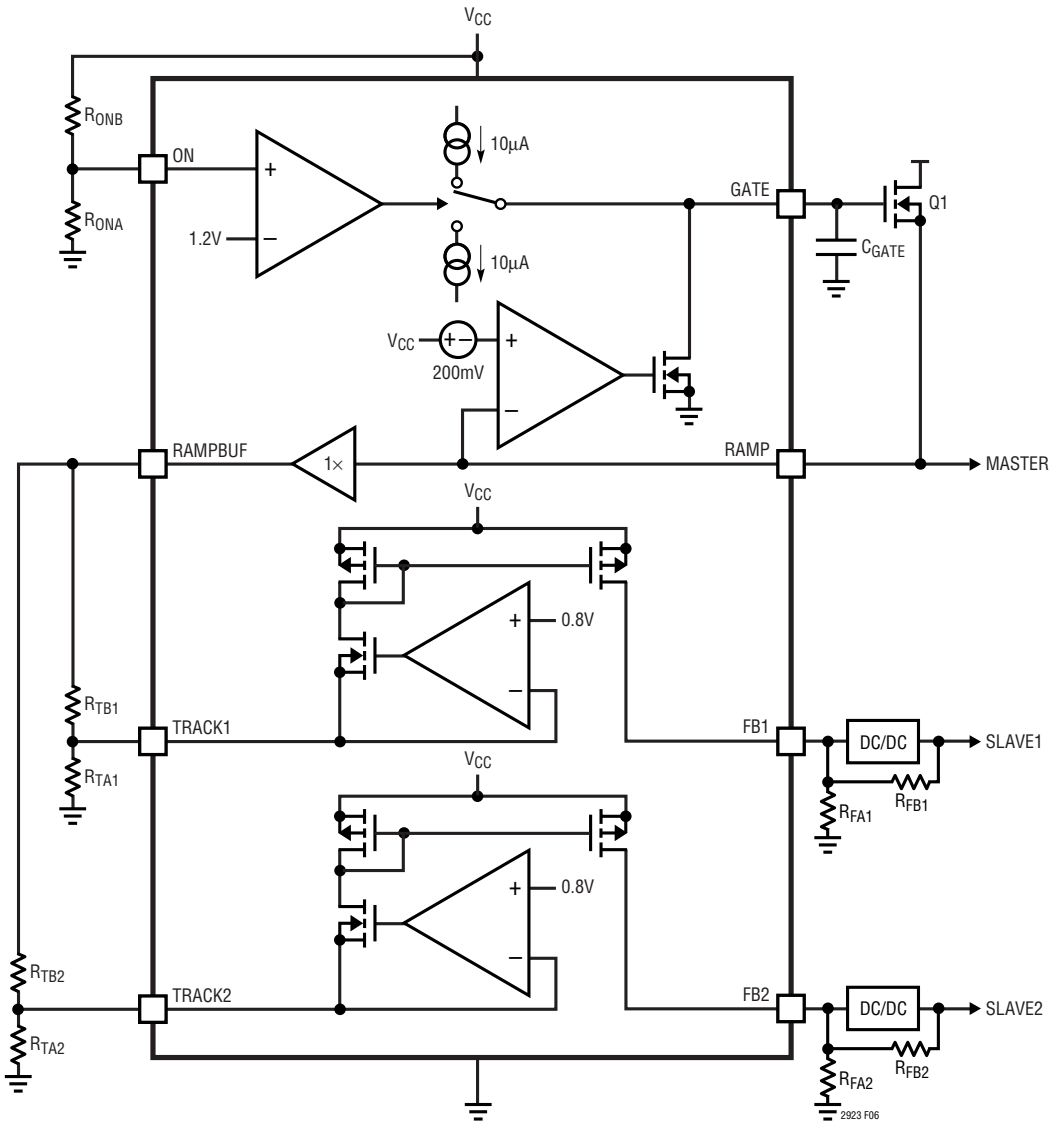


Figure 6. Simplified Functional Diagram

The LTC2923 features an electronic circuit breaker function that protects the optional series FET against short circuits. When the FET is fully enhanced (GATE > RAMP + 4.9V), the electronic circuit breaker is enabled. Then, if the voltage across the FET (V_{DS}) exceeds 200mV as measured from V_{CC} to the RAMP pin for more than about 10µs the gate of the FET is pulled down with 20mA, turning it off. Because the slaved supplies track the RAMP pin, they are pulled low by the tracking circuit when a short-circuit fault occurs. Following a short-circuit fault, the FET is latched off until the fault is cleared by pulling the ON pin below 0.4V.

The Ramp Buffer

The RAMPBUF pin provides a buffered version of the RAMP pin voltage that drives the resistive dividers on the TRACKx pins. When there is no external FET, it provides up to 2mA to drive the resistors even though the GATE pin only supplies 10µA. The RAMPBUF pin also proves useful in systems with an external FET. Since the track cell in the simplified functional diagram above drives 0.8V on the TRACKx pins, if R_{TBx} is connected directly to the FET's source, the TRACKx pin could potentially pull up the FET's source towards 0.8V when the FET is off. RAMPBUF blocks this path.

APPLICATIONS INFORMATION

Shutdown Output

In some applications it might be necessary to control the shutdown or RUN/SS pins of the slave supplies using the 12-lead LTC2923CDE or LTC2923IDE. The LTC2923 may not be able to supply the rated 1mA of current from the FB1 and FB2 pins when V_{CC} is below 2.9V. If the slave power supplies are capable of operating at low input voltages, use the open-drain $\overline{SDO}$ output to drive the $\overline{SHDN}$ or RUN/SS pins of the slave supplies (see Figure 7). This will hold the slave supplies' outputs low until the ON pin is above 1.23V, V_{CC} is above the 2.6V undervoltage lockout condition and there are no short-circuit faults latched. It pulls low again when the ON pin is pulled below 1.23V and the RAMP pin is below about 100mV. When two supplies must have their RUN/SS or $\overline{SHDN}$ pins controlled independently, tie a Schottky diode between each pin and the $\overline{SDO}$ output (see Figure 8).

Status Output

The STATUS pin provides an indication that the supplies are finished ramping up. This pin is an open-drain output that pulls low until the GATE has been fully charged. Since the GATE pin drives the gate of the external FET, or the RAMP pin directly when no FET is used, the supplies are completely ramped up when the GATE pin is fully charged. It will go low again when the GATE pin is pulled low, either because of a short-circuit fault or because the ON pin has been pulled low.

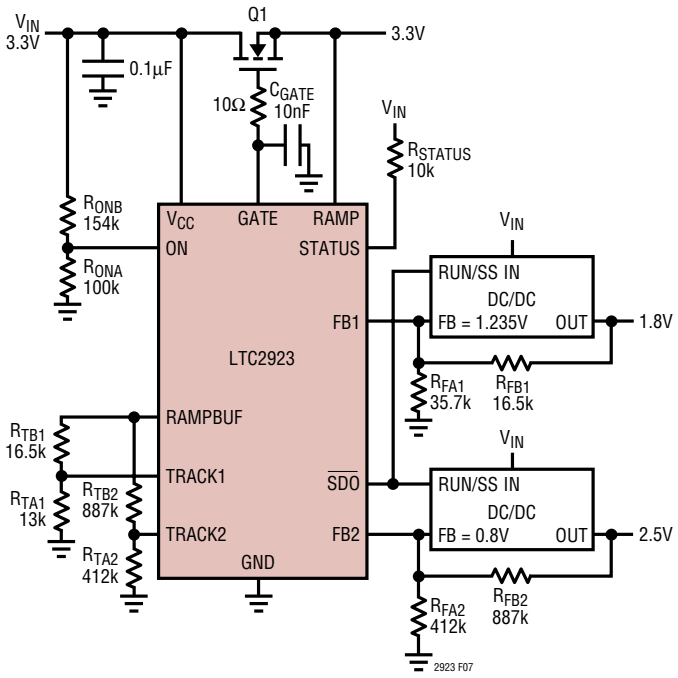


Figure 7

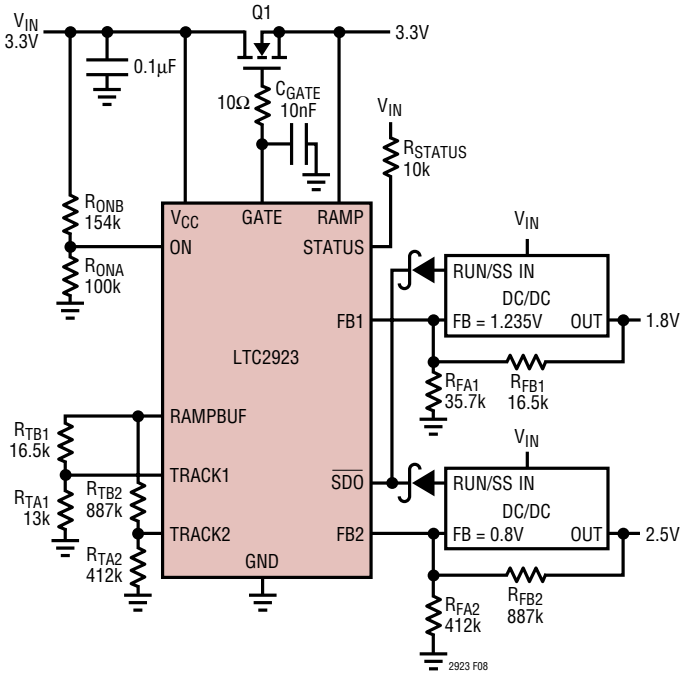


Figure 8

APPLICATIONS INFORMATION

3-Step Design Procedure

The following 3-step procedure allows one to complete a design for any of the tracking or sequencing profiles shown in Figures 1 to 4. A basic three supply application circuit is shown in Figure 9.

1. *Set the ramp rate of the master signal.*

   Solve for the value of C_{GATE}, the capacitor on the GATE pin, based on the desired ramp rate (V/s) of the master supply, S_M.

$$C_{GATE} = \frac{I_{GATE}}{S_M} \text{ where } I_{GATE} \approx 10\mu A \quad (1)$$

   If the external FET has a gate capacitance comparable to C_{GATE}, then the external capacitor's value should be reduced to compensate for the FET's gate capacitance.

   If no external FET is used, tie the GATE and RAMP pins together.

2. *Solve for the pair of resistors that provide the desired ramp rate of the slave supply, assuming no delay.*

   Choose a ramp rate for the slave supply, S_S. If the slave supply ramps up coincident with the master supply or with a fixed voltage offset, then the ramp rate equals the master supply's ramp rate. Be sure to use a fast enough ramp rate for the slave supply so that it will finish ramping before the master supply has reached its final supply value. If not, the slave supply will be held below the intended regulation value by the master supply. Use the following formulas to determine the resistor values for the desired ramp rate, where R_{FB} and R_{FA} are the feedback resistors in the slave supply and V_{FB} is the feedback reference voltage of the slave supply:

$$R_{TB} = R_{FB} \bullet \frac{S_M}{S_S} \quad (2)$$

$$R_{TA}' = \frac{V_{TRACK}}{\frac{V_{FB}}{R_{FB}} + \frac{V_{FB}}{R_{FA}} - \frac{V_{TRACK}}{R_{TB}}} \quad (3)$$

   where $V_{TRACK} \approx 0.8V$.

   Note that large ratios of slave ramp rate to master ramp rate, S_S/S_M, may result in negative values for R_{TA}'. If sufficiently large delay is used in step 3, R_{TA} will be positive, otherwise S_S/S_M must be reduced.

3. *Choose R_{TA} to obtain the desired delay.*

   If no delay is required, such as in coincident and ratiometric tracking, then simply set $R_{TA} = R_{TA}'$. If a delay is desired, as in offset tracking and supply sequencing, calculate R_{TA}'' to determine the value of R_{TA} where t_D is the desired delay in seconds.

$$R_{TA}'' = \frac{V_{TRACK} \bullet R_{TB}}{t_D \bullet S_M} \quad (4)$$

$$R_{TA} = R_{TA}' || R_{TA}'' \quad (5)$$

   the parallel combination of R_{TA}' and R_{TA}''

As noted in step 2, small delays and large ratios of slave ramp rate to master ramp rate (usually only seen in sequencing) may result in solutions with negative values for R_{TA}. In such cases, either the delay must be increased or the ratio of slave ramp rate to master ramp rate must be reduced.

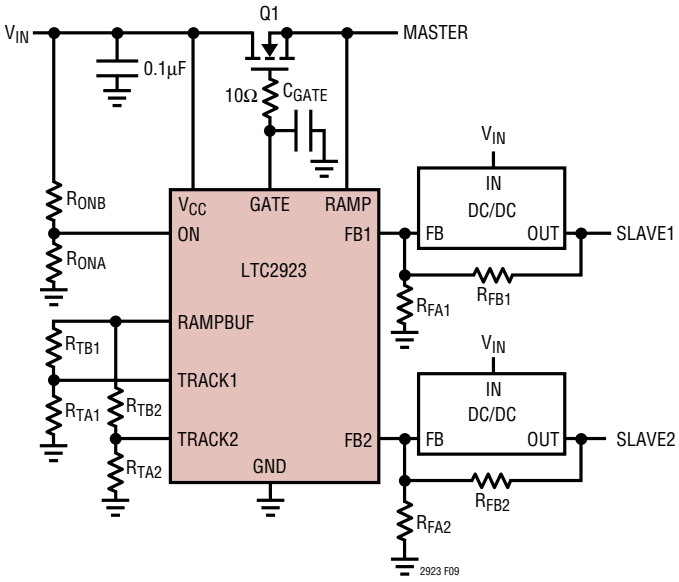


Figure 9. Three Supply Application

APPLICATIONS INFORMATION

Coincident Tracking Example

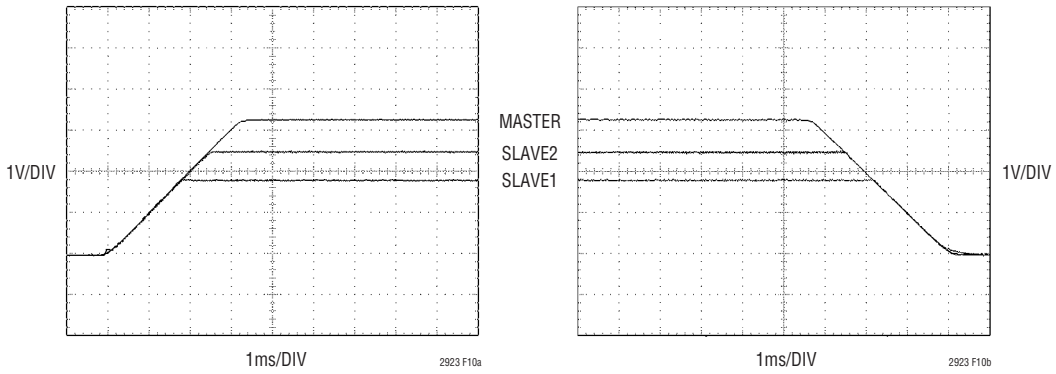


Figure 10. Coincident Tracking (From Figure 11)

A typical three supply application is shown in Figure 11. The master signal is a 3.3V module. The slave 1 supply is a 1.8V switching power supply and the slave 2 supply is a 2.5V switching power supply. Both slave supplies track coincidently with the 3.3V supply that is controlled with an external FET. The ramp rate of the supplies is 1000V/s. The 3-step design procedure detailed previously can be used to determine component values. Only the slave 1 supply is considered here as the procedure is the same for the slave 2 supply.

1. *Set the ramp rate of the master signal.*

   From Equation 1:

$$C_{GATE} = \frac{10\mu A}{1000V/s} = 10nF$$

2. *Solve for the pair of resistors that provide the desired slave supply behavior, assuming no delay.*

   From Equation 2:

$$R_{TB} = 16.5k\Omega \bullet \frac{1000V/s}{1000V/s} = 16.5k\Omega$$

   From Equation 3:

$$R_{TA}' = \frac{0.8V}{\frac{1.235V}{16.5k\Omega} + \frac{1.235V}{35.7k\Omega} - \frac{0.8V}{16.5k\Omega}} \approx 13k\Omega$$

3. *Choose R_{TA} to obtain the desired delay.*

   Since no delay is desired, $R_{TA} = R_{TA}'$

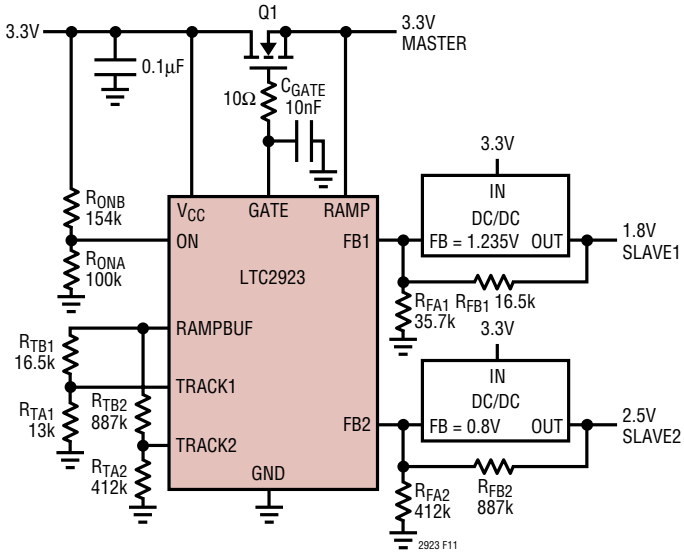


Figure 11. Coincident Tracking Example

In this example, all supplies remain low while the ON pin is held below 1.23V. When the ON pin rises above 1.23V, 10µA pulls up C_{GATE} and the gate of the FET at 1000V/s. As the gate of the FET rises, the source follows and pulls up the output to 3.3V at 1000V/s. This output serves as the master signal and is buffered from the RAMP pin to the RAMPBUF pin. As this output and the RAMPBUF pin rise, the current from the TRACK pins is reduced. Consequently, the voltage at the slave supply's outputs is reduced, and the slave supplies track the master supply. When the ON pin is again pulled below 1.23V, 10µA will pull down C_{GATE} and the gate of the FET at 1000V/s. If the loads on the outputs are sufficient, all outputs will track down coincidently at 1000V/s.

APPLICATIONS INFORMATION

Ratiometric Tracking Example

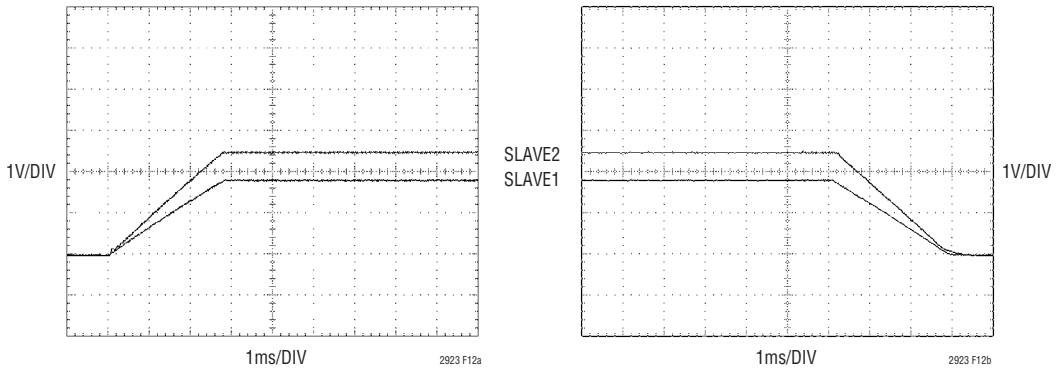


Figure 12. Ratiometric Tracking (From Figure 13)

This example converts the coincident tracking example to the ratiometric tracking profile shown in Figure 12, using two supplies without an external FET. The ramp rate of the master signal remains unchanged (Step 1) and there is no delay in ratiometric tracking (Step 3), so only the result of step 2 in the 3-step design procedure needs to be considered. In this example, the ramp rate of the 1.8V slave 1 supply ramps up at 600V/s and the 2.5V slave 2 supply ramps up at 850V/s. Always verify that the chosen ramp rate will allow the supplies to ramp-up completely before RAMPBUF reaches V_{CC}. If the 1.8V supply were to ramp-up at 500V/s it would only reach 1.65V because the RAMPBUF signal would reach its final value of V_{CC} = 3.3V before the slave supply reached 1.8V.

2. *Solve for the pair of resistors that provide the desired slave supply behavior, assuming no delay.*

   From Equation 2:

$$R_{TB} = 16.5k\Omega \bullet \frac{1000V/s}{600V/s} \approx 27.4k\Omega$$

From Equation 3:

$$R_{TA}' = \frac{0.8V}{\frac{1.235V}{16.5k\Omega} + \frac{1.235V}{35.7k\Omega} - \frac{0.8V}{27.5k\Omega}} = 10k\Omega$$

Step 3 is unnecessary because there is no delay, so $R_{TA} = R_{TA}'$.

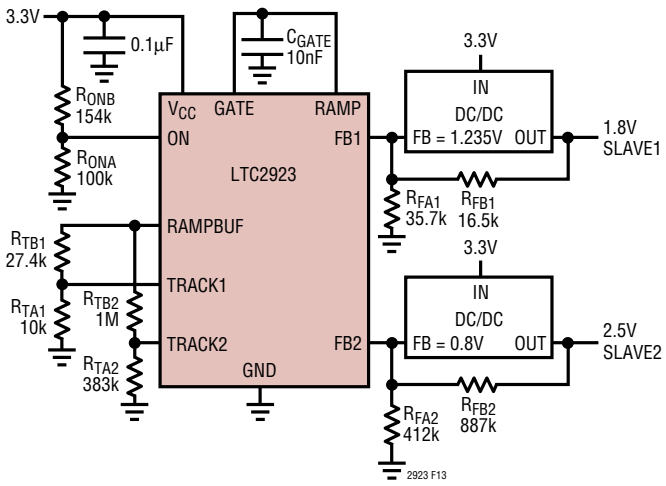


Figure 13. Ratiometric Tracking Example

APPLICATIONS INFORMATION

Offset Tracking Example

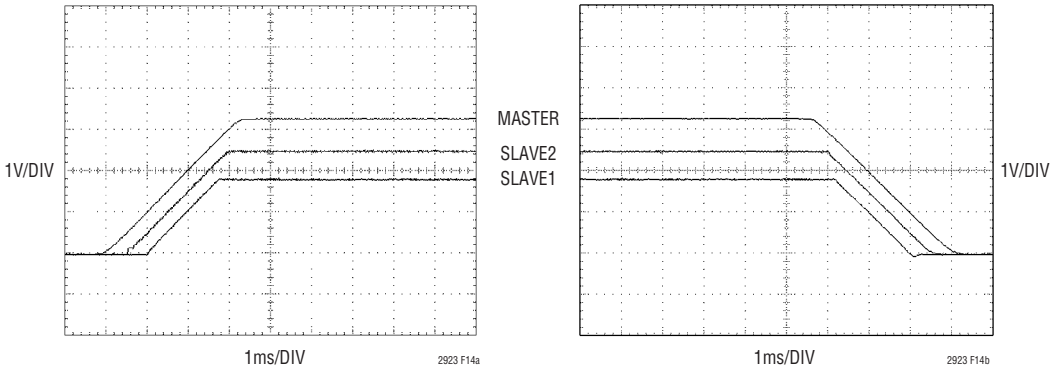


Figure 14. Offset Tracking (From Figure 15)

Converting the circuit in the coincident tracking example to the offset tracking shown in Figure 14 is relatively simple. Here the 1.8V slave 1 supply ramps up 1V below the master. The ramp rate remains the same (1000V/s), so there are no changes necessary to steps 1 and 2 of the 3-step design procedure. Only step 3 must be considered. Be sure to verify that the chosen voltage offsets will allow the slave supplies to ramp up completely. In this example, if the voltage offset were 2V, the slave supply would only ramp up to 3.3V – 2V = 1.3V.

3. *Choose R_{TA} to obtain the desired delay.*

First, convert the desired voltage offset, V_{OS}, to a delay, t_D, using the ramp rate:

$$t_D = \frac{V_{OS}}{S_S} = \frac{1V}{1000V/s} = 1ms \quad (6)$$

From Equation 4:

$$R_{TA}'' = \frac{0.8V \bullet 16.5k\Omega}{1ms \bullet 1000V/s} = 13.2k\Omega$$

From Equation 5:

$$R_{TA} = 13.1k\Omega || 13.2k\Omega \approx 6.65k\Omega$$

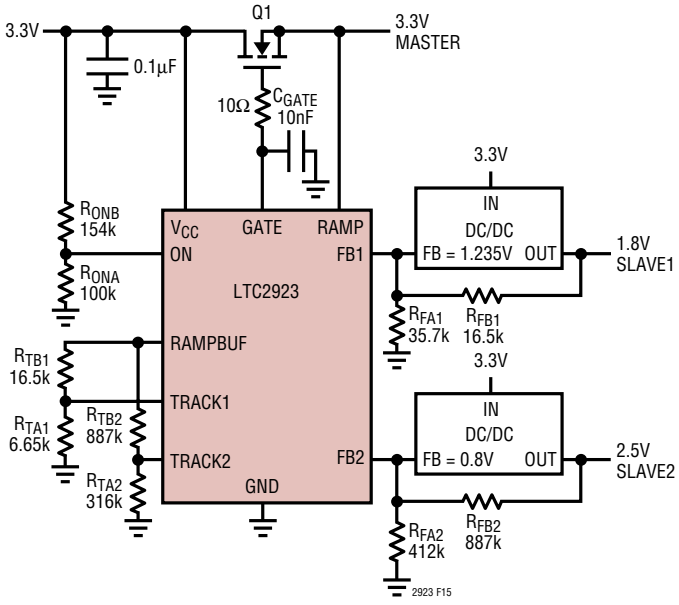


Figure 15. Offset Tracking Example

APPLICATIONS INFORMATION

Supply Sequencing Example

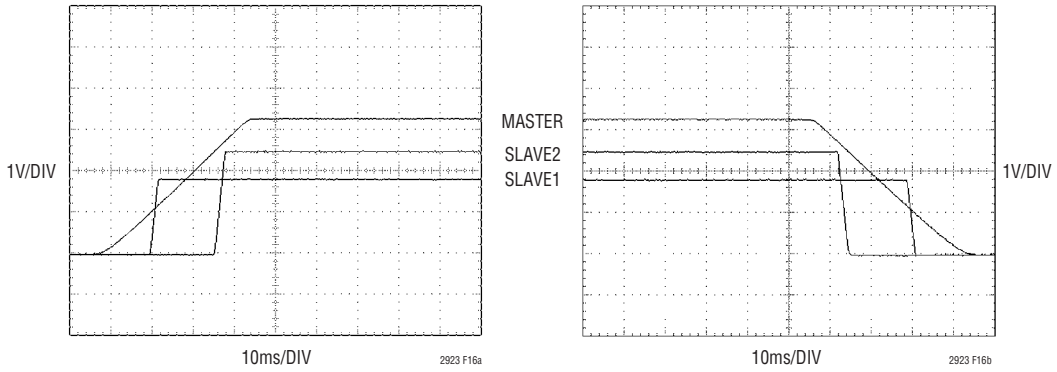


Figure 16. Supply Sequencing (From Figure 17)

In Figure 16, the slave 1 supply and the slave 2 supply are sequenced instead of tracking. The 3.3V supply ramps up at 100V/s with an external FET and serves as the master signal. The 1.8V slave 1 supply ramps up at 1000V/s beginning 10ms after the master signal starts to ramp up. The 2.5V slave 2 supply ramps up at 1000V/s beginning 25ms after the master signal begins to ramp up. Note that not every combination of ramp rates and delays is possible. Small delays and large ratios of slave ramp rate to master ramp rate may result in solutions that require negative resistors. In such cases, either the delay must be increased or the ratio of slave ramp rate to master ramp rate must be reduced. In this example, solving for the slave 1 supply yields:

1. *Set the ramp rate of the master signal.*

   From Equation 1:

$$C_{GATE} = \frac{10\mu A}{100V/s} = 100nF$$

2. *Solve for the pair of resistors that provide the desired slave supply behavior, assuming no delay.*

   From Equation 2:

$$R_{TB} = 16.5k\Omega \bullet \frac{100V/s}{1000V/s} = 1.65k\Omega$$

   From Equation 3:

$$R_{TA}' = \frac{0.8V}{\frac{1.235V}{16.5k\Omega} + \frac{1.235V}{35.7k\Omega} - \frac{0.8V}{1.65k\Omega}} = -2.13k\Omega$$

3. *Choose R_{TA} to obtain the desired delay.*

   From Equation 4:

$$R_{TA}'' = \frac{0.8V \bullet 1.65k\Omega}{10ms \bullet 100V/s} = 1.32k\Omega$$

   From Equation 5:

$$R_{TA} = -2.13k\Omega || 1.32k\Omega = 3.48k\Omega$$

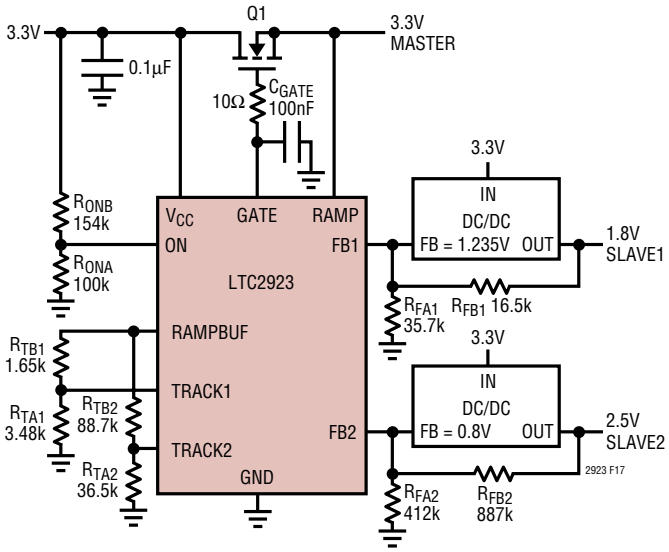


Figure 17. Supply Sequencing Example

APPLICATIONS INFORMATION

Final Sanity Checks

The collection of equations below is useful for identifying unrealizable solutions.

As stated in step 2, the slave supply must finish ramping before the master signal has reached its final voltage. This can be verified by the following equation:

$$V_{TRACK}\left(1+\frac{R_{TB}}{R_{TA}}\right) < V_{CC}, \text{ where } V_{TRACK} = 0.8V$$

It is possible to choose resistor values that require the LTC2923 to supply more current than the Electrical Characteristics table guarantees. To avoid this condition, check that I_{TRACKx} does not exceed 1mA and $I_{RAMPBUF}$ does not exceed ±2mA.

To confirm that $I_{TRACKx} < 1mA$, the TRACKx pin's maximum guaranteed current, verify that:

$$\frac{V_{TRACK}}{R_{TA} \| R_{TB}} < 1mA$$

Finally, check that the RAMPBUF pin will not be forced to sink more then 2mA when it is at 0V or be forced to source more than 2mA when it is at V_{CC}.

$$\frac{V_{TRACK}}{R_{TA1} \| R_{TB1}} + \frac{V_{TRACK}}{R_{TA2} \| R_{TB2}} < 2mA \text{ and}$$

$$\frac{V_{CC}}{R_{TA1} + R_{TB1}} + \frac{V_{CC}}{R_{TA2} + R_{TB2}} < 2mA$$

Load Requirements

When the supplies are ramped down quickly, either the load or the supply itself must be capable of sinking enough current to support the ramp rate. For example, if there is a large output capacitance on the supply and a weak resistive load, supplies that do not sink current will have their falling ramp rate limited by the RC time constant of the load and the output capacitance. Figure 18 shows the case when the 2.5V supply does not track the 1.8V and 3.3V supplies near ground.

Start-Up Delays

Often power supplies do not start-up immediately when their input supplies are applied. If the LTC2923 tries to ramp-up these power supplies as soon as the input supply is present, the start-up of the outputs may be delayed, defeating the tracking circuit (Figure 19). Often this delay is intentionally configured by a soft-start capacitor. This can be remedied either by reducing the soft-start capacitor on the slave supply or by including a capacitor in the ON pin's resistive divider to delay the ramp up. See Figure 20.

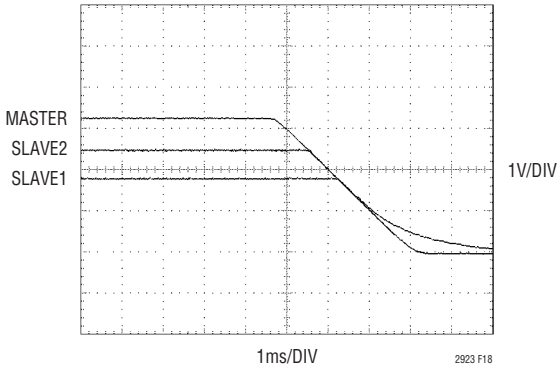


Figure 18. Weak Resistive Load

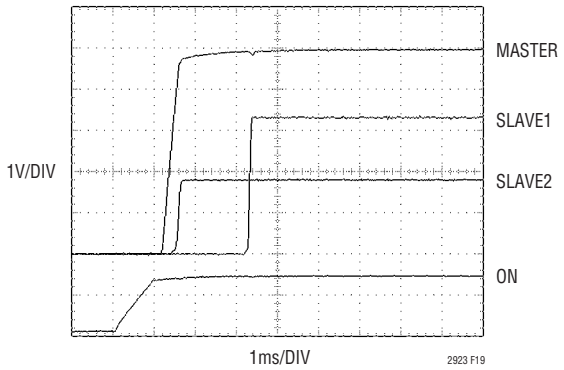


Figure 19. Power Supply Start-Ups Delayed

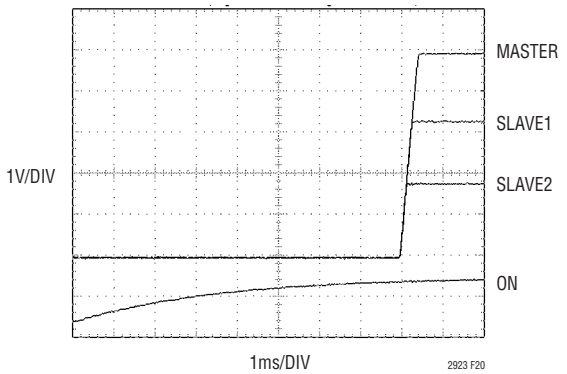


Figure 20. ON Pin Delayed

APPLICATIONS INFORMATION

Layout Considerations

Be sure to place a 0.1µF bypass capacitor as near as possible to the supply pin of the LTC2923. A 10Ω resistor located near the FET and connected between the FET's gate and the external C_{GATE} capacitor is recommended. This will almost assuredly eliminate the troublesome high frequency oscillations that can occur due to the FET interacting with PCB parasitics.

To minimize the noise on the slave supplies' outputs, keep the traces connecting the FBx pins of the LTC2923 and the feedback nodes of the slave supplies as short as possible. In addition, do not route those traces next to signals with fast transition times. In some circumstances it might be advantageous to add a resistor near the feedback node of the slave supply in series with the FBx pin of the LTC2923.

This resistor must not exceed:

$$R_{SERIES} = \frac{1.5V - V_{FB}}{I_{MAX}} = \left(\frac{1.5V}{V_{FB}} - 1\right)\left(R_{FA} || R_{FB}\right)$$

This resistor is most effective if there is already a capacitor at the feedback node of the slave supply (often a compensation component). Increasing the capacitance on a slave supply's feedback node will further improve the noise immunity, but could affect the stability and transient response of the supply.

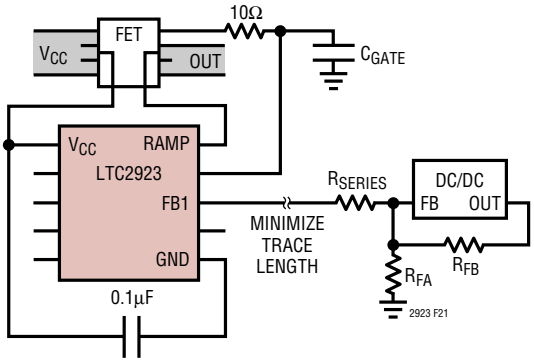
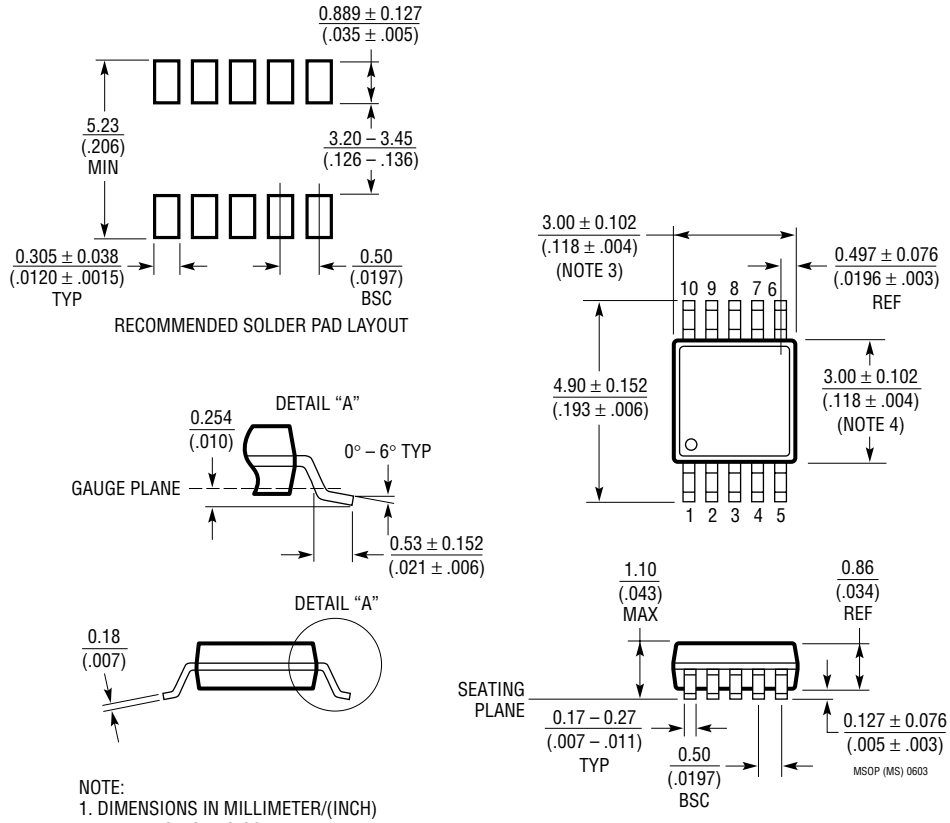


Figure 21. Layout Considerations

PACKAGE DESCRIPTION

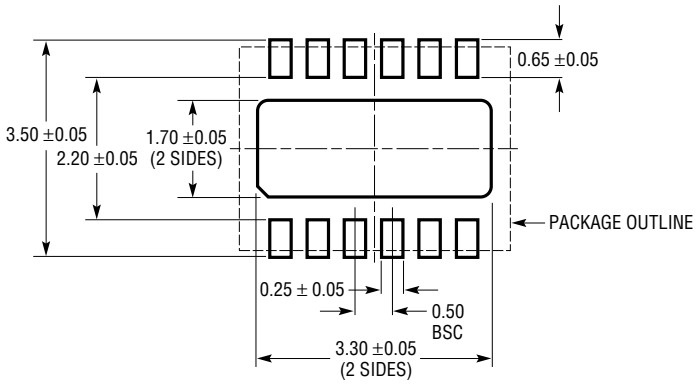
MS Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1661)



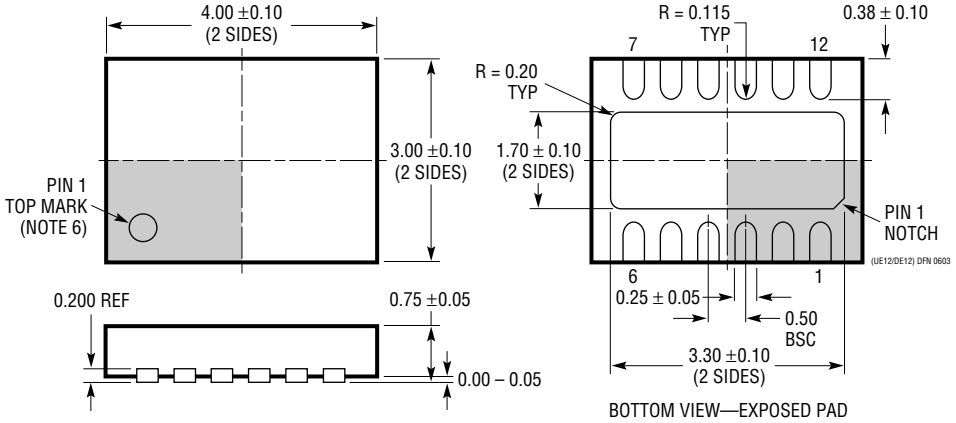
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

DE/UE Package
12-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1695)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

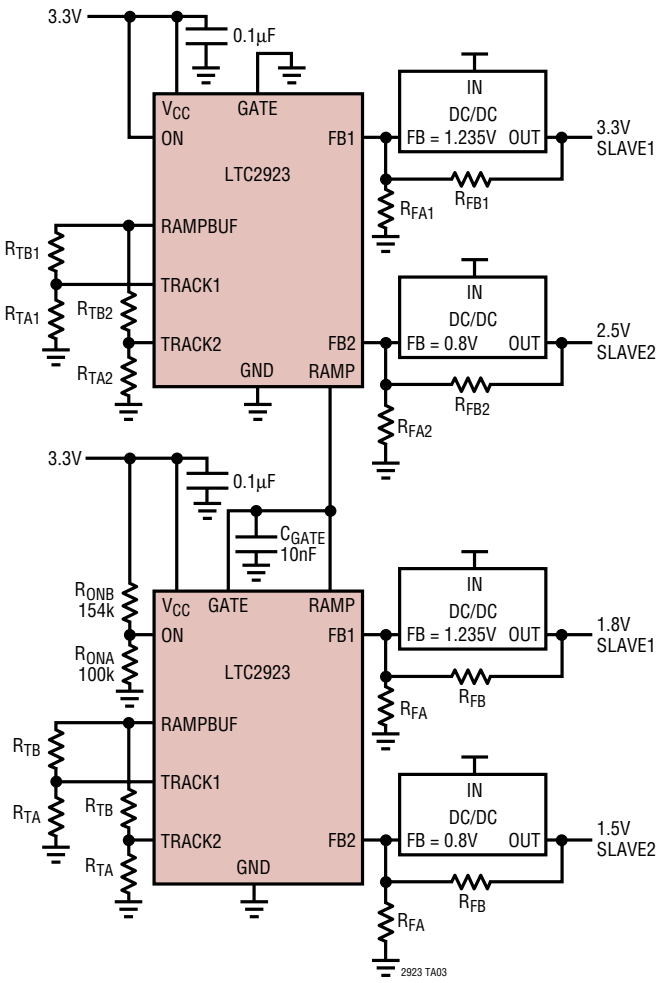


BOTTOM VIEW—EXPOSED PAD

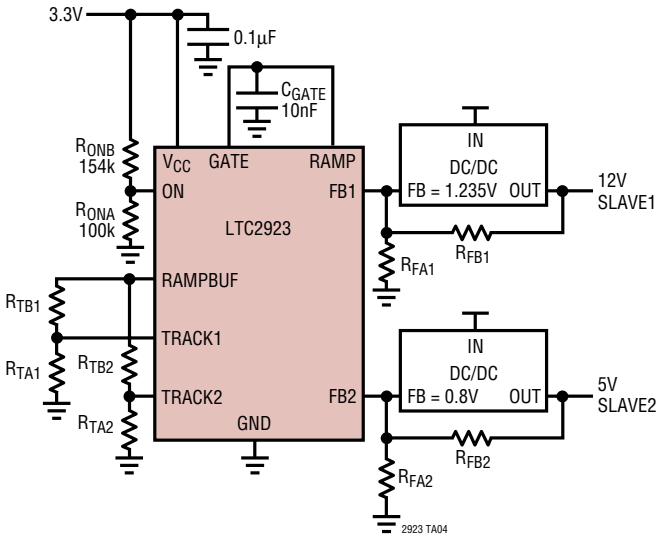
NOTE:
1. DRAWING PROPOSED TO BE A VARIATION OF VERSION (WGED) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATIONS

Daisy-Chained Application



High Voltage Supply Application



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1645	Dual Hot Swap™ Controller	Operates from 1.2V to 12V, Allows Supply Sequencing
LTC2920	Power Supply Margining Controller	Single or Dual Versions, Symmetric as Symmetric High and Low Margining
LTC2921/LTC2922	Power Supply Tracker with Input Monitors	Includes 3 (LTC2921) or 5 (LTC2922) Remote Sense Switches
LT®4220	Dual Supply Hot Swap Controller	±2.7V to ±16.5V, Supply Tracking Mode
LTC4230	Triple Hot Swap Controller with Multifunction Current Control	1.7V to 16.5V, Active Inrush Limiting, Fast Comparator
LTC4253	–48V Hot Swap Controller and Supply Sequencer	Floating Supply from –15V, Active Current Limiting, Enables Three DC/DC Converters

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