

## FEATURES

- Allows Safe Board Insertion and Removal from a Live PCI Slot
- Works on either a Motherboard (LTC1643H) or CompactPCI™ Card (LTC1643L/LTC1643L-1)
- Controls -12V, 3.3V, 5V, 12V Supplies
- Programmable Foldback Current Limit with Circuit Breaker
- User-Programmable Supply Voltage Power-Up Rate
- High Side Drive for External N-Channel MOSFETs
- -12V and 12V On-Chip Switches
- Fault and Power-Good Outputs

## APPLICATIONS

- PCI-Based Servers
- CompactPCI Compliant Boards

LT, LTC and LT are registered trademarks of Linear Technology Corporation.  
 Hot Swap is a trademark of Linear Technology Corporation.  
 CompactPCI is a trademark of PCI Industrial Computer Manufacturing Group.

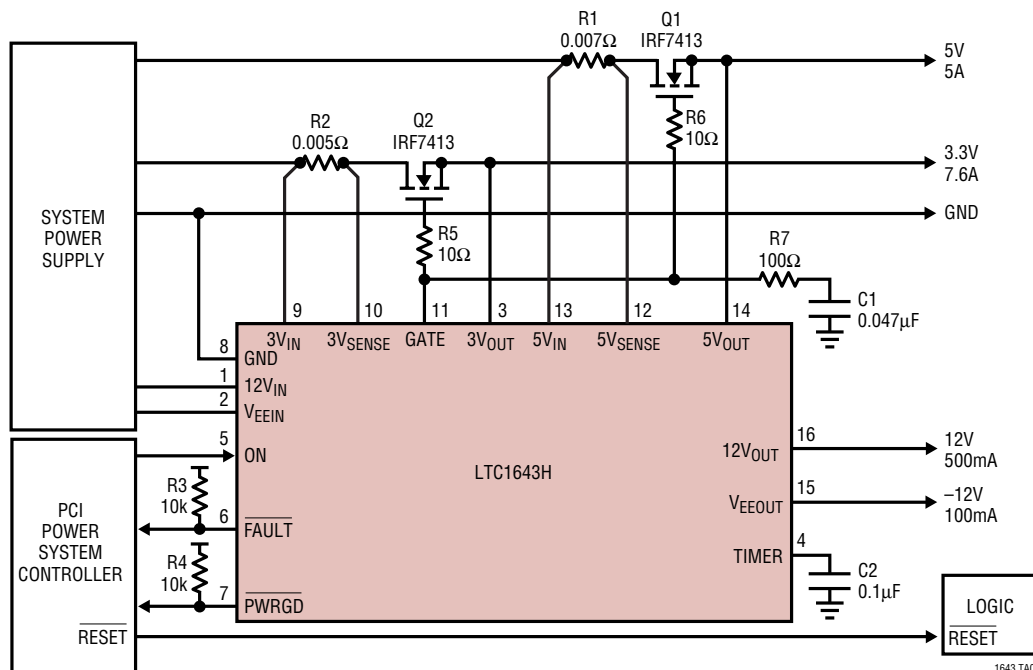
## DESCRIPTION

The LTC<sup>®</sup>1643 is a Hot Swap™ controller that allows a board to be safely inserted and removed from a live PCI-Bus slot. Two external N-channel transistors control the 3.3V and 5V supplies while on-chip switches control the -12V and 12V supplies. All supply voltages can be ramped up at a programmable rate. An electronic circuit breaker protects all four supplies against overcurrent faults. The foldback current limit feature limits current spikes and power dissipation when shorts occur and allows boards with large capacitances to be powered up without tripping the circuit breaker. The PWRGD output indicates when all of the supply voltages are within tolerance and the FAULT output indicates an overcurrent condition. The ON (LTC1643H)/ON (LTC1643L/LTC1643L-1) pin is used to cycle the board power or reset the circuit breaker. The LTC1643L-1 has the ±12V power good comparators disabled.

The LTC1643 is available in a 16-pin narrow SSOP package.

## TYPICAL APPLICATION

Hot Swappable PCI Supply



# LTC1643L/LTC1643L-1/LTC1643H

## ABSOLUTE MAXIMUM RATINGS

(Note 1)

### Supply Voltages

12V<sub>IN</sub> ..... 13.2V

V<sub>EEIN</sub> ..... -13.2V

Input Voltage (Pin 5) ..... -0.3V to (12V<sub>IN</sub> + 0.3V)

Output Voltages (Pins 6, 7) ..... -0.3V to (12V<sub>IN</sub> + 0.3V)

### Analog Voltages

(Pins 3, 4, 9, 10 to 14) ..... -0.3V to (12V<sub>IN</sub> + 0.3V)

V<sub>EEOUT</sub> ..... -13.2V to +0.3V

12V<sub>OUT</sub> ..... -0.3V to 13.2V

### Operating Temperature Range

LTC1643LC/LTC1643L-1C/LTC1643HC ... 0°C to 70°C

LTC1643LI/LTC1643HI ..... -40°C to 85°C

Storage Temperature Range ..... -65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

## PACKAGE/ORDER INFORMATION

TOP VIEW		ORDER PART NUMBER
12V <sub>IN</sub> [1]	[16] 12V <sub>OUT</sub>	LTC1643HCGN
V <sub>EEIN</sub> [2]	[15] V <sub>EEOUT</sub>	LTC1643LCGN
3V <sub>OUT</sub> [3]	[14] 5V <sub>OUT</sub>	LTC1643L-1CGN
TIMER [4]	[13] 5V <sub>IN</sub>	LTC1643HIGHN
ON/ <u>ON</u> * [5]	[12] 5V <sub>SENSE</sub>	LTC1643LIGN
FAULT [6]	[11] GATE	
PWRGD [7]	[10] 3V <sub>SENSE</sub>	GN PART MARKING
GND [8]	[9] 3V <sub>IN</sub>	1643H
GN PACKAGE 16-LEAD NARROW PLASTIC SSOP * ON FOR LTC1643H, ON FOR LTC1643L T <sub>JMAX</sub> = 150°C, θ <sub>JA</sub> = 135°C/W		1643L
		1643L1
		1643HI
		1643LI

Consult LTC Marketing for parts specified with wider operating temperature ranges.

## DC ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T<sub>A</sub> = 25°C.

V<sub>12VIN</sub> = 12V, V<sub>EE</sub> = -12V, V<sub>3VIN</sub> = 3.3V, V<sub>5VIN</sub> = 5V. (Note 2)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I <sub>DD</sub>	V <sub>12VIN</sub> Supply Current	<u>ON</u> = 3V, <u>ON</u> = GND	●	3.5	8	mA
V <sub>LKO</sub>	Undervoltage Lockout	12V <sub>IN</sub> 3V <sub>IN</sub> 5V <sub>IN</sub>	● ● ●	7 2.25 2.25	9.5 2.5 2.5	10.8 V 2.75 V
V <sub>FB</sub>	Foldback Current Limit Voltage	V <sub>FB</sub> = (V <sub>5VIN</sub> - V <sub>5VSENSE</sub> ), V <sub>5VOUT</sub> = 0V V <sub>FB</sub> = (V <sub>5VIN</sub> - V <sub>5VSENSE</sub> ), V <sub>5VOUT</sub> > 4V V <sub>FB</sub> = (V <sub>3VIN</sub> - V <sub>3VSENSE</sub> ), V <sub>3VOUT</sub> = 0V V <sub>FB</sub> = (V <sub>3VIN</sub> - V <sub>3VSENSE</sub> ), V <sub>3VOUT</sub> > 2V	● ● ● ●	4 40 4 40	7.5 53 7.5 53	12 mV 65 mV 12 mV 65 mV
t <sub>CB</sub>	Circuit Breaker Trip Filter Time			14.6		μs
I <sub>CP</sub>	GATE Pin Output Current	Charge Pump On, V <sub>GATE</sub> = GND, <u>FAULT</u> = High Charge Pump Off, V <sub>GATE</sub> = 5V, <u>FAULT</u> = High Charge Pump Off, V <sub>GATE</sub> = 2V, <u>FAULT</u> = Low	● ●	-20 3	-50 10	-100 20 μA mA
ΔV <sub>GATE</sub>	External Gate Voltage	(V <sub>12VIN</sub> - V <sub>GATE</sub> )		100	200	mV
V <sub>DROP</sub>	Internal Switch Voltage Drop	(V <sub>12VIN</sub> - V <sub>12VOUT</sub> ), I <sub>12VOUT</sub> = 500mA (V <sub>EEOUT</sub> - V <sub>EEIN</sub> ), I <sub>VEEIN</sub> = 100mA	● ● ●	250 250	600 750	mV mV
I <sub>CL</sub>	Current Foldback	12V <sub>IN</sub> = 12V, 12V <sub>OUT</sub> = 0V 12V <sub>IN</sub> , 12V <sub>OUT</sub> = 12V V <sub>EEIN</sub> = -12V, V <sub>EEOUT</sub> = 0V (LTC1643L/LTC1643H Only) V <sub>EEIN</sub> , V <sub>EEOUT</sub> = -12V	● ● ● ●	50 525 100 225	250 850 160 450	500 1500 500 800 mA mA mA mA
T <sub>TS</sub>	Thermal Shutdown Temperature			150		°C
V <sub>TH</sub>	Power-Good Threshold Voltage	V <sub>12VOUT</sub> LTC1643H/LTC1643L Only V <sub>EEOUT</sub> LTC1643H/LTC1643L Only	● ● ● ●	10.8 10.4	11.1 11.1	11.4 11.4 V V
		0°C ≤ T <sub>A</sub> ≤ 70°C -40°C ≤ T <sub>A</sub> ≤ 85°C				
		0°C ≤ T <sub>A</sub> ≤ 70°C -40°C ≤ T <sub>A</sub> ≤ 85°C	● ●	-10.2 -10.0	-10.5 -10.5	-10.8 -10.8 V V

## DC ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are  $T_A = 25^\circ\text{C}$ .  
 $V_{12VIN} = 12\text{V}$ ,  $V_{EE} = -12\text{V}$ ,  $V_{3VIN} = 3.3\text{V}$ ,  $V_{5VIN} = 5\text{V}$ . (Note 2)

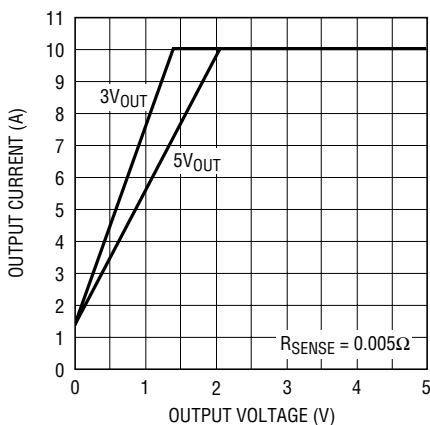
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
$V_{TH}$	Power-Good Threshold Voltage	$V_{3VOUT}$	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	● 2.8	2.9	3.0	V
			$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	● 2.75	2.9	3.0	V
		$V_{5VOUT}$	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	● 4.5	4.65	4.75	V
			$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	● 4.4	4.65	4.75	V
$V_{IL}$	Input Low Voltage	ON/ON, FAULT	●		0.8	V	
$V_{IH}$	Input High Voltage	ON/ON, FAULT	●	2		V	
$V_{OL}$	Output Low Voltage	FAULT, PWRGD, I = 3mA	●		0.4	V	
$I_{IN}$	ON/ON Pin Input Current	ON/ON = GND ON/ON = 12VIN	●	$\pm 0.08$	$\pm 10$	$\mu\text{A}$	
	5VSENSE Input Current	5VSENSE = 5V	●	50	100	$\mu\text{A}$	
	3VSENSE Input Current	3VSENSE = 3V	●	50	100	$\mu\text{A}$	
	5VIN Input Current	5VIN = 5V	●	460	700	$\mu\text{A}$	
	3VIN Input Current	3VIN = 3V	●	320	600	$\mu\text{A}$	
	5VOUT Input Current	5VOUT = 5V, ON = 3V, ON = GND	●	240	500	$\mu\text{A}$	
	3VOUT Input Current	3VOUT = 3.3V, ON = 3V, ON = GND	●	220	500	$\mu\text{A}$	
$R_{DIS}$	5VOUT Discharge Impedance	ON = GND or ON = 3V		100		$\Omega$	
	3VOUT Discharge Impedance	ON = GND or ON = 3V		70		$\Omega$	
	12VOUT Discharge Impedance	ON = GND or ON = 3V		450		$\Omega$	
	V <sub>EE</sub> OUT Discharge Impedance	ON = GND or ON = 3V		1600		$\Omega$	
$I_{TIMER}$	TIMER Pin Current	Timer On, $V_{TIMER} = \text{GND}$	●	-15	-22	$\mu\text{A}$	
		Timer Off, $V_{TIMER} = 5\text{V}$			45	mA	
$V_{TIMER}$	TIMER Threshold Voltage	( $V_{12VIN} - V_{TIMER}$ )	●	0.5	0.9	1.3	V

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

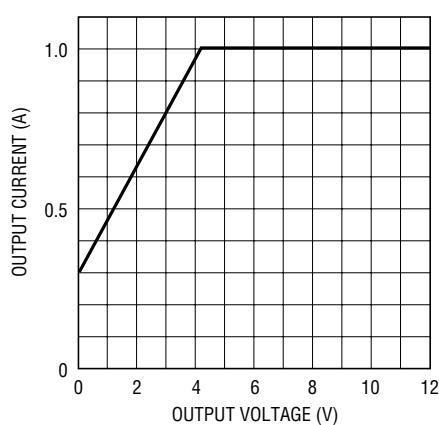
## TYPICAL PERFORMANCE CHARACTERISTICS

3.3V and 5V Current Foldback Profile



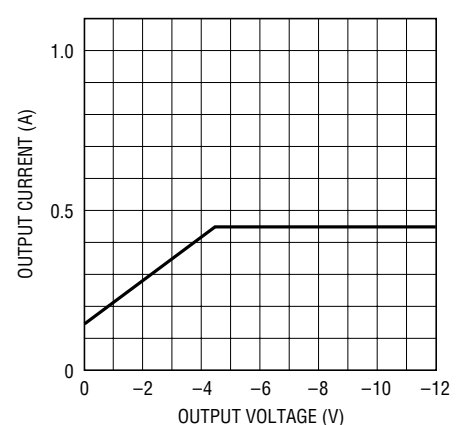
1643 G01

12V Current Foldback Profile



1643 G02

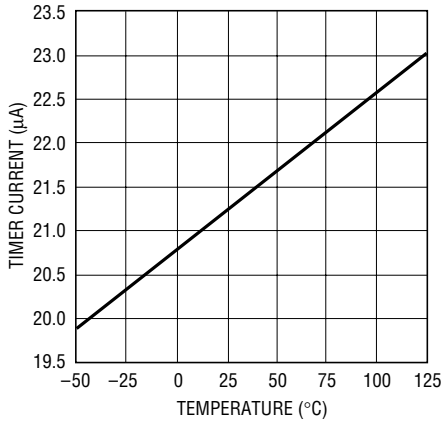
-12V Current Foldback Profile



1643 G03

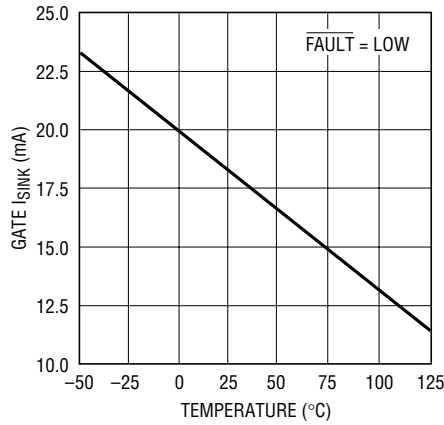
# TYPICAL PERFORMANCE CHARACTERISTICS

**Timer Current vs Temperature**



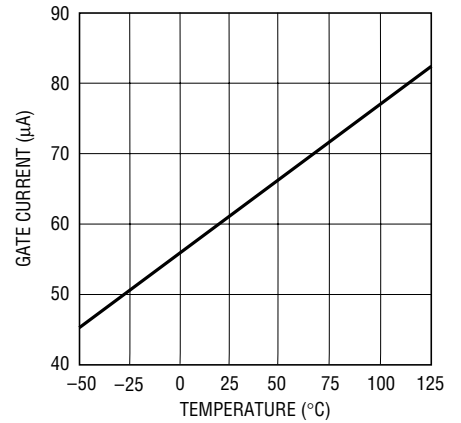
1643 G04

**Gate I<sub>SINK</sub> vs Temperature**



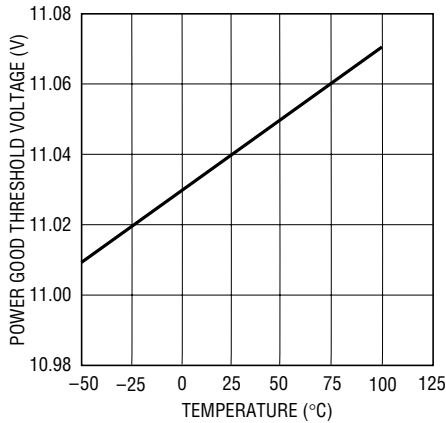
1643 G05

**Gate Current vs Temperature**



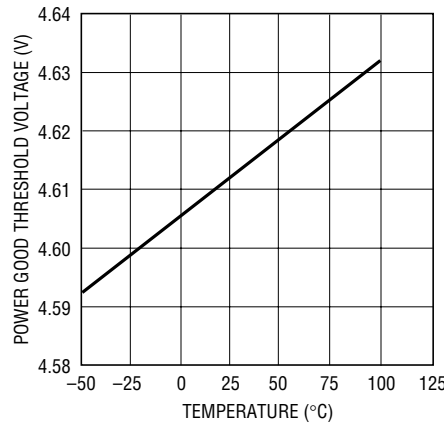
1643 G06

**Power Good Threshold Voltage vs Temperature (12V<sub>OUT</sub>)**



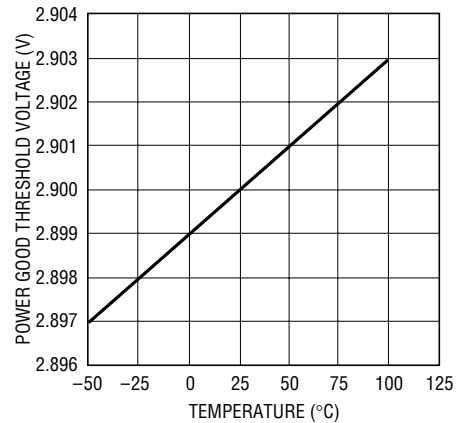
1643 G07

**Power Good Threshold Voltage vs Temperature (5V<sub>OUT</sub>)**



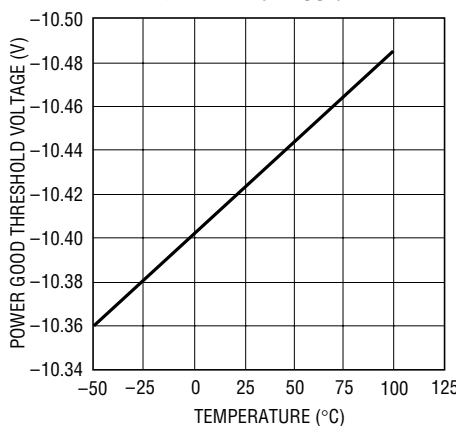
1643 G08

**Power Good Threshold Voltage vs Temperature (3V<sub>OUT</sub>)**



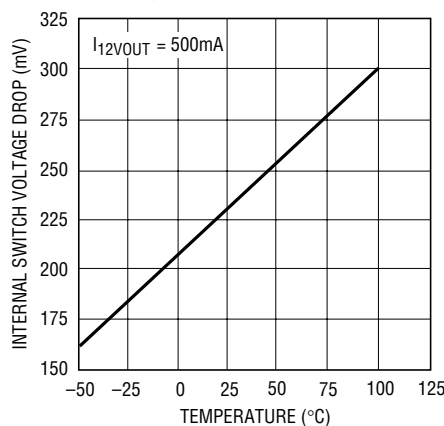
1643 G09

**Power Good Threshold Voltage vs Temperature (V<sub>EEOUT</sub>)**



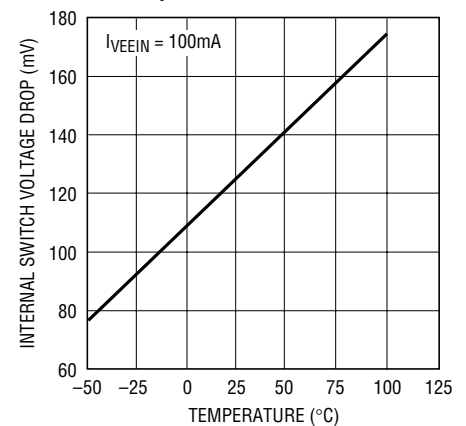
1643 G10

**12V Internal Switch Voltage Drop vs Temperature**



LT1643 G11

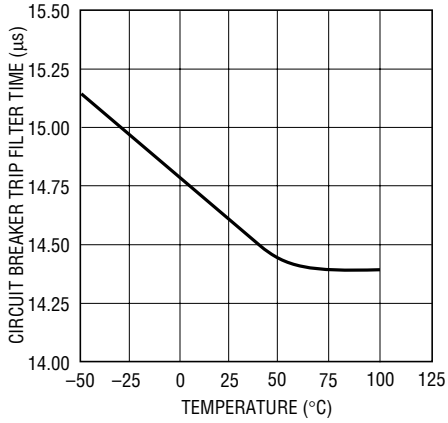
**V<sub>EE</sub> Internal Switch Voltage Drop vs Temperature**



1643 G12

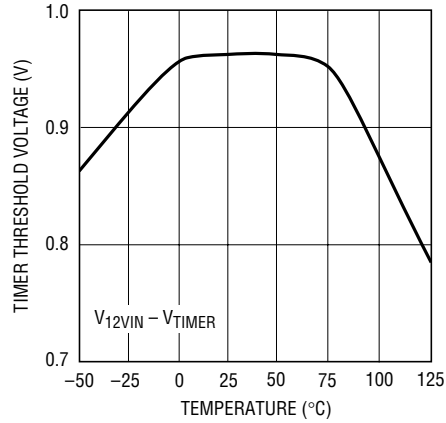
# TYPICAL PERFORMANCE CHARACTERISTICS

**Circuit Breaker Trip Filter Time vs Temperature**



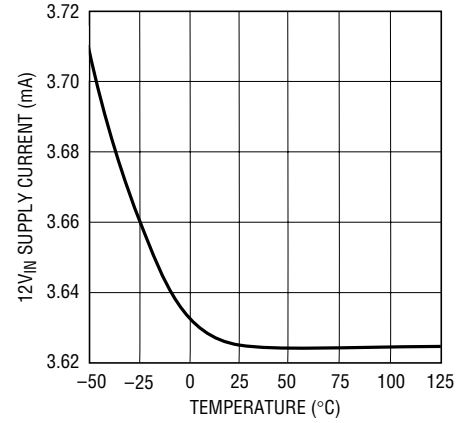
1643 G13

**Timer Threshold Voltage vs Temperature**



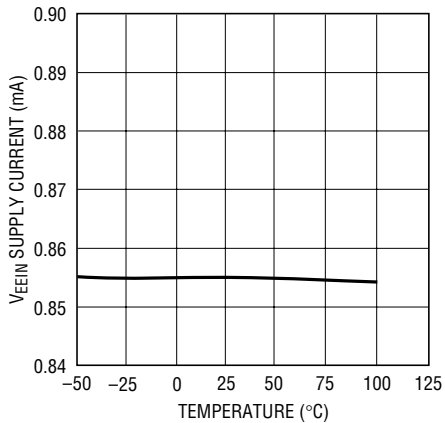
1643 G14

**12V<sub>IN</sub> Supply Current vs Temperature**



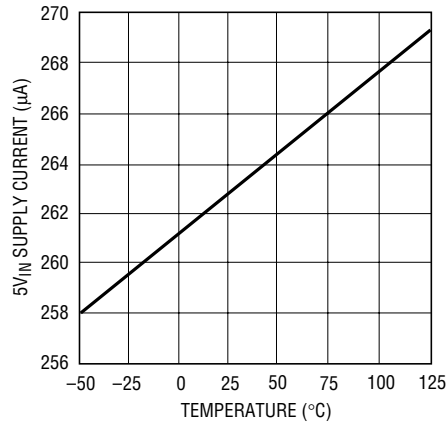
1643 G15

**V<sub>EEIN</sub> Supply Current vs Temperature**



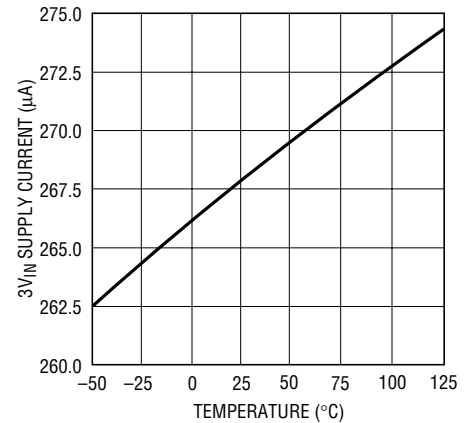
1643 G16

**5V<sub>IN</sub> Supply Current vs Temperature**



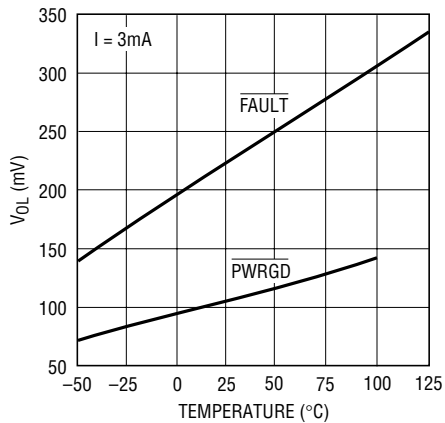
LT1643 G17

**3V<sub>IN</sub> Supply Current vs Temperature**



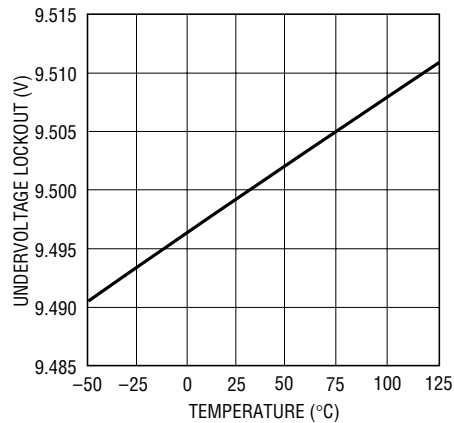
1643 G18

**V<sub>OL</sub> vs Temperature**



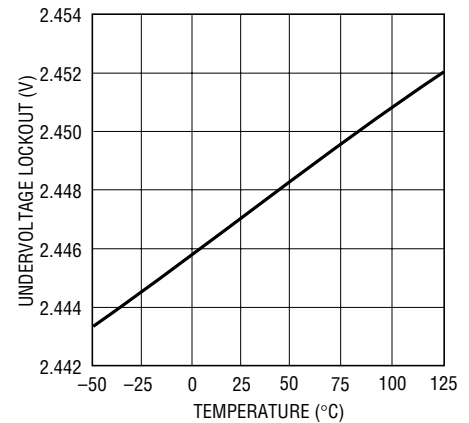
1643 G19

**12V<sub>IN</sub> Undervoltage Lockout vs Temperature**



1643 G20

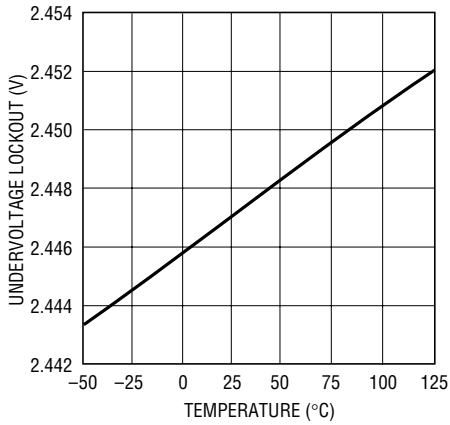
**5V<sub>IN</sub> Undervoltage Lockout vs Temperature**



1643 G21

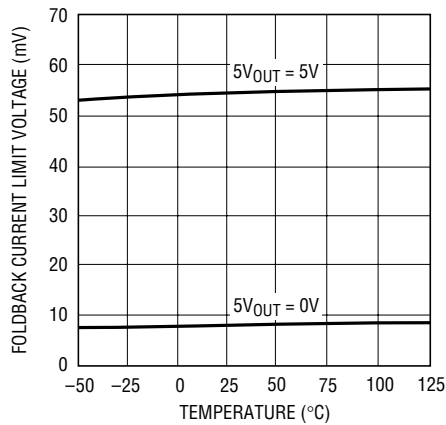
## TYPICAL PERFORMANCE CHARACTERISTICS

**3V<sub>IN</sub> Undervoltage Lockout vs Temperature**



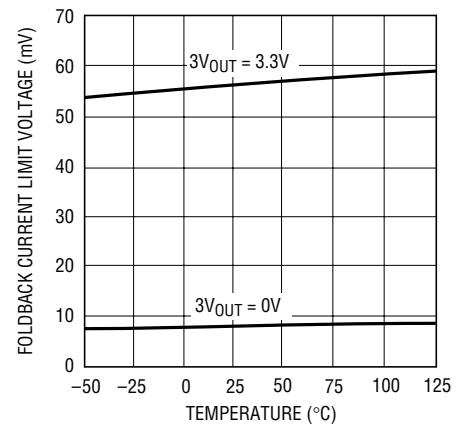
1643 G21

**5V<sub>IN</sub> Foldback Current Limit Voltage vs Temperature**



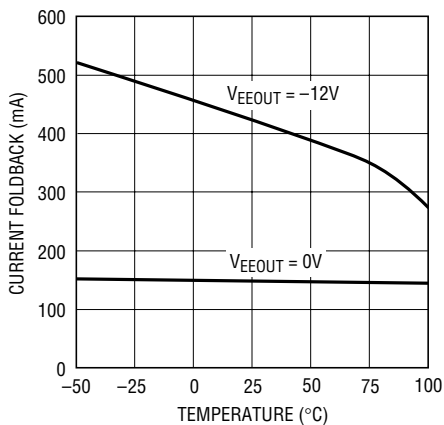
LT1643 G23

**3V<sub>IN</sub> Foldback Current Limit Voltage vs Temperature**



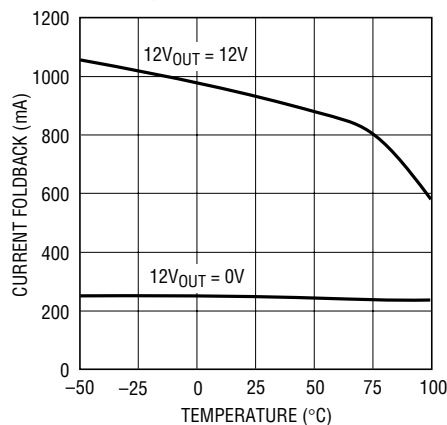
LT1643 G24

**V<sub>EE</sub> Current Foldback vs Temperature**



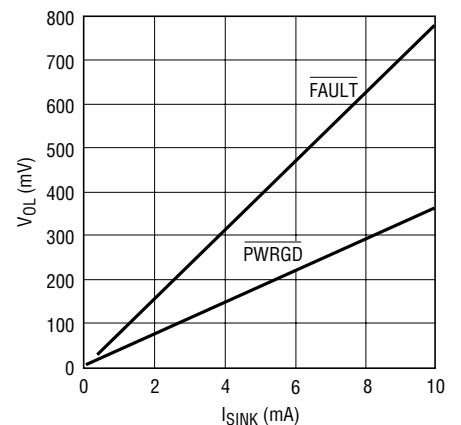
1643 G25

**12V Current Foldback vs Temperature**



1643 G26

**V<sub>OL</sub> vs I<sub>SINK</sub> (25°C)**



1643 G27

## PIN FUNCTIONS

**12V<sub>IN</sub> (Pin 1):** 12V Supply Input. It powers all the chip's internal circuitry. A 0.5Ω switch is connected between 12V<sub>IN</sub> and 12V<sub>OUT</sub> with a foldback current limit. An undervoltage lockout circuit prevents the switches from turning on while the 12V<sub>IN</sub> pin voltage is less than 9.5V typically.

**V<sub>EEIN</sub> (Pin 2):** -12V Supply Input. A 1.2Ω switch is connected between V<sub>EEIN</sub> and V<sub>EEOUT</sub> with a foldback current limit.

**3V<sub>OUT</sub> (Pin 3):** Analog Input. Used to monitor the 3.3V output supply voltage. The PWRGD signal cannot go high until the 3V<sub>OUT</sub> pin exceeds 2.9V typically.

**TIMER (Pin 4):** Analog Current Fault Inhibit Timing Input. Connect a capacitor from  $\overline{\text{TIMER}}$  to GND. With the chip turned off (ON = GND or  $\overline{\text{ON}}$  = High) or the internal circuit breaker tripped ( $\overline{\text{FAULT}}$  = GND), the TIMER pin is internally held at GND. When the chip is turned on, a 20μA pull-up current source is connected to TIMER. Current limit faults will be ignored until the voltage at the TIMER pin rises to within 0.9V of 12V<sub>IN</sub>.

**ON/ $\overline{\text{ON}}$  (Pin 5):** Digital Input. The LTC1643L/LTC1643L-1 have an active low enable,  $\overline{\text{ON}}$ , and the LTC1643H has an active high enable, ON. When the ON pin is pulled high or

## PIN FUNCTIONS

the  $\overline{\text{ON}}$  pin pulled low, the GATE pin is pulled high by a  $50\mu\text{A}$  current source and the internal 12V and  $-12\text{V}$  switches are turned on. When the ON pin is pulled low or the  $\overline{\text{ON}}$  pin pulled high, the GATE pin will be pulled to ground by a  $200\mu\text{A}$  current source and the 12V and  $-12\text{V}$  switches turned off.

The ON/ $\overline{\text{ON}}$  pin is also used to reset the electronic circuit breaker. If the ON/ $\overline{\text{ON}}$  pin is cycled following the trip of the circuit breaker, the circuit breaker is reset and a normal power-up sequence will occur.

**FAULT (Pin 6):** Open-Drain Digital I/O.  $\overline{\text{FAULT}}$  is pulled low when a current limit fault is detected. Current limit faults are ignored while the voltage at the TIMER pin is less than  $12\text{V}_{\text{IN}} - 0.9\text{V}$ . Once the TIMER cycle is complete,  $\overline{\text{FAULT}}$  will pull low typically  $14.6\mu\text{s}$  after any of the supplies go into current limit. At the same time, the GATE and TIMER pins are pulled to GND and the 12V and  $-12\text{V}$  switches are turned off. The chip will remain latched in the off state until the ON/ $\overline{\text{ON}}$  pin is toggled or the power is cycled.

Forcing the  $\overline{\text{FAULT}}$  pin low with an external pull-down will immediately turn off the internal switches and force the GATE and TIMER pins to GND independent of the state of the ON/ $\overline{\text{ON}}$  pin. However, the chip is not latched into the off state, so when the  $\overline{\text{FAULT}}$  pin is released, the state of the chip will be determined by the ON pin.

**PWRGD (Pin 7):** Open-Drain Digital Power-Good Output. PWRGD remains low while  $V_{12\text{VOUT}} \geq 11.4\text{V}$ ,  $V_{3\text{VOUT}} \geq 3\text{V}$ ,  $V_{5\text{VOUT}} \geq 4.75\text{V}$  and  $V_{\text{EEOUT}} \leq -10.8\text{V}$ . The LTC1643L-1 has the power good comparators connected to the  $12\text{V}_{\text{OUT}}$  and  $V_{\text{EEOUT}}$  pins disabled, with only the  $3\text{V}_{\text{OUT}}$  and  $5\text{V}_{\text{OUT}}$  outputs being monitored to generate PWRGD. When one of the supplies falls below its power-good threshold voltage, PWRGD will go high after a  $15\mu\text{s}$  deglitching time. The switches will *not* be turned off when PWRGD goes high.

**GND (Pin 8):** Chip Ground.

**$3\text{V}_{\text{IN}}$  (Pin 9):** 3.3V Supply Sense Input. An undervoltage lockout circuit prevents the switches from turning on when the voltage at the  $3\text{V}_{\text{IN}}$  pin is less than 2.5V typically. If no 3.3V input supply is available, tie  $3\text{V}_{\text{IN}}$  to the  $5\text{V}_{\text{IN}}$  pin.

**$3\text{V}_{\text{SENSE}}$  (Pin 10):** The 3.3V Current Limit Set Pin. With a sense resistor placed in the supply path between  $3\text{V}_{\text{IN}}$  and  $3\text{V}_{\text{SENSE}}$ , the GATE pin voltage will be adjusted to maintain a constant voltage across the sense resistor and a constant current through the switch. A foldback feature makes the current limit decrease as the voltage at the  $3\text{V}_{\text{OUT}}$  pin approaches GND. To disable the current limit,  $3\text{V}_{\text{SENSE}}$  and  $3\text{V}_{\text{IN}}$  can be shorted together.

**GATE (Pin 11):** High Side Gate Drive for the External N-Channel Pass Transistors. Requires an external series RC network for the current limit loop compensation and setting the minimum ramp-up rate. During power-up, the slope of the voltage rise at the GATE is set by the  $50\mu\text{A}$  current source connected to  $12\text{V}_{\text{IN}}$  and the external capacitor connected to GND or by the 3.3V or 5V current limit and the bulk capacitance on the  $3\text{V}_{\text{OUT}}$  or  $5\text{V}_{\text{OUT}}$  supply lines. During power-down, the slope of the falling voltage is set by the  $200\mu\text{A}$  current source connected to GND and the external GATE capacitor.

The voltage at the GATE pin will be modulated to maintain a constant current when either the 3V or 5V supplies go into current limit. When a current limit fault occurs after the inhibit period set by the TIMER pin capacitance, the undervoltage lockout circuit on 3.3V, 5V or 12V trips or the  $\overline{\text{FAULT}}$  pin is pulled low, the GATE pin is immediately pulled to GND.

**$5\text{V}_{\text{SENSE}}$  (Pin 12):** 5V Current Limit Set Pin. With a sense resistor placed in the supply path between  $5\text{V}_{\text{IN}}$  and  $5\text{V}_{\text{SENSE}}$ , the GATE pin voltage will be adjusted to maintain a constant voltage across the sense resistor and a constant current through the switch. A foldback feature makes the current limit decrease as the voltage at the  $5\text{V}_{\text{OUT}}$  pin approaches GND. To disable the current limit,  $5\text{V}_{\text{SENSE}}$  and  $5\text{V}_{\text{IN}}$  can be shorted together.

**$5\text{V}_{\text{IN}}$  (Pin 13):** Analog Input. Used to monitor the 5V input supply voltage. An undervoltage lockout circuit prevents the switches from turning on when the voltage at the  $5\text{V}_{\text{IN}}$  pin is less than 2.5V typically.

**$5\text{V}_{\text{OUT}}$  (Pin 14):** Analog Input. Used to monitor the 5V output supply voltage. The PWRGD signal cannot go high until the  $5\text{V}_{\text{OUT}}$  pin exceeds 4.65V typically.

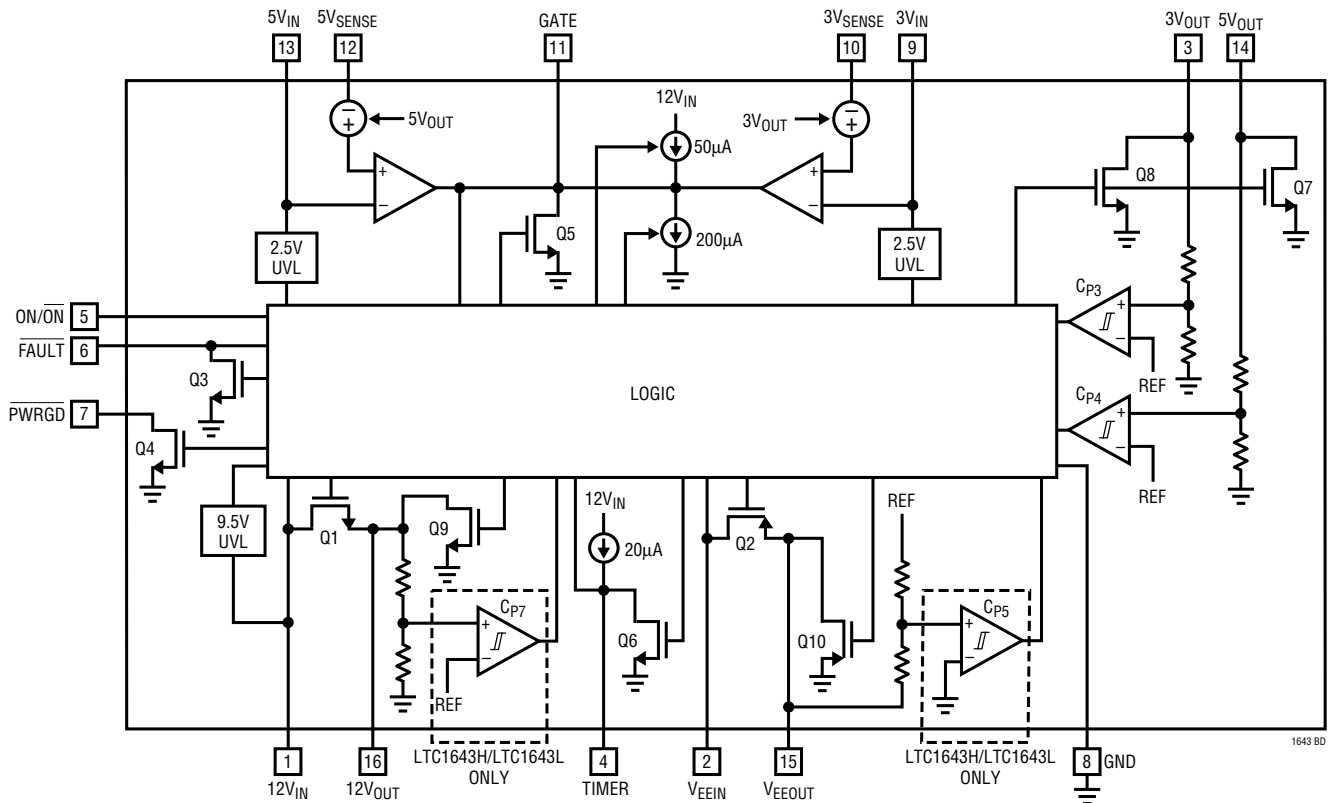


## PIN FUNCTIONS

**V<sub>EEOUT</sub> (Pin 15):** -12V Supply Output. A 1.2Ω switch is connected between V<sub>EEIN</sub> and V<sub>EEOUT</sub>. V<sub>EEOUT</sub> must exceed -10.8V before the PWRGD signal can go high on the LTC1643H and LTC1643L.

**12V<sub>OUT</sub> (Pin 16):** 12V Supply Output. A 0.5Ω switch is connected between 12V<sub>IN</sub> and 12V<sub>OUT</sub>. 12V<sub>OUT</sub> must exceed 11.4V before the PWRGD signal can go high on the LTC1643H and LTC1643L.

## BLOCK DIAGRAM



## APPLICATIONS INFORMATION

### Hot Circuit Insertion

When a circuit board is inserted into a live PCI slot, the supply bypass capacitors on the board can draw huge transient currents from the PCI power bus as they charge up. The transient currents can cause permanent damage to the connector pins and cause glitches on the power bus, causing other boards in the system to reset.

The LTC1643 is designed to turn a board's supply voltages on and off in a controlled manner, allowing the board to be

safely inserted or removed from a live PCI slot without glitching the system power supplies. The chip also protects the PCI supplies from shorts and monitors the supply voltages.

The LTC1643H is designed for motherboard applications, while the LTC1643L/LTC1643L-1 are designed for CompactPCI applications where the chip resides on the plug-in board.



## APPLICATIONS INFORMATION

### LTC1643 FEATURE SUMMARY

1. Allows safe board insertion and removal from either a motherboard (LTC1643H) or CompactPCI board (LTC1643L/LTC1643L-1).
2. Controls all four PCI supplies: -12V, 12V, 3.3V and 5V.
3. Programmable foldback current limit: a programmable analog current limit with a value that depends on the output voltage. If the output is shorted to ground, the current limit drops to keep power dissipation and supply glitches to a minimum.
4. Programmable circuit breaker: if a supply remains in current limit too long, the circuit breaker will trip, the supplies will be turned off and the FAULT pin pulled low.
5. Current limit power-up: the supplies are allowed to power up in current limit. Allows the chip to power up boards with widely varying capacitive loads without tripping the circuit breaker. The maximum allowable power-up time is programmable using the TIMER pin.
6. -12V and 12V power switches on chip.
7. Power good output: monitors the voltage status of the four supply voltages, except the LTC1643L-1 which only monitors 3V<sub>OUT</sub> and 5V<sub>OUT</sub>.
8. Space saving 16-pin SSOP package.

### PCI Power Requirements

PCI systems usually require four power rails: 5V, 3.3V, 12V and -12V. Systems implementing the 3.3V signaling environment are usually required to provide all four rails in every system. Systems implementing the 5V signaling environment may either ship the 3.3V supply with the system or provide a means to add it afterward. The tolerance of the supplies as measured at the components on the plug-in card is summarized in Table 1.

**Table 1. PCI Power Supply Requirements**

SUPPLY	TOLERANCE	CAPACITIVE LOAD
5V	5V ±5%	<3000μF
3.3V	3.3V ±0.3V	<3000μF
12V	12V ±5%	<500μF
-12V	-12V ±10%	<120μF

Some ±12V supplies in CompactPCI applications are not well regulated and can violate the tolerance specification. For these applications, the LTC1643L-1 should be used because the PWRGD signal does not depend on ±12V outputs.

### Power-Up Sequence

The power supplies are controlled by placing external N-channel pass transistors in the 3.3V and 5V power paths, and internal pass transistors for the 12V and -12V power paths (Figure 1).

Resistors R1 and R2 provide current fault detection and R7 and C1 provide current control loop compensation. Resistors R5 and R6 prevent high frequency oscillations in Q1 and Q2.

When the ON pin (Pin 5) is pulled high, the pass transistors are allowed to turn on and a 20μA current source is connected to the TIMER pin (Pin 4) (Figure 2).

The current in each pass transistor increases until it reaches the current limit for each supply. Each supply is then allowed to power up at the rate  $dv/dt = 50\mu A/C1$  or as determined by the current limit and the load capacitance whichever is slower. Current limit faults are ignored while the TIMER pin (Pin 4) voltage is ramping up and is less than 0.9V below 12V<sub>IN</sub> (Pin 1). Once all four supply voltages are within tolerance, the PWRGD pin (Pin 7) will pull low.

### Power-Down Sequence

When the ON (Pin 5) is pulled low, a power-down sequence begins (Figure 3).

Internal switches are connected to each of the output supply voltage pins to discharge the bypass capacitors to ground. The TIMER pin (Pin 4) is immediately pulled low. The GATE pin (Pin 11) is pulled down by a 200μA current source to prevent the load currents on the 3.3V and 5V supplies from going to zero instantaneously and glitching the power supply voltages. When any of the output voltages dip below its threshold, the PWRGD pin (Pin 7) pulls high.

APPLICATIONS INFORMATION

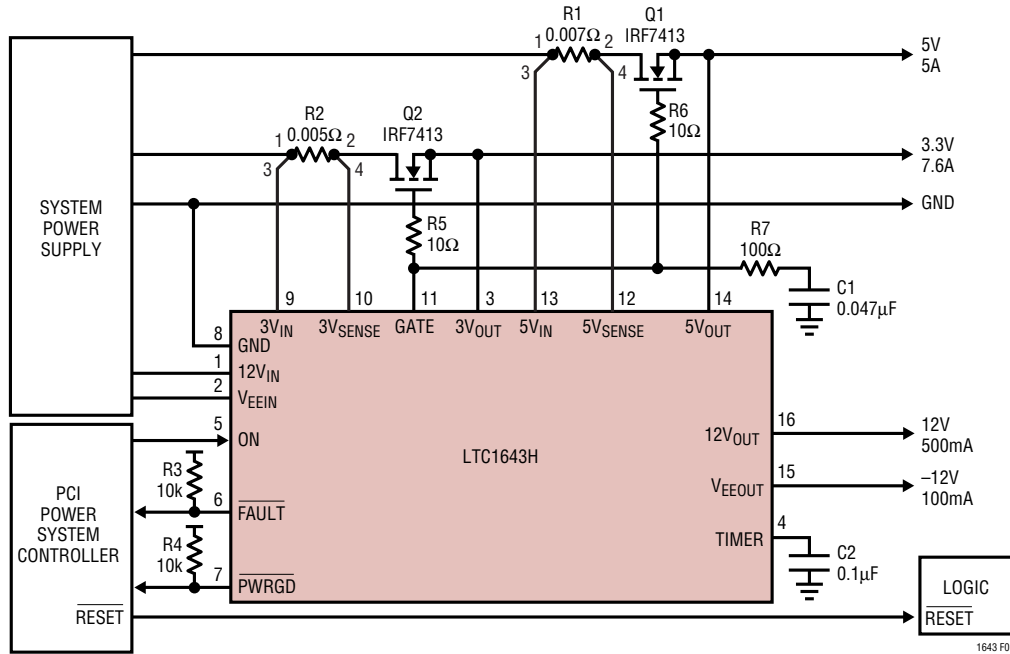


Figure 1. Typical Application

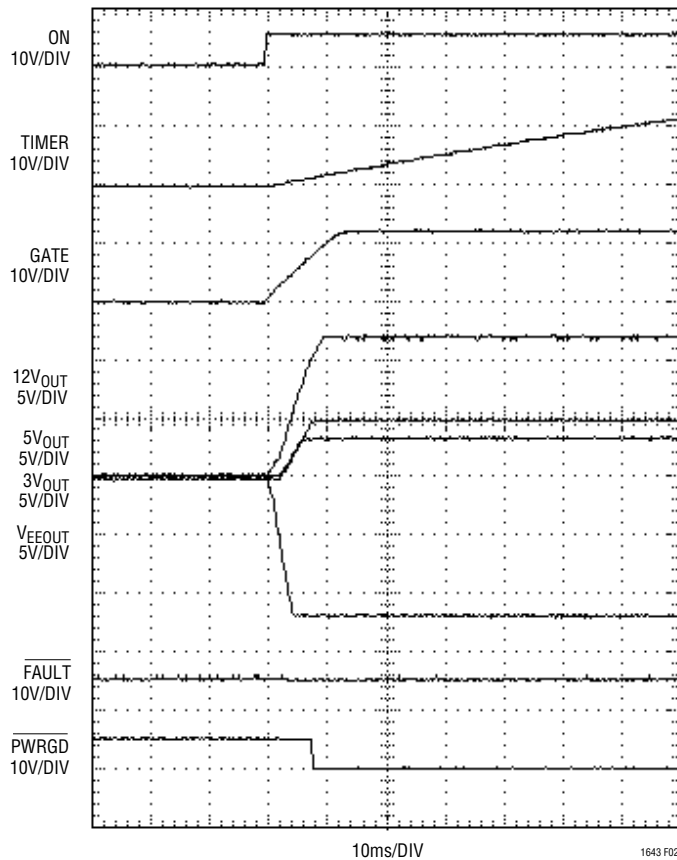


Figure 2. Normal Power-Up Sequence

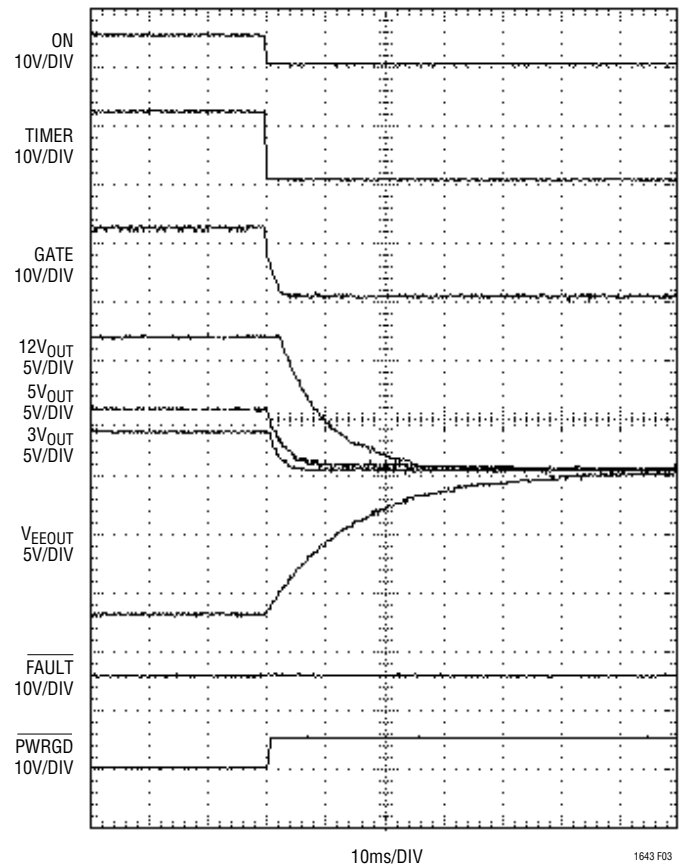


Figure 3. Normal Power-Down Sequence

## APPLICATIONS INFORMATION

### Timer

During a power-up sequence, a 20 $\mu$ A current source is connected to the TIMER pin (Pin 4) and current limit faults are ignored until the voltage ramps to within 0.9V of 12V<sub>IN</sub> (Pin 1). This feature allows the chip to power up a PCI slot that can accept boards with widely varying capacitive loads on the supplies. The power-up time will be:

$$t_{ON} \cong 2 \frac{C_{SUPPLY} \cdot V_{SUPPLY}}{I_{LIMIT} - I_{LOAD}}$$

For  $C_{SUPPLY} = 2000\mu\text{F}$ ,  $V_{SUPPLY} = 5\text{V}$ ,  $I_{LIMIT} = 7\text{A}$ ,  $I_{LOAD} = 5\text{A}$ , the turn-on time will be ~10ms. The timer period should be set longer than the maximum supply turn-on time but short enough to not exceed the maximum safe operating area of the pass transistor during a short circuit. The timer period will be:

$$t_{TIMER} = \frac{C_{TIMER} \cdot 11.1\text{V}}{22\mu\text{A}}$$

For  $C_{TIMER} = 0.1\mu\text{F}$ , the timer period will be ~50ms. The TIMER pin (Pin 4) is immediately pulled low when ON (Pin 5) goes low.

### Thermal Shutdown

The internal switches for the 12V and –12V supplies are protected by an internal current limit and thermal shutdown circuit. When the temperature of chip reaches 150°C, all switches will be latched off and the  $\overline{\text{FAULT}}$  pin (Pin 6) will be pulled low.

### Short-Circuit Protection

During a normal power-up sequence, if the TIMER (Pin 4) is done ramping and a supply is still in current limit, all of the pass transistors will be immediately turned off and the  $\overline{\text{FAULT}}$  pin (Pin 6) will be pulled low as shown in Figure 4.

If a short circuit occurs after the supplies are powered up, the shorted supply's current will drop immediately to the limit value (Figure 5).

If the supply remains in current limit for more than 15 $\mu$ s, all of the supplies will be latched off. The 15 $\mu$ s delay prevents quick current spikes—for example, from a fan

turning on—from causing false trips of the circuit breaker. The chip will stay in the latched-off state until ON (Pin 5) is cycled low then high, or the 12V<sub>IN</sub> pin (Pin 1) power supply is cycled.

To prevent excessive power dissipation in the pass transistors and to prevent voltage spikes on the supplies during short-circuit conditions, the current limit on each supply is designed to be a function of the output voltage. As the output voltage drops, the current limit decreases. Unlike a traditional circuit breaker function where huge currents can flow before the breaker trips, the current foldback feature assures that the supply current will be kept at a safe level and prevent voltage glitches when powering up into a short.

The current limit for the 5V and 3.3V supplies is set by placing a sense resistor between 5V<sub>IN</sub> (Pin 13) and 5V<sub>SENSE</sub> (Pin 12) and between 3V<sub>IN</sub> (Pin 9) and 3V<sub>SENSE</sub> (Pin 10). The current limit will be set by:

$$I_{LIMIT} = 53\text{mV}/R_{SENSE}$$

For a 0.005 $\Omega$  resistor, the current limit will be set at 10.6A and fold back to 1.5A when the output is shorted. For a 0.007 $\Omega$  resistor, the current limit will be set at 7.6A and fold back to 1.1A when the output is shorted.

The current limit for the internal 12V switch is set at 850mA folding back to 250mA and the –12V switch at 450mA folding back to 160mA.

In systems where it is possible to exceed the current limit for a short amount of time, it might be necessary to prevent the analog current loop from responding quickly so the output voltage does not droop. This can be accomplished by adding an RC filter across the sense resistor as shown in Figure 6. R4 should be 20 $\Omega$  or less to prevent offset errors. A 0.1 $\mu$ F capacitor gives a delay of about 1.5 $\mu$ s and a 1 $\mu$ F capacitor gives a delay of about 15 $\mu$ s.

### CompactPCI Application

The LTC1643L is designed for hot swapping CompactPCI boards. The typical application is shown in Figure 7. The 3.3V, 5V, 12V and –12V inputs to the LTC1643L come from the medium length power pins. The long 3.3V, 5V and V(I/O) pins power up the pull-up resistors, bus precharge

APPLICATIONS INFORMATION

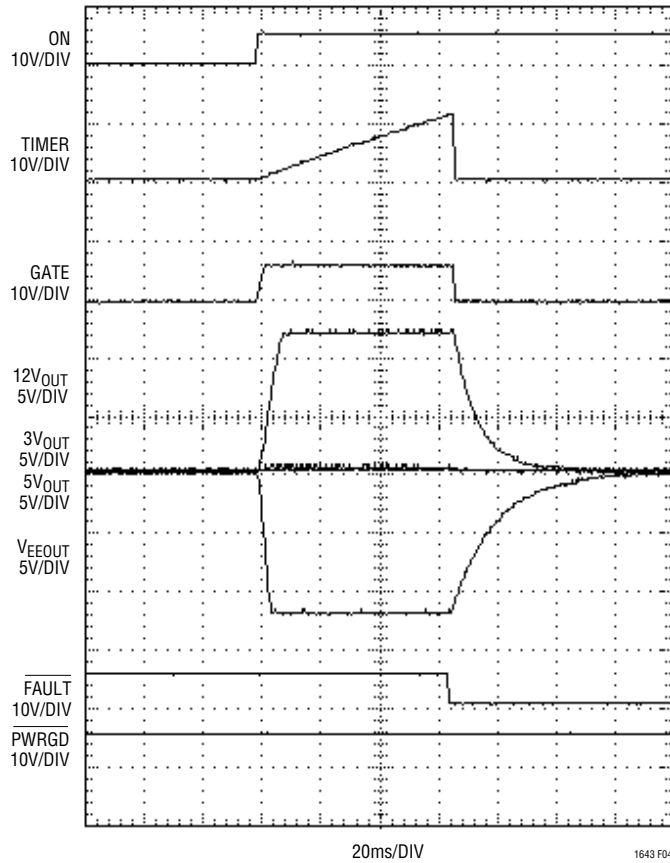


Figure 4. Power-Up into a Short on 3.3V Output

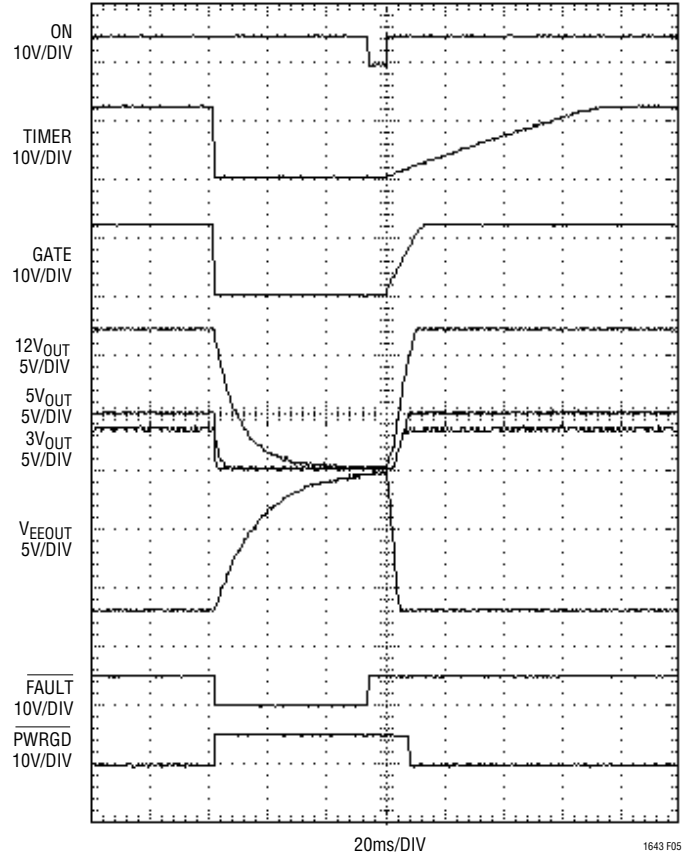


Figure 5. Short Circuit on 5V Followed by Circuit Breaker Reset

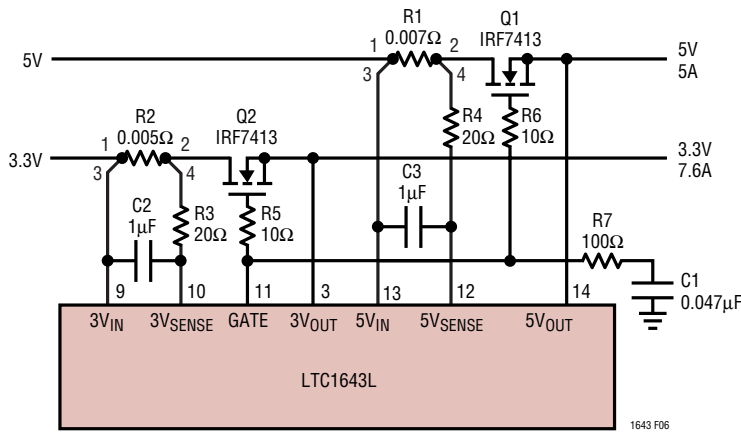


Figure 6. Delay in the Current Limit Loop

## APPLICATIONS INFORMATION

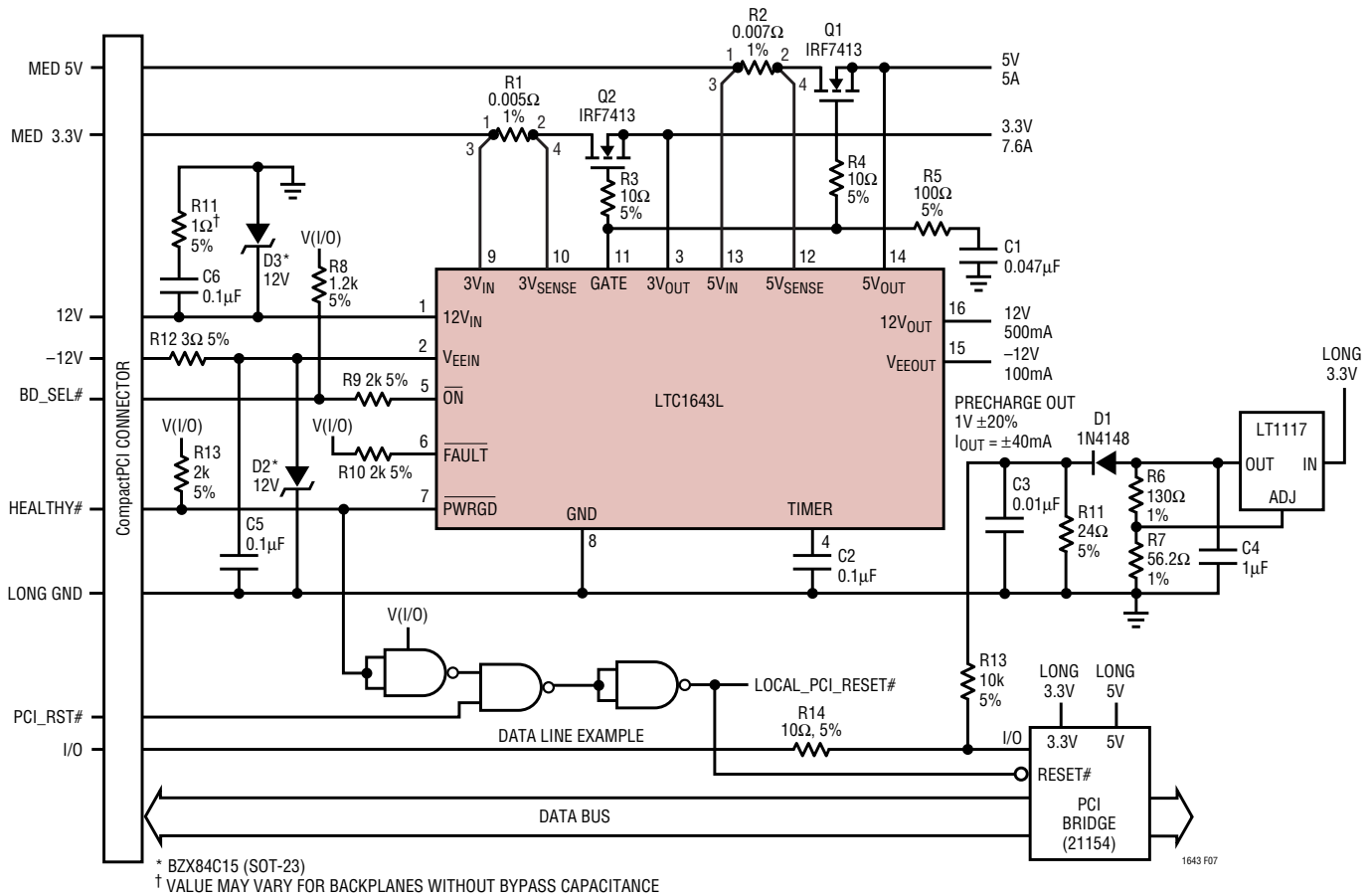


Figure 7. Typical CompactPCI Application

circuit, PCI bridge chip and the LOCAL\_PCI\_RESET# logic circuitry. The BD\_SEL# signal is connected to the ON pin while the PWRGD pin is connected to the HEALTHY# signal. The HEALTHY# signal is combined with the PCI\_RESET# signal to generate the LOCAL\_PCI\_RESET# signal. Capacitors C6 and C7 provide chip bypassing on the 12V and -12V inputs. Diode D2 protects the part from voltage surges below -13.2V on the -12V supply.

The 1V precharge voltage for the data bus lines is generated by an LT1117 low dropout regulator. The output of the LT1117 is set to 1.8V, then the voltage is dropped by a 1N4148 diode to generate 1V. The precharge circuit is capable of sourcing and sinking 40mA.

## LTC1643L-1

The LTC1643L-1 is designed for CompactPCI designs where the  $\pm 12V$  supplies are not being used on the board or the supplies are not well regulated. The power good comparators on the 12V<sub>OUT</sub> and V<sub>EE</sub>OUT pins are disabled. The V<sub>EE</sub>IN pin can be connected to GND and the part will still operate normally if a -12V<sub>OUT</sub> output is not needed. However, 12V is still required at the 12V<sub>IN</sub> pin for the part to function. Refer to Figure 10 for a typical LTC1643L-1 application circuit.

## Increasing 12V and -12V Current Capability

The internal switches in the LTC1643 are designed for up to 500mA loads on 12V and 200mA on -12V. If more current is needed, then the circuits in Figure 8 can be used.

## APPLICATIONS INFORMATION

For the 12V supply, P-channel transistor Q4 is placed in parallel with the internal switch. When the LTC1643H is turned off, the GATE pin is held low and transistor Q3 is turned on which pulls the gate of Q4 high, turning it off. When the LTC1643H is turned on, the GATE pin goes high, turning off Q3 and allowing R8 to pull the gate of Q4 low to turn it on.

Because Q4 is in parallel with the internal 12V switch, the load current will be shared in proportion to their respective  $R_{DS(ON)}$  values. For example, if the  $R_{DS(ON)}$  of the external switch is  $0.2\Omega$  and the internal switch is  $0.4\Omega$ , then, at 1.5A load current, the external switch will provide 1A and the internal switch 500mA. The circuit breaker current will be reached when the internal current reaches 1A and the external current is 2A or 3A load current.

For the  $-12V$  supply, N-channel transistor Q6 is used to provide the extra load current. When the LTC1643H is turned off, the internal  $V_{EE}$  switch is turned on and the  $-12V$  output starts to pull down through D1 and turns on Q5. When Q5 turns on, the gate of Q6 starts to rise, turning it on. When the LTC1643H turns off, the  $V_{EEOUT}$  pin is pulled up to ground, diode D1 is reversed biased, and transistor Q5 turns off, which allows resistor R10 to turn off Q6.

The internal  $-12V$  switch provides the current limit for the supply, but because the high  $R_{DS(ON)}$  of the internal switch ( $1.2\Omega$ ) is in series with D1, very large currents can flow through Q6 before the circuit breaker trips. However, if a short to ground occurs on the  $-12V$  output, diode D1 will prevent Q5 from turning on, which will prevent Q6 from turning on.

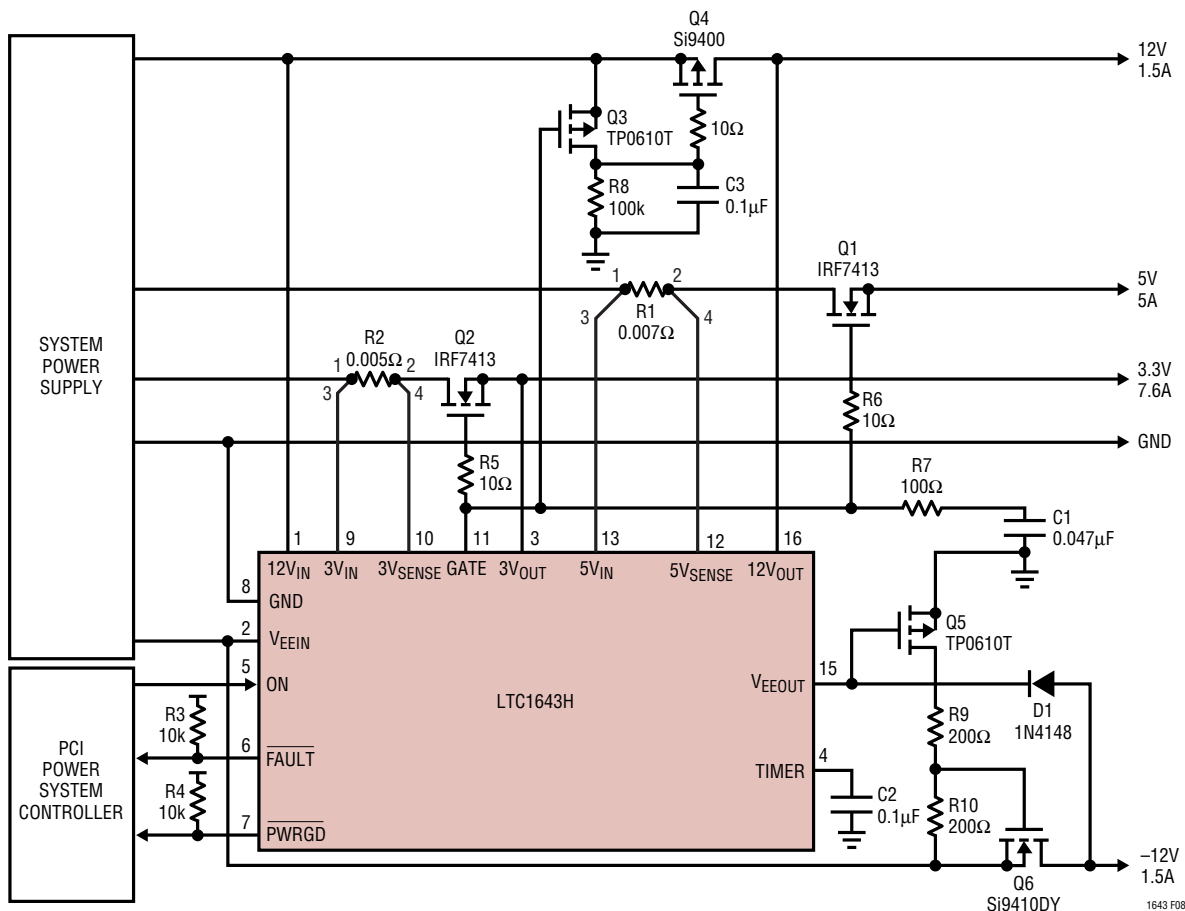
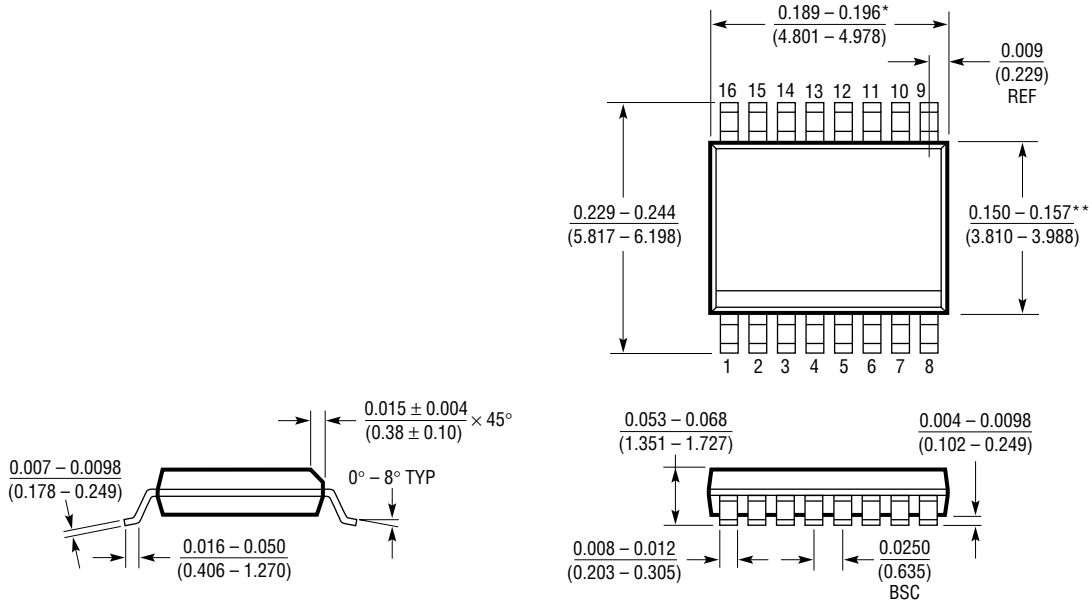


Figure 8. Increasing 12V and  $-12V$  Current Capability

## PACKAGE DESCRIPTION

**GN Package**  
**16-Lead Plastic SSOP (Narrow .150 Inch)**  
 (Reference LTC DWG # 05-08-1641)



\* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE  
 \*\* DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN16 (SSOP) 1098

## TYPICAL APPLICATIONS

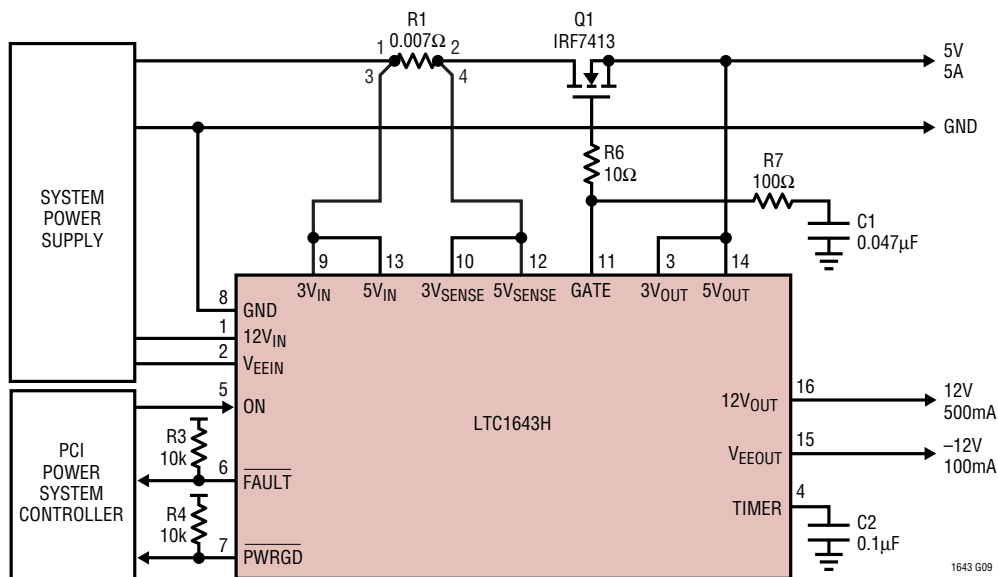


Figure 9. System Without 3.3V Supply



