HARRIS

HI-518/883

8 Channel/Differential 4 Channel CMOS High Speed Analog Multiplexer

July 1987

Features

- **This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Access Time (Max. Over Temp.) 225ns**
- **Low Leakage (Max. Over Temp.) ..... $I_{D(OFF)}$ 50nA**
- **Low Charge Transfer Error (100pF Load) 25mV**
- **Single Ended to Differential Selectable (SDS)**
- **TTL/CMOS Compatible**

Applications

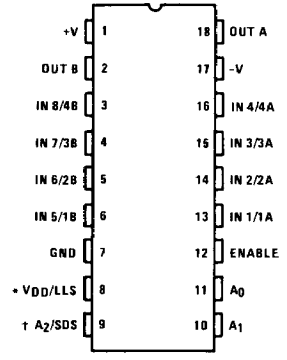
- **Data Acquisition Systems**
- **Telemetry**
- **Industrial Control**

Description

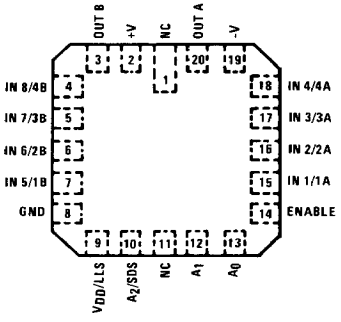
The HI-518/883 is a monolithic dielectrically isolated, high speed, high performance CMOS analog multiplexer. It offers unique built-in channel selection decoding plus an inhibit input for disabling all channels. The dual function of address input A_2 enables the HI-518/883 to be user programmed either as a single ended 8-channel multiplexer by connecting 'OUT A' to 'OUT B' and using A_2 as a digital address input, or as a 4-channel differential multiplexer by connecting A_2 to the $-V_{SUPPLY}$. The substrate leakages and parasitic capacitances are reduced substantially by using the Harris dielectric isolation process to achieve optimum performance in both high and low level signal applications. The low output leakage current ($I_{D(OFF)} < 50nA$ over temperature) of the device makes it an ideal choice for high speed data acquisition systems, precision instrumentation, and industrial process control.

Pinouts

HI1-518/883 (CERAMIC DIP)
TOP VIEW



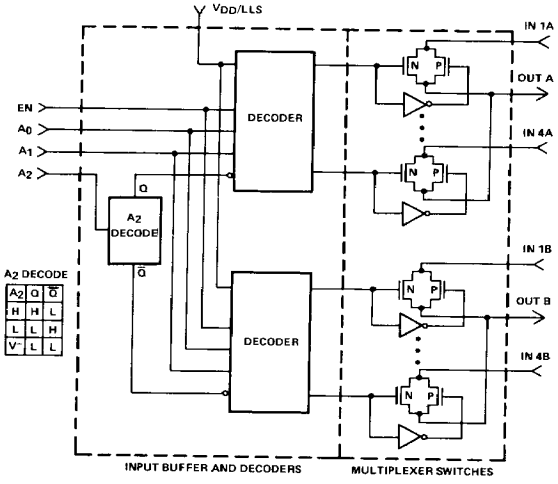
HI4-518/883 (CERAMIC LCC)
TOP VIEW



* LLS = Logic Level Select (TTL Compatible with V_{DD}/LLS Pin = Ground or Open, CMOS Compatible when V_{DD}/LLS Pin = V_{DD})

† SDS = Single Ended/Differential Select (Multiplexer is in Differential Mode when A_2/SDS Pin = $-V_{SUPPLY}$)

Functional Diagram



Truth Tables

HI-518/883 USED AS 8 CHANNEL MULTIPLEXER

USE A_2/SDS AS DIGITAL ADDRESS INPUT				ON CHANNEL TO	
ENABLE	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	None	None
H	L	L	L	1A	None
H	L	L	H	2A	None
H	L	H	L	3A	None
H	L	H	H	4A	None
H	H	L	L	None	1B
H	H	L	H	None	2B
H	H	H	L	None	3B
H	H	H	H	None	4B

HI-518/883 USED AS DIFFERENTIAL 4 CHANNEL MULTIPLEXER

A_2/SDS CONNECTED TO -V_{SUPPLY}			ON CHANNEL TO	
ENABLE	A_1	A_0	OUT A	OUT B
L	X	X	None	None
H	L	L	1A	1B
H	L	H	2A	2B
H	H	L	3A	3B
H	H	H	4A	4B

Absolute Maximum Ratings

Voltage Between Supply Pins 33V
$+V_{SUPPLY}$ to Ground 16.5V
$-V_{SUPPLY}$ to Ground 16.5V
Analog Input Voltage
  $+V_S$ ..... $+V_{SUPPLY}$ +2V
  $-V_S$ ..... $-V_{SUPPLY}$ -2V
Digital Input Voltage
  TTL Levels Selected (V_{DD}/LLS Pin = GND or Open)
    $+V_A$ ..... +6V
    $-V_A$ ..... -6V
    A_2/SDS ..... $-V_{SUPPLY}$ -2V
    A_2/SDS ..... $+V_{SUPPLY}$ +2V
  CMOS Levels Selected (V_{DD}/LLS Pin = V_{DD})
    $+V_A$ ..... $+V_{SUPPLY}$ +2V
    $-V_A$ ..... -2V
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10 Seconds) ..... 275°C
Junction Temperature ..... +175°C
Thermal Resistance, Junction-to-Case (θjc)
  Ceramic DIP Package ..... 25°C/W
  Ceramic LCC Package ..... 21°C/W
Thermal Resistance, Junction-to-Ambient (θja)
  Ceramic DIP Package ..... 84°C/W
  Ceramic LCC Package ..... 78°C/W
Power Dissipation (at 75°C)
  Ceramic DIP Package 1.19W
  Ceramic LCC Package 1.28W
Power Dissipation Derating Factor (Above +75°C)
  Ceramic DIP Package ..... 11.9mW/°C
  Ceramic LCC Package ..... 12.8mW/°C
ESD Classification ..... ≤2000V

Recommended Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Supply Voltage ($\pm V_{SUPPLY}$) ..... ±15V
Analog Input Voltage (V_S) ..... ±14V
Logic Level Low (V_{AL}) ..... 0V to 0.8V
Logic Level High (V_{AH}) ..... 2.4V to $+V_{SUPPLY}$
Max RMS Current, S or D 8mA

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, V_{EN} = 2.4V, V_{DD}/LLS = GND, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Leakage Current	I_{IH}	Measure Inputs Sequentially, Connect All Unused Inputs to GND	1, 2, 3	+25°C, +125°C -55°C	-1.0	1.0	µA
	I_{IL}	Measure Inputs Sequentially, Connect All Unused Inputs to +5V	1, 2, 3	+25°C, +125°C -55°C	-20	20	µA
Leakage Current Into the Source Terminal of an "OFF" Switch	$^+I_{S(OFF)}$	V_S = 10V, V_D = -10V, V_{EN} = 0.8V All Unused Inputs = -10V	1, 2, 3	+25°C, +125°C, -55°C	-50	+50	nA
	$^-I_{S(OFF)}$	V_S = -10V, V_D = 10V, V_{EN} = 0.8V All Unused Inputs = +10V	1, 2, 3	+25°C, +125°C, -55°C	-50	+50	nA
Leakage Current Into the Drain Terminal of an "OFF" Switch	$^+I_{D(OFF)}$	V_S = -10V, V_D = +10V, V_{EN} = 0.8V All Unused Inputs = -10V	1, 2, 3	+25°C, +125°C, -55°C	-50	+50	nA
	$^-I_{D(OFF)}$	V_S = +10V, V_D = -10V, V_{EN} = 0.8V All Unused Inputs = +10V	1, 2, 3	+25°C, +125°C, -55°C	-50	+50	nA
Leakage Current From an "ON" Driver Into the Switch (Drain)	$^+I_{D(ON)}$	V_S = V_D = 10V All Unused Inputs = -10V	1, 2, 3	+25°C, +125°C, -55°C	-50	+50	nA
	$^-I_{D(ON)}$	V_S = V_D = -10V All Unused Inputs = +10V	1, 2, 3	+25°C, +125°C -55°C	-50	+50	nA
Positive Supply Current	I(+)	V_S = 0V, V_D = Open, V_{EN} = 2.4V Sequence All Address Combinations, Record Highest I+	1, 2, 3	+25°C, +125°C, -55°C	—	+15	mA
Negative Supply Current	I(-)	V_S = 0V, V_D = Open, V_{EN} = 2.4V Sequence All Address Combinations, Record Highest I-	1, 2, 3	+25°C, +125°C, -55°C	—	+15	mA
Standby Positive Supply Current	$^+I_{SBY}$	V_A = 0.8V, V_{EN} = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-15	—	mA
Standby Negative Supply Current	$^-I_{SBY}$	V_A = 0.8V, V_{EN} = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-15	—	mA
Switch "ON" Resistance	$^+R_{DS1}$	V_S = 10V I_D = 100µA	1	+25°C	—	750	Ω
			2, 3	+125°C, -55°C	—	1000	Ω
	$^-R_{DS1}$	V_S = -10V I_D = -100µA	1	+25°C	—	750	Ω
			2, 3	+125°C, -55°C	—	1000	Ω
Logic Level Voltage	V_{AL} (TTL)	V_{DD}/LLS = GND	1, 2, 3	+25°C, +125°C, -55°C	—	0.8	V
	V_{AH} (TTL)	V_{DD}/LLS = GND	1, 2, 3	+25°C, +125°C -55°C	2.4	—	V
	V_{AL} (CMOS)	V_{DD}/LLS = +15V	1, 2, 3	+25°C, +125°C -55°C	—	4.5	V
	V_{AH} (CMOS)	V_{DD}/LLS = +15V	1, 2, 3	+25°C, +125°C, -55°C	10.5	—	V

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, V_{EN} = 2.4V, V_{DD}/LLS = GND, Unless Otherwise Specified.

A.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMP	LIMITS MIN	LIMITS MAX	UNITS
Break-Before-Make Time Delay	t_D	R_L = 800Ω, C_L = 12.5pF	9	+25°C	10	—	ns
			10	+125°C	2	—	ns
Propagation Delay Times: Address Inputs to I/O Channel Times	t_A	R_L = 10MΩ, C_L = 12.5pF	9	+25°C	—	175	ns
			10, 11	+125°C, -55°C	—	225	ns
Enable to I/O	$t_{ON(EN)}$	R_L = 800Ω, C_L = 12.5pF	9	+25°C	—	175	ns
			10, 11	+125°C, -55°C	—	225	ns
	$t_{OFF(EN)}$	R_L = 800Ω, C_L = 12.5pF	9	+25°C	—	175	ns
			10, 11	+125°C, -55°C	—	225	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Characterized at $+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V, V_{EN} = 2.4V, V_{DD}/LLS = GND, Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMP	LIMITS MIN	LIMITS MAX	UNITS
Capacitance: Address Input	C_A	V+ = V- = 0V f = 1MHz	1	+25°C	—	5.0	pF
Capacitance: Output Switch	C_{OS}	V+ = V- = 0V f = 1MHz	1	+25°C	—	10	pF
Capacitance: Input Switch	C_{IS}	V+ = V- = 0V f = 1MHz	1	+25°C	—	5.0	pF
Charge Transfer Error	V_{CTE}	V_S = GND, C_L = 100pF V_{GEN} = 0V to 5V	1	+25°C	—	25	mV
Off Channel Isolation	V_{ISO}	V_{EN} = 0.8V, R_L = 1kΩ C_L = 40pF, V_S = $3V_{RMS}$ f = 500kHz	1	+25°C	-45	—	dB
Break-Before-Make Time Delay	t_D	R_L = 800Ω, C_L = 12.5pF	1	-55°C	2	—	ns

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1, 2 & 3)
Interim Electrical Parameters (Pre-Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

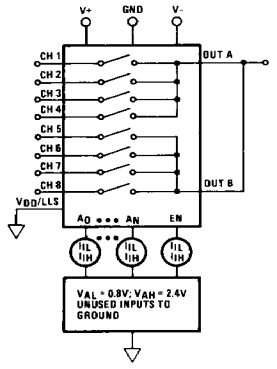
*PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

NOTE 1. The parameters listed in this table are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

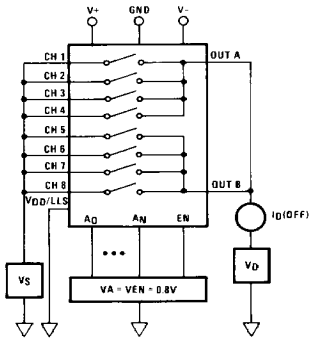
CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Test Circuits

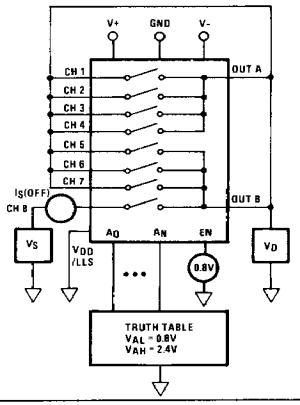
INPUT LEAKAGE CURRENT



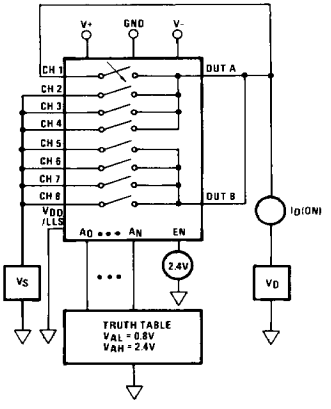
$I_{D(OFF)}$



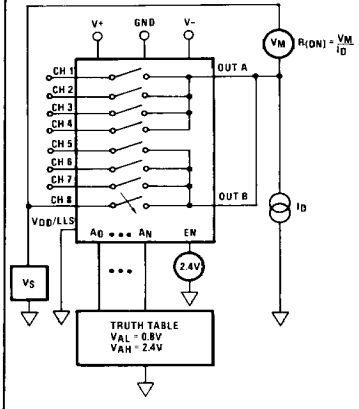
$I_{S(OFF)}$



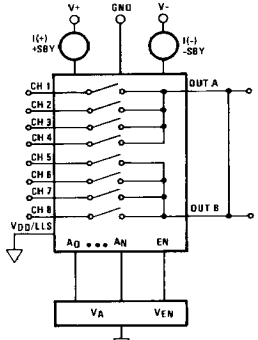
$I_{D(ON)}$



R_{DS}



SUPPLY CURRENTS

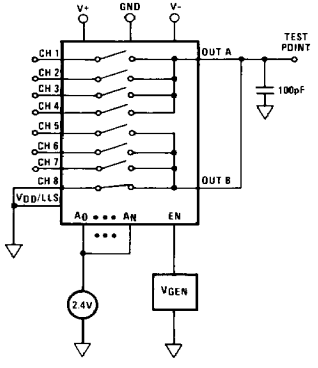


SBY: V_A, V_{EN} = 0.8V

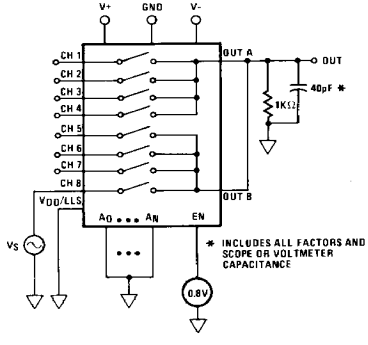
OPERATIONAL: V_{EN} = 2.4V,

V_A = All Combinations are Sequenced

CHARGE TRANSFER ERROR

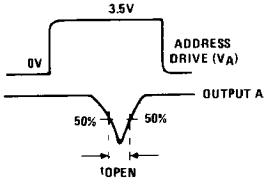


OFF CHANNEL ISOLATION

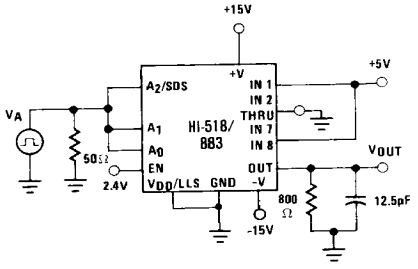


Switching Waveforms

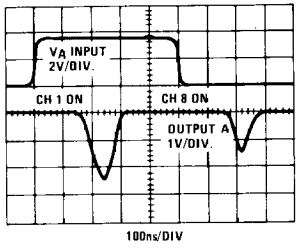
ADDRESS DRIVE



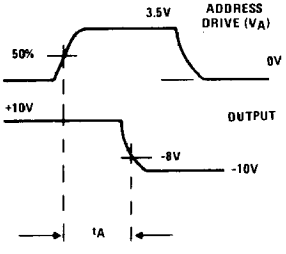
BREAK-BEFORE-MAKE DELAY (t_{OPEN})



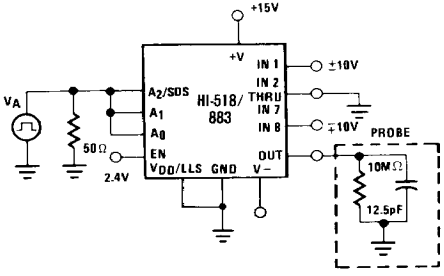
BREAK-BEFORE-MAKE DELAY (t_{OPEN})



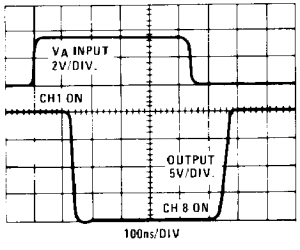
ACCESS TIME



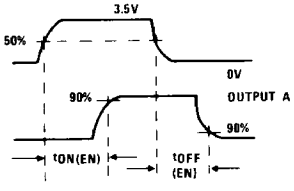
ACCESS TIME



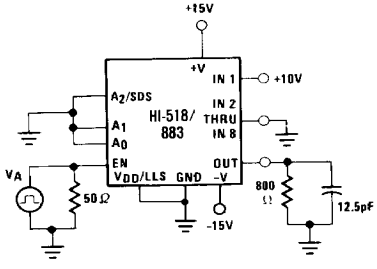
ACCESS TIME



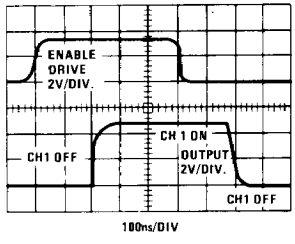
ENABLE DRIVE



ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$

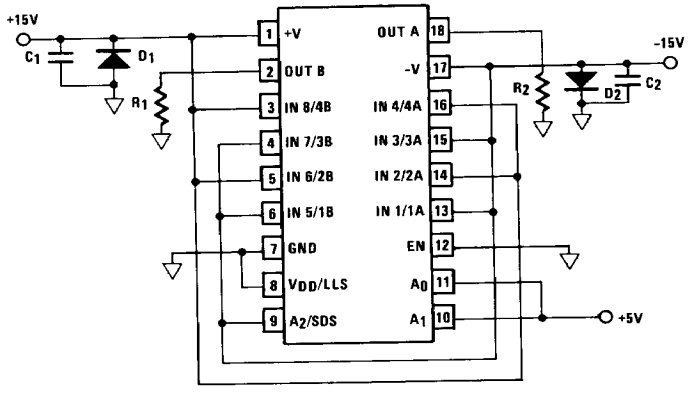


ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$



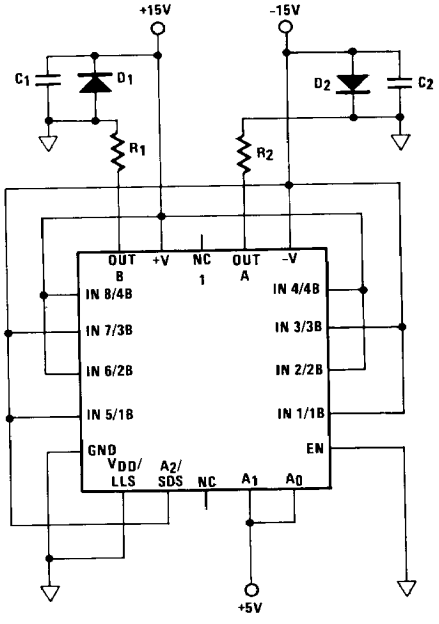
Burn-In Circuits

HI-518/883 CERAMIC DIP



NOTES:
$R_1 = R_2 = 10k\Omega$, ±5%, 1/4 or 1/2W
$C_1 = C_2 = 0.01\mu F$ (one per socket) or $0.1\mu F$ (one per row)
$D_1 = D_2$ = IN4002 or equivalent (per board)

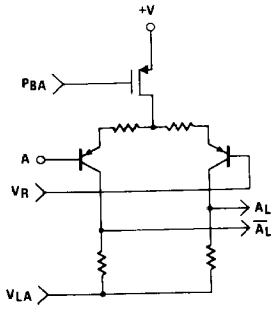
HI-518/883 CERAMIC LCC



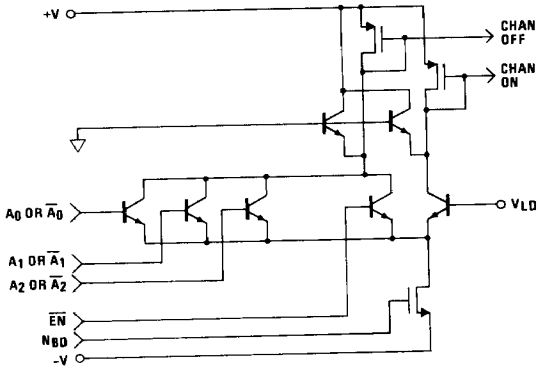
NOTES:
$R_1 = R_2 = 10k\Omega$, ±5%, 1/2 or 1/4W (per socket)
$C_1 = C_2 = 0.01\mu F$ (one per socket) or $0.1\mu F$ (one per row)
$D_1 = D_2$ = IN4002 or equivalent (per board)

Schematic Diagrams

ADDRESS/ENABLE INPUT BUFFER

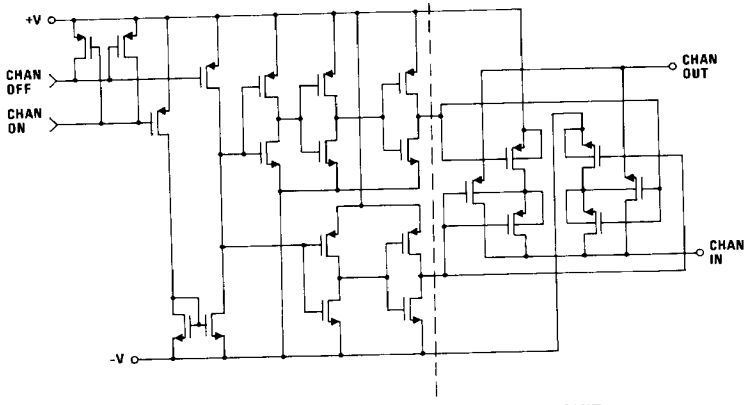


DECODE

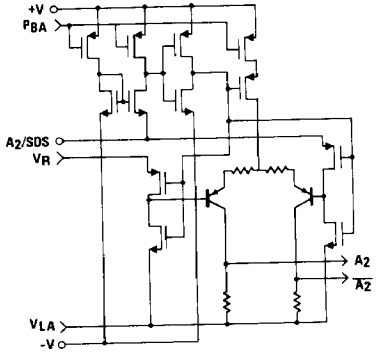


LEVEL SHIFTER

SWITCH

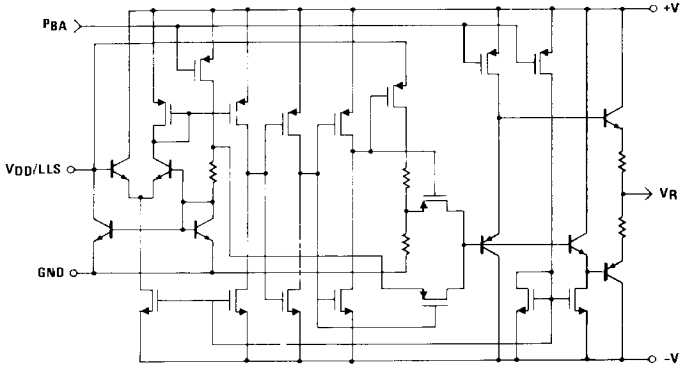


A_2-SINGLE ENDED/DIFFERENTIAL SELECT CIRCUIT

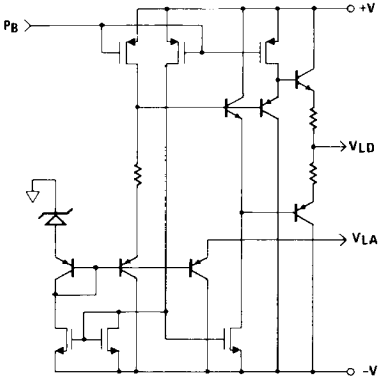


Schematic Diagrams (Continued)

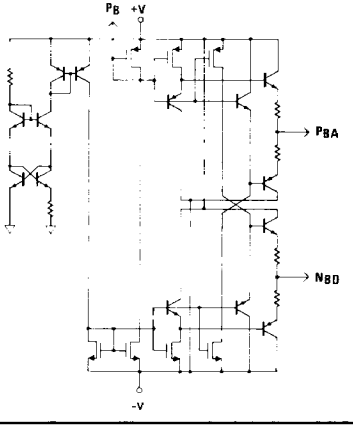
LOGIC LEVEL SELECT CIRCUIT



REFERENCE VOLTAGES



BIAS



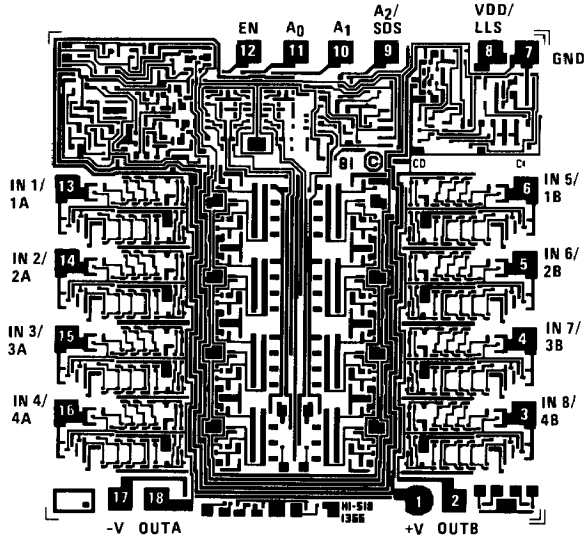
Die Characteristics

DIE DIMENSIONS: 89 x 93 x 19 mils
METALLIZATION:
Type: Al
Thickness: 16kÅ ± 2kÅ
GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 1.0kÅ
WORST CASE CURRENT DENSITY: $2 \times 10^5 A/cm^2$

TRANSISTOR COUNT:
HI-518/883 356
PROCESS: CMOS DI
DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP - 460° (Max)
Ceramic LCC - 420° (Max)

Metallization Mask Layout

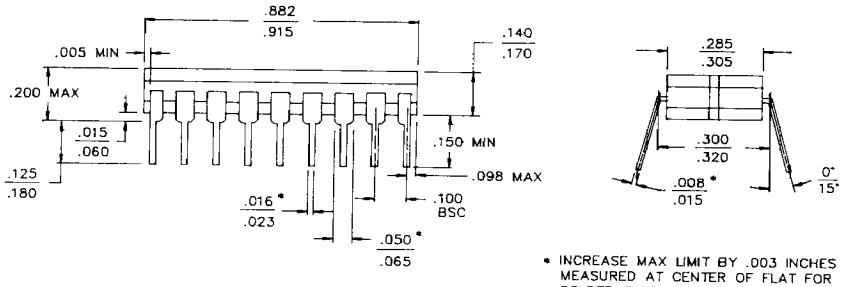
HI-518/883



NOTE: Pad Numbers Correspond to DIP Pin Numbers Only.

Packaging †

18 PIN CERAMIC DIP

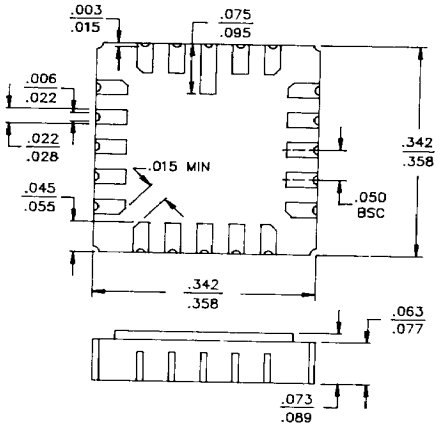


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ±10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-6

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ±10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$ Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.