HI-508/509

Single 8/Differential 4 Channel CMOS Analog Multiplexers

Features

- Low On Resistance (Typ) 180Ω
- Wide Analog Signal Range ..... ±15V
- TTL/CMOS Compatible ..... 2.4V (Logic "1")
- Fast Access 250ns
- Fast Settling (0.01%) 600ns
- 44V Maximum Power Supply
- Break-Before-Make Switching
- No Latch-Up
- Replaces DG508A/DG508AA and DG509A/DG509AA

Applications

- Data Acquisition Systems
- Precision Instrumentation
- Demultiplexing
- Selector Switch

Description

These monolithic CMOS multiplexers each include an array of eight analog switches, a digital decode circuit for channel selection, a voltage reference for logic thresholds, and an ENABLE input for device selection when several multiplexers are present.

The Dielectric Isolation (DI) process used in fabrication of these devices eliminates the problem of latch-up. Also, DI offers much lower substrate leakage and parasitic capacitance than conventional junction-isolated CMOS (see Application Note 521). Combined with the low ON resistance (180Ω typical), these benefits allow low static error, fast channel switching rates, and fast settling.

Switches are guaranteed to break-before-make, so that two channels are never shorted together.

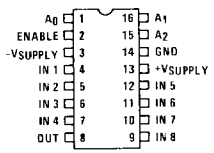
The switching threshold for each digital input is established by an internal +5V reference, providing a guaranteed minimum 2.4V for "1" and maximum 0.8V for "0". This allows direct interface without pull-up resistors to signals from most logic families: CMOS, TTL, DTL and some PMOS. For protection against transient overvoltage, the digital inputs include a series 200Ω resistor and a diode clamp to each supply.

The HI-508 is an eight channel single-ended multiplexer, and the HI-509 is a four channel differential version. Each device is available in a 16 pin Plastic or Ceramic DIP, a 20 pin Plastic Leaded Chip Carrier (PLCC) or 20 pad Ceramic Leadless Chip Carrier (LCC). If input overvoltage protection is needed, the HI-548/549 multiplexers are recommended.

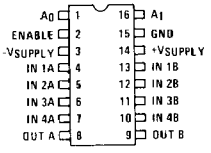
The HI-508/509 is offered in both commercial and military grades, suitable for spacecraft/military applications. For additional Hi-Rel screening including 160 hour burn-in, specify the "-8" suffix. For further information see Application Notes 520 and 521. For MIL-STD-883 compliant parts, request the HI-508/883 or HI-509/883 data sheets.

Pinouts

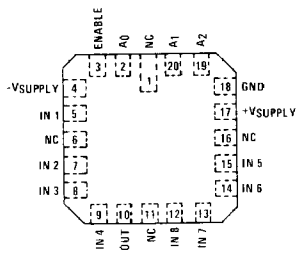
HI1-508 (CERAMIC DIP)
HI3-508 (PLASTIC DIP)
TOP VIEW



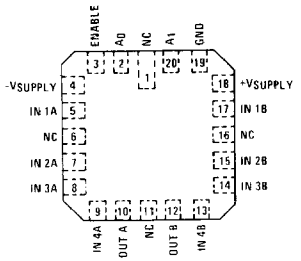
HI1-509 (CERAMIC DIP)
HI3-509 (PLASTIC DIP)
TOP VIEW



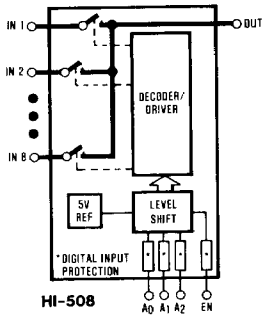
HI4-508 (CERAMIC LCC)
HI4P508 (PLCC)
TOP VIEW



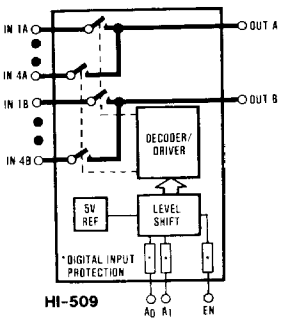
HI4-509 (CERAMIC LCC)
HI4P509 (PLCC)
TOP VIEW



Functional Diagrams



HI-508



HI-509

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

$V_{SUPPLY(+)}$ to $V_{SUPPLY(-)}$ 44V
$V_{SUPPLY(+)}$ to GND 22V
$V_{SUPPLY(-)}$ to GND 25V
Digital Input Overvoltage
$+V_{EN}$, $+V_A$ ..... $+V_{SUPPLY}$ +4V
$-V_{EN}$, $-V_A$ ..... $-V_{SUPPLY}$ -4V
or 20mA, whichever occurs first
Analog Signal Overvoltage (Note 7)
$+V_S$ ..... $+V_{SUPPLY}$ +2V
$-V_S$ ..... $-V_{SUPPLY}$ -2V
Continuous Current, S or D: 20mA
Peak Current, S or D
(Pulsed at 1ms, 10% duty cycle max): 40mA
Junction Temperature ..... +175°C
Operating Temperature Ranges:
HI-508/509-2, -8 ..... -55°C to +125°C
HI-508/509-4 ..... -25°C to +85°C
HI-508/509-5 ..... 0°C to +75°C
Storage Temperature Range ..... -65°C to +150°C

Electrical Specifications Unless Otherwise Specified:

Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V;
V_{AL} (Logic Level Low) = +0.8V. For Test Conditions, consult Performance Characteristics Section.

PARAMETER	TEMP.	HI-508/HI-509 -2, -8 MIN.	TYP.	MAX.	HI-508/509 -4, -5 MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
*R_{ON}, On Resistance (Note 2)	+25°C		180	300		180	400	Ω
	Full			400			500	Ω
ΔR_{ON}, Any Two Channels	+25°C		5			5		%
*I_S (OFF), Off Input Leakage Current (Note 3)	+25°C		0.03			0.03		nA
	Full			50			50	nA
*I_D (OFF), Off Output Leakage Current (Note 3)	+25°C		0.3			0.3		nA
HI-508	Full			200			200	nA
HI-509	Full			100			100	nA
*I_D (ON), On Channel Leakage Current (Note 3)	+25°C		0.3			0.3		nA
HI-508	Full			200			200	nA
HI-509	Full			100			100	nA
*I_{DIFF}, Differential Off Output Leakage Current (HI-509 Only)	Full			50			50	nA
DIGITAL INPUT CHARACTERISTICS								
*V_{AL}, Input Low Threshold	Full			0.8			0.8	V
*V_{AH}, Input High Threshold	Full	2.4			2.4			V
*I_A, Input Leakage Current (High or Low) (Note 4)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
*t_A, Access Time	+25°C		250	500		250		ns
	Full			1000			1000	ns
*t_{OPEN}, Break-Before-Make Interval	+25°C	25	80		25	80		ns
*t_{ON} (EN), Enable Turn-On	+25°C		250	500		250		ns
	Full			1000			1000	ns
*t_{OFF} (EN), Enable Turn-Off	+25°C		250	500		250		ns
	Full			1000			1000	ns
t_S, Settling Time to 0.1%	+25°C		360			360		ns
to 0.01%	+25°C		600			600		ns
"Off Isolation" (Note 5)	+25°C	50	68		50	68		dB
C_S (OFF), Channel Input Capacitance	+25°C		5			5		pF
C_D (OFF), Channel Output Capacitance HI-508	+25°C		22			22		pF
HI-509	+25°C		11			11		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
C_{DS} (OFF), Input to Output Capacitance	+25°C		.08			.08		pF
POWER REQUIREMENTS								
*I+, Positive Supply Current (Note 6)	Full		1.5	2.4		1.5	2.4	mA
*I-, Negative Supply Current (Note 6))	Full		0.4	1		0.4	1	mA
P_D, Power Dissipation	Full			51			51	mW

*100% tested for Dash 8. Leakage currents not tested at -55°C.

TRUTH TABLES

HI-508

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-509

A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

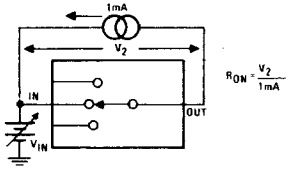
NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{OUT} = ±10V, I_{OUT} = -1mA.
3. Ten nanoamps is the practical lower limit for high speed measurement in the production test environment.
4. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1nA at 25°C.
5. V_{EN} = 0.8V, R_L = 1K, C_L = 15pF, V_S = 7V_{RMS}, f = 100kHz. Worst case isolation occurs on channel 4 due to proximity of the output pins.
6. V_{EN}, V_A = 0V or 2.4V.
7. Signal voltage at any analog input or output (S or D) will be clamped to the supply rail by internal diodes. Limit the resulting current as shown under absolute maximum ratings. If an overvoltage condition is anticipated (analog input exceeds either power supply voltage), the Harris HI-548/549 multiplexers are recommended.

Performance Characteristics and Test Circuits

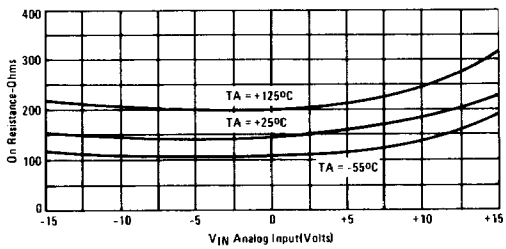
Unless Otherwise Specified; T_A = 25°C, V_{Supply} = ±15 V, V_{AH} = 2.4 V, V_{AL} = 0.8 V.

TEST CIRCUIT NO. 1

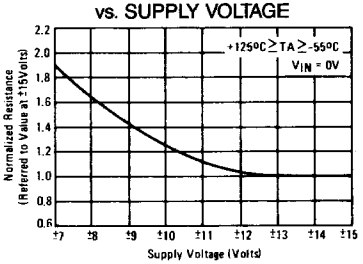
ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE



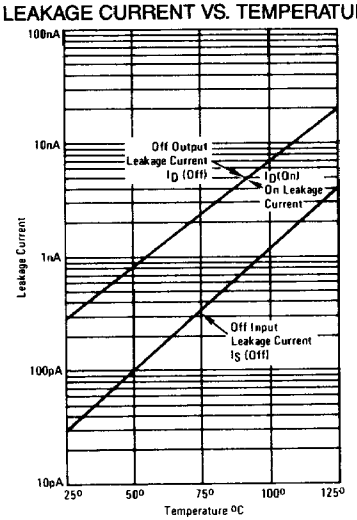
ON RESISTANCE vs. ANALOG INPUT VOLTAGE, TEMPERATURE



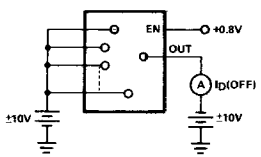
NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE



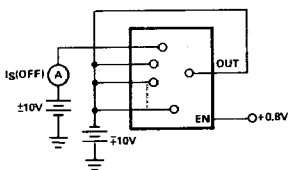
LEAKAGE CURRENT VS. TEMPERATURE



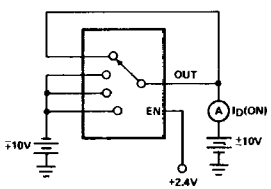
TEST CIRCUIT NO. 2*



TEST CIRCUIT NO. 4*

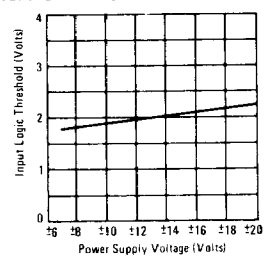


TEST CIRCUIT NO. 3*

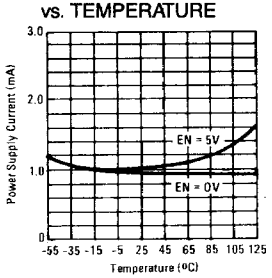


***Two measurements per channel: +10 V/−10 V and −10 V/+10 V. (Two measurements per device for ID(OFF): +10 V/−10 V and −10 V/+10 V.)**

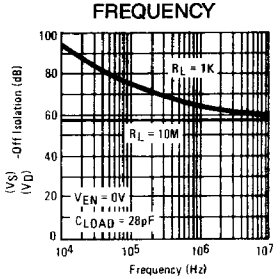
LOGIC THRESHOLD vs. POWER SUPPLY VOLTAGE



POWER SUPPLY CURRENT vs. TEMPERATURE

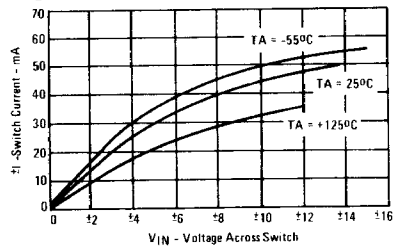


OFF ISOLATION vs. FREQUENCY



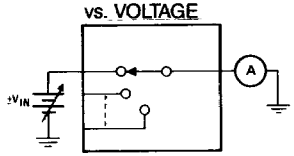
Performance Characteristics and Test Circuits (continued)

ON CHANNEL CURRENT vs. VOLTAGE

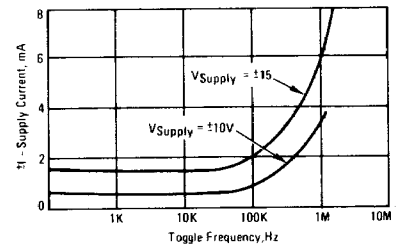


TEST CIRCUIT NO. 5

ON CHANNEL CURRENT vs. VOLTAGE

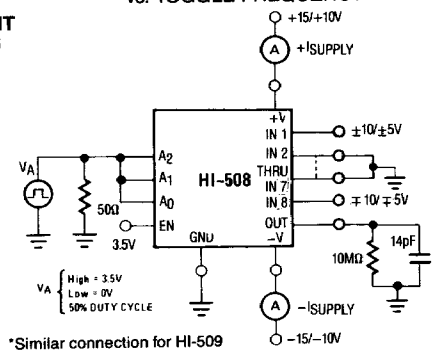


SUPPLY CURRENT vs. TOGGLE FREQUENCY



TEST CIRCUIT NO. 6

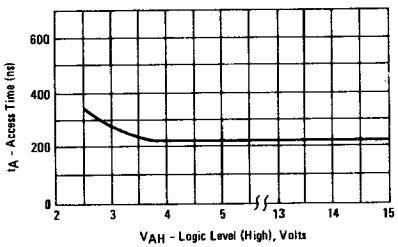
SUPPLY CURRENT vs. TOGGLE FREQUENCY



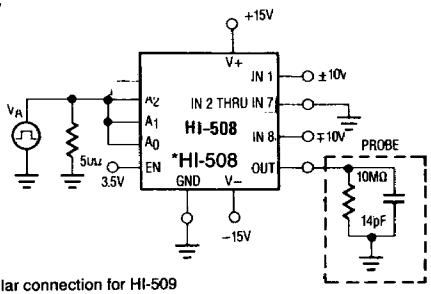
*Similar connection for HI-509

TEST CIRCUIT NO. 7

ACCESS TIME vs. LOGIC LEVEL (HIGH)

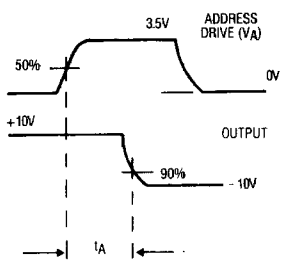


ACCESS TIME vs. LOGIC LEVEL (HIGH)

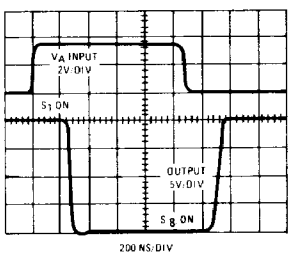


*Similar connection for HI-509

Switching Wav



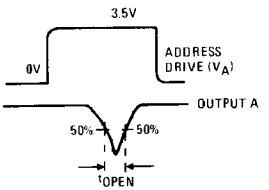
ACCESS TIME



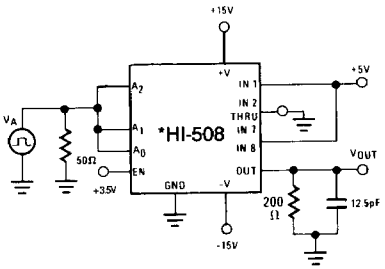
Switching Waveforms (continued)

TEST CIRCUIT NO. 8

ADDRESS DRIVE

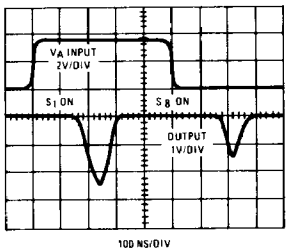


BREAK-BEFORE-MAKE DELAY (tOPEN)



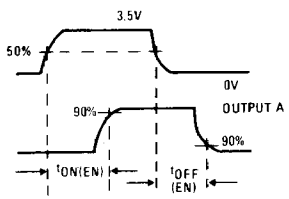
*Similar connection for HI-509

BREAK-BEFORE-MAKE DELAY(tOPEN)

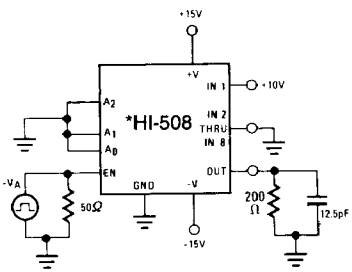


TEST CIRCUIT NO. 9

ENABLE DRIVE

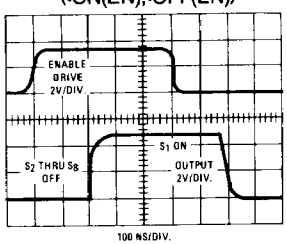


ENABLE DELAY (tON(EN),tOFF(EN))



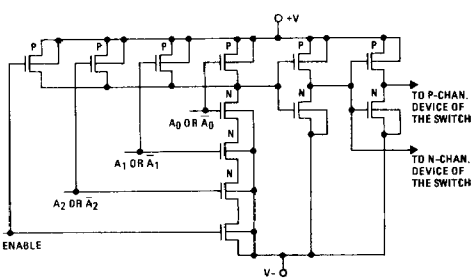
*Similar connection for HI-509

ENABLE DELAY (tON(EN),tOFF(EN))

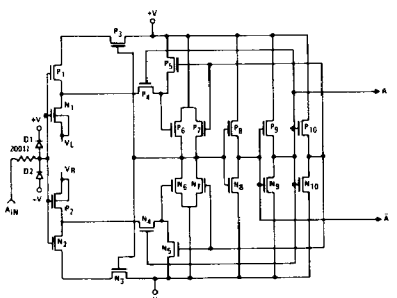


Schematic Diagrams

ADDRESS DECODER



ADDRESS INPUT BUFFER LEVER SHIFTER

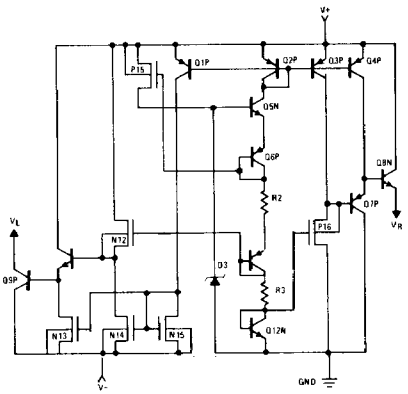


Delete A_2 or $\bar{A}_2$ Input for HI-509

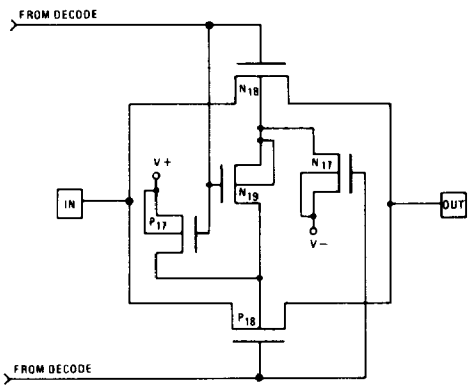
All N-Channel Bodies to V−
All P-Channel Bodies to V+ Unless Otherwise Indicated

Schematic Diagrams (continued)

TTL REFERENCE CIRCUIT

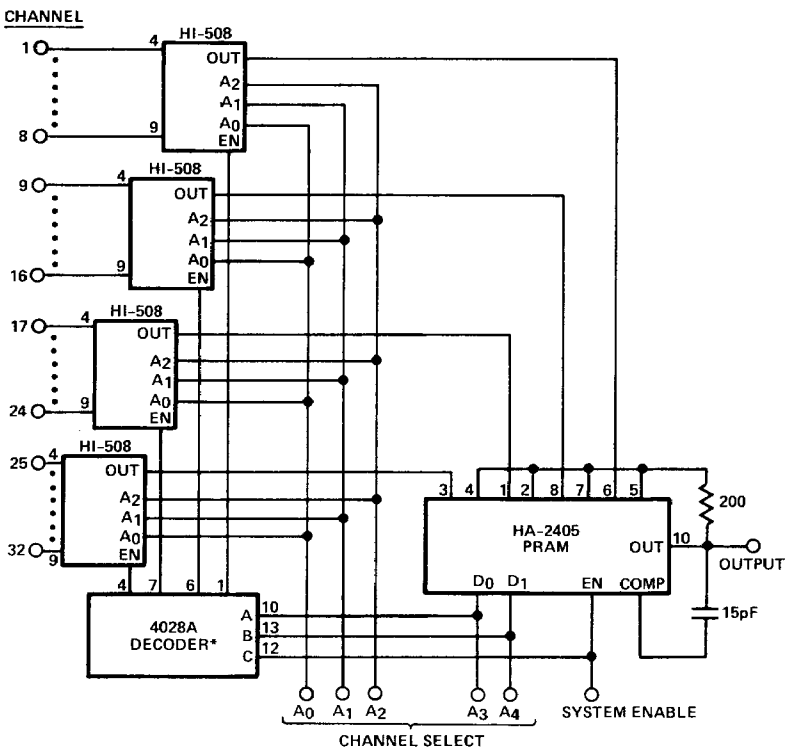


MULTIPLEX SWITCH



Applications

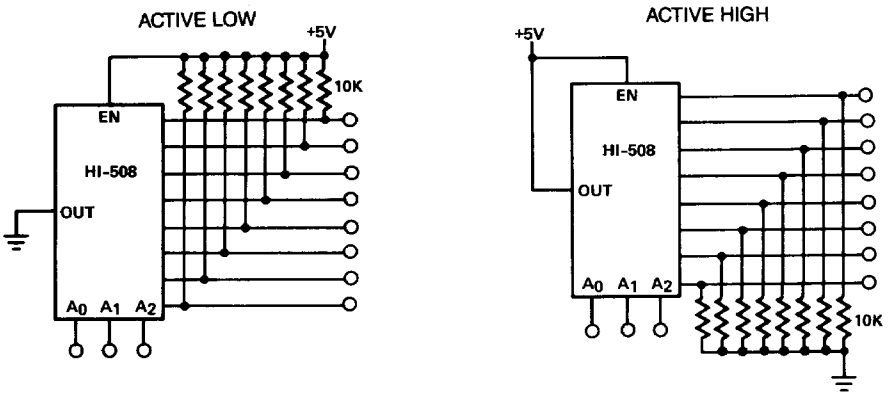
32 CHANNEL BUFFERED MULTIPLEXER *HI-508



*Optional; Provides Greater Isolation for AC Signals.

Applications (continued)

ONE OF 8 DECODER



Die Characteristics

Transistor Count 243
Die Dimensions ..... 81.9 x 90.2 mils
Substrate Potential* ..... $-V_{SUPPLY}$
Process ..... CMOS-DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
Ceramic DIP	110	41
Plastic DIP	80	31
Ceramic LCC	82	24

*The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1-0508-5	0°C to +75°C	16-Pin CERDIP
HI3-0508-5	0°C to +75°C	16-Pin Plastic DIP
HI1-0508-4	-25°C to +85°C	16-Pin CERDIP
HI1-0508-2	-55°C to +125°C	16-Pin CERDIP
HI4P0508-5	0°C to +75°C	20-Pin PLCC
HI1-0508-7	0°C to +75°C + 96 Hr. Burn-In	16-Pin CERDIP
HI9P0508-9	-40°C to +85°C	16-Pin SOIC
HI9P0508-5	0°C to +75°C	16-Pin SOIC
HI1-0509-4	-25°C to +85°C	16-Pin CERDIP
HI1-0509-5	0°C to +75°C	16-Pin CERDIP
HI3-0509-5	0°C to +75°C	16-Pin Plastic DIP
HI4P0509-5	0°C to +75°C	20-Pin PLCC
HI1-0509-2	-55°C to +125°C	16-Pin CERDIP
HI1-0509-7	0°C to +75°C + 96 Hr. Burn-In	16-Pin CERDIP