Intel® Pentium® M Processor with 2-MB L2 Cache and 400 MHz Front Side Bus

Datasheet

May 2009

Document Number: 302189-009

Contents

Figures

Tables

Revision History

Revision	Description	Date
001	Initial release of datasheet	May 2004
002	Added Intel® Pentium® M processor 725 and 715 specifications	June 2004
003	• Specifications of Intel® Pentium® M processor Low Voltage 738 and Ultra Low Voltage 733 & 723 added in chapter 3 and chapter 5. • Chapter 2 section 2.1.3 - Missing Stop Grant State title added. Description was previously merged with Auto Halt state section and is unchanged. • Table 4 - Max ratings specifications updated	July 2004
004	Added Intel® Pentium® M processor 765 specifications	October 2004
005	• Added Intel® Pentium® M processor 753 and 758 specifications • Added Execute Disable support feature and lead free SLI (second layer interconnect) Micro-FCPGA packaging information in chapter 1 • Added Table 3-20 AGTL + Signal Group Signal DC Specifications • Table 3-18 - Voltage Tolerances for Intel® Pentium® M processor ULV (Deep Sleep State) updated	January 2005
006	• Added Intel® Pentium® M processor 778 specifications	July 2005
007	Updated Intel® Pentium® M processor 753 and 733J specifications for optimized VID	July 2005
008	Added Intel® Pentium® M processor 773 specifications	January 2006
009	Changed product name from Intel® Pentium® M Processor on 90 nm Process with 2-MB L2 Cache to Intel® Pentium® M Processor with 2-MB L2 Cache and 400 MHz Front Side Bus	May 2009

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1 Introduction

The Intel® Pentium® M processor based on 90 nm process technology featuring 2-MB L2 cache and 400-MHz front side bus (FSB) is the next generation high- performance, low-power mobile processor based on the Intel® Pentium® processor architecture.

Throughout this document, Intel Pentium M processor based on 90 nm technology featuring 2-MB L2 cache and 400 MHz FSB will be referred to as Pentium M processor, or simply the processor, including low voltage and ultra low voltage processors.

This document contains specifications for the Pentium M processors 765/ 755/ 745/ 735/ 725/ 715 Standard Voltage, 778/758/738 Low Voltage and 773/753/733J/733/723 Ultra Low Voltage[Δ].

[Δ]Intel processor numbers are not a measure of performance. Processor numbers differentiate features within each processor family, not across different processor families. See www.intel.com/products/processor_number for details.

The following list provides some of the key features on this processor:

- Supports Intel® Architecture with Dynamic Execution
- On-die, primary 32-KB instruction cache and 32-KB write-back data cache
- On-die, 2 MB second level cache with Advanced Transfer Cache Architecture
- Way set associativity and ECC (Error Correcting Code) support
- Data Prefetch Logic
- Streaming SIMD extensions 2 (SSE2)
- 400 MHz source-synchronous FSB
- Advanced power management features including Enhanced Intel SpeedStep® technology
- Micro-FCPGA and Micro-FCBGA packaging technologies
- Manufactured on Intel’s advanced 90 nanometer process technology with copper interconnect.
- Support for MMX™ technology and Internet Streaming SIMD instructions
- The processor’s data prefetch logic fetches data to the L2 cache before L1 cache requests occurs, resulting in reduced bus cycle penalties and improved performance
- Micro-FCPGA and Micro-FCBGA packaging technologies, including lead free SLI (second level interconnect) technology for the Micro-FCBGA package (for Pentium M processors 755, 745, 778, 758, 738, 773, 753, 733J/733, 723)
- Execute Disable Bit support for enhanced security (available on processors with CPU Signature = 06D8h and recommended for implementation on Intel® 915 Express chipset family-based platforms only)

The Pentium M processor will be manufactured on Intel’s advanced 90 nm process technology with copper interconnect. The processor maintains support for MMX technology and Internet Streaming SIMD instructions and full compatibility with IA-32 software. The on-die, 32-KB Level 1 instruction and data caches along with the 2-MB L2 cache with advanced transfer cache architecture enable significant performance improvement over existing mobile processors. The processor's data prefetch logic fetches data to the L2 cache before L1 cache requests occurs, resulting in reduced bus cycle penalties and improved performance.

The streaming SIMD extensions 2 (SSE2) enable break-through levels of performance in multimedia applications including 3-D graphics, video decoding/encoding, and speech recognition. The new packed double-precision floating-point instructions enhance performance for applications that require greater range and precision, including scientific and engineering applications and advanced 3-D geometry techniques, such as ray tracing.

The 400-MHz FSB on the Pentium M processor utilizes a split-transaction, deferred reply protocol and uses source-synchronous transfer (SST) of address and data to improve performance by transferring data four times per bus clock (4X data transfer rate, as in AGP 4X). Along with the 4X data bus, the address bus can deliver addresses two times per bus clock and is referred to as a "double-clocked" or 2X address bus. Working together, the 4X data bus and 2X address bus provide a data bus bandwidth of up to 3.2 GB/second. The FSB uses Advanced Gunning Transceiver Logic (AGTL+) signaling technology, a variant of GTL+ signaling technology with low power enhancements.

The processor features Enhanced Intel SpeedStep technology, which enables real-time dynamic switching between multiple voltage and frequency points. This results in optimal performance without compromising low power. The processor features the Auto Halt, Stop Grant, Deep Sleep, and Deeper Sleep low power states.

The Pentium M processor utilizes socketable Micro Flip-Chip Pin Grid Array (Micro-FCPGA) and surface mount Micro Flip-Chip Ball Grid Array (Micro-FCBGA) package technology. The Micro-FCPGA package plugs into a 479-hole, surface-mount, zero insertion force (ZIF) socket, which is referred to as the mPGA479M socket.

Pentium M processors with CPU Signature = 06D8h will also include the Execute Disable Bit capability. This feature combined with a support operating system allows memory to be marked as executable or non executable. If code attempts to run in non-executable memory the processor raises an error to the operating system. This feature can prevent some classes of viruses or worms that exploit buffer overrun vulnerabilities and can thus help improve the overall security of the system. See the *Intel® Architecture Software Developer's Manual* for more detailed information. Intel will validate this feature only on Intel 915 Express chipset family based platforms and recommends customers implement BIOS changes related to this feature, only on Intel 915 Express chipset family based platforms.

Note: The term AGTL+ is used to refer to Assisted GTL+ signalling technology on some Intel processors.

1.1 Terminology

Term	Definition
#	A "#" symbol after a signal name refers to an active low signal, indicating a signal is in the active state when driven to a low level. For example, when RESET# is low, a reset has been requested. Conversely, when NMI is high, a nonmaskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as *address* or *data*), the "#" symbol implies that the signal is inverted. For example, D[3:0] = "HLHL" refers to a hex 'A', and D[3:0]# = "LHLH" also refers to a hex "A" (H= High logic level, L= Low logic level). XXXX means that the specification or value is yet to be determined.
Front Side Bus (FSB)	Refers to the interface between the processor and system core logic (also known as the chipset components).

1.2 References

Material and concepts available in the following documents may be beneficial when reading this document. Please note that "platform design guides," when used throughout this document, refers to the platform design guides listed below:

Table 1-1. References (Sheet 1 of 2)

Document	Document Number/ Location[1]
Intel® Pentium® M Processor with 2-MB L2 Cache and 400 MHz Front Side Bus- Specification Update	http://download.intel.com/ support/processors/ mobile/pm/sb/ 30220925.pdf
Mobile Intel® 915PM/GM/GMS and 910GML Express Chipset Datasheet	http://www.intel.com/ design/mobile/datashts/ 305264.htm
Mobile Intel® 915PM/GM/GMS and 910GML Express Chipset Specification Update	http://www.intel.com/ design/mobile/specupdt/ 307167.htm
Intel®855PM Chipset Platform Design Guide: For use with Intel®Pentium® M and Intel®Celeron®Processors	http://developer.intel.com/ design/mobile/desguide/ 252614.htm
Intel® 855PM Chipset Memory Controller Hub (MCH) Datasheet	http://developer.intel.com/ design/chipsets/datashts/ 252613.htm
Intel® 855PM Chipset MCH DDR 333/200/266 MHz Specification Update	http://developer.intel.com/ design/chipsets/specupdt/ 253488.htm
Intel® 855GM/GME Chipset Graphics and Memory Controller Hub (GMCH) Datasheet	http://developer.intel.com/ design/chipsets/datashts/ 252615.htm
Intel® 855GM/GME Chipset Graphics and Memory Controller Hub (GMCH) Chipset Specification Update	http://developer.intel.com/ design/chipsets/specupdt/ 253572.htm
Intel®855GM/855GME Chipset Platform Design Guide	http://developer.intel.com/ design/mobile/desguide/ 252616.htm

Table 1-1. References (Sheet 2 of 2)

Document	Document Number/ Location[1]
IA-32 Intel® Architecture Software Developer's Manual	http://www.intel.com/ products/processor/ manuals/
Volume 1: Basic Architecture	
Volume 2A: Instruction Set Reference	
Volume 2B: Instruction Set Reference	
Volume 3: System Programming Guide	

NOTE: Contact your Intel representative for the latest revision and document number of this document.

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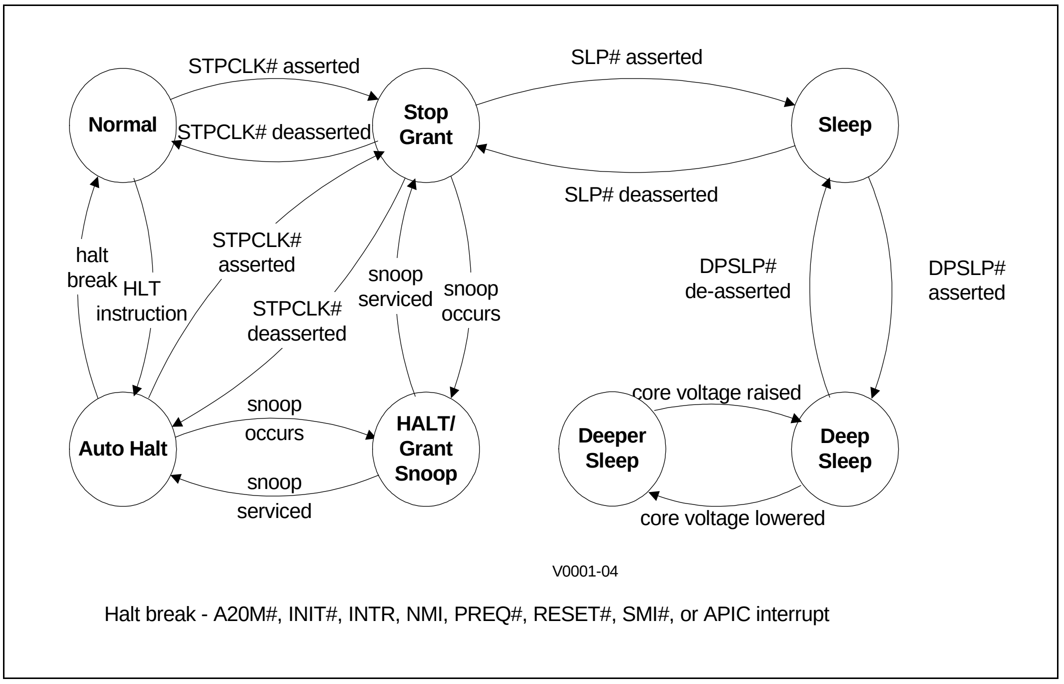
2 Low Power Features

2.1 Clock Control and Low Power States

The Pentium M processor supports the AutoHALT Power-Down, Stop Grant, Sleep, Deep Sleep, and Deeper Sleep states for optimal power management. See Figure 2-1 for a visual representation of the processor low-power states.

Figure 2-1. Clock Control States



2.1.1 Normal State

This is the normal operating state for the processor.

2.1.2 AutoHALT Power-Down State

AutoHALT Power-Down is a low-power state entered when the processor executes the HALT instruction. The processor will transition to the Normal state upon the occurrence of SMI#, INIT#, LINT[1:0] (NMI, INTR), or FSB interrupt message. RESET# will cause the processor to immediately initialize itself.

A system management interrupt (SMI) handler will return execution to either Normal state or the AutoHALT Power-Down state. See the *IA-32 Intel® Architecture Software Developer's Manual, Volume 3: System Programmer's Guide* for more information.

The system can generate a STPCLK# while the processor is in the AutoHALT Power-Down state. When the system deasserts the STPCLK# interrupt, the processor will return execution to the HALT state.

While in AutoHALT Power-Down state, the processor will process bus snoops and interrupts.

2.1.3 Stop-Grant State

When the STPCLK# pin is asserted, the Stop-Grant state of the processor is entered 20 bus clocks after the response phase of the processor-issued Stop Grant Acknowledge special bus cycle.

Since the AGTL+ signal pins receive power from the FSB, these pins should not be driven (allowing the level to return to V_{CCP}) for minimum power drawn by the termination resistors in this state. In addition, all other input pins on the FSB should be driven to the inactive state.

RESET# will cause the processor to immediately initialize itself, but the processor will stay in Stop-Grant state. A transition back to the Normal state will occur with the de-assertion of the STPCLK# signal. When re-entering the Stop-Grant state from the Sleep state, STPCLK# should be deasserted ten or more bus clocks after the de-assertion of SLP#.

A transition to the HALT/Grant Snoop state will occur when the processor detects a snoop on the FSB (see Section 2.1.3). A transition to the Sleep state (see Section 2.1.5) will occur with the assertion of the SLP# signal.

While in the Stop-Grant State, SMI#, INIT# and LINT[1:0] will be latched by the processor, and only serviced when the processor returns to the Normal State. Only one occurrence of each event will be recognized upon return to the Normal state.

While in Stop-Grant state, the processor will process snoops on the FSB and it will latch interrupts delivered on the FSB.

The PBE# signal can be driven when the processor is in Stop-Grant state. PBE# will be asserted if there is any pending interrupt latched within the processor. Pending interrupts that are blocked by the EFLAGS.IF bit being clear will still cause assertion of PBE#. Assertion of PBE# indicates to system logic that it should return the processor to the Normal state.

2.1.4 HALT/Grant Snoop State

The processor responds to snoop or interrupt transactions on the FSB while in Stop-Grant state or in AutoHALT Power-Down state. During a snoop or interrupt transaction, the processor enters the HALT/Grant Snoop state. The processor will stay in this state until the snoop on the FSB has been serviced (whether by the processor or another agent on the FSB) or the interrupt has been latched. After the snoop is serviced or the interrupt is latched, the processor will return to the Stop-Grant state or AutoHALT Power-Down state, as appropriate.

2.1.5 Sleep State

A low power state in which the processor maintains its context, maintains the phase-locked loop (PLL), and has stopped all internal clocks. The Sleep state can be entered only from Stop-Grant state. Once in the Stop-Grant state, the processor will enter the Sleep state upon the assertion of the SLP# signal. The SLP# pin should only be asserted when the processor is in the Stop Grant state. SLP# assertions while the processor is not in the Stop-Grant state is out of specification and may result in unapproved operation.

Snoop events that occur while in Sleep State or during a transition into or out of Sleep state will cause unpredictable behavior.

In the Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals (with the exception of SLP#, DPSLP# or RESET#) are allowed on the FSB while the processor is in Sleep state. Any transition on an input signal before the processor has returned to Stop-Grant state will result in unpredictable behavior.

If RESET# is driven active while the processor is in the Sleep state, and held active as specified in the RESET# pin specification, then the processor will reset itself, ignoring the transition through Stop-Grant State. If RESET# is driven active while the processor is in the Sleep State, the SLP# and STPCLK# signals should be deasserted immediately after RESET# is asserted to ensure the processor correctly executes the reset sequence.

While in the Sleep state, the processor is capable of entering an even lower power state, the Deep Sleep state by asserting the DPSLP# pin. (See Section 2.1.6.) While the processor is in the Sleep state, the SLP# pin must be deasserted if another asynchronous FSB event needs to occur.

2.1.6 Deep Sleep State

Deep Sleep state is a very low power state the processor can enter while maintaining context. Deep Sleep state is entered by asserting the DPSLP# pin while in the Sleep state. BCLK may be stopped during the Deep Sleep state for additional platform level power savings.

BCLK stop/restart timings on 855PM and Intel 855GM chipset-based platforms are as follows:

- Deep Sleep entry - DPSLP# and CPU_STP# are asserted simultaneously. The platform clock chip will stop/tristate BCLK within 2 BCLKs +/- a few nanoseconds.
- Deep Sleep exit - DPSLP# and CPU_STP# are deasserted simultaneously. The platform clock chip will drive BCLK to differential DC levels within 2-3 ns and starts toggling BCLK 2-6 BCLK periods later.

To re-enter the Sleep state, the DPSLP# pin must be deasserted. BCLK can be restarted after DPSLP# deassertion, as described above. A period of 30 microseconds (to allow for PLL stabilization) must occur before the processor can be considered to be in the Sleep State. Once in the Sleep state, the SLP# pin must be deasserted to re-enter the Stop-Grant state.

While in Deep Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions of signals are allowed on the FSB while the processor is in Deep Sleep state. Any transition on an input signal before the processor has returned to Stop-Grant state will result in unpredictable behavior.

When the processor is in Deep Sleep state, it will not respond to interrupts or snoop transactions.

2.1.7 Deeper Sleep State

The Deeper Sleep state is the lowest power state the processor can enter. This state is functionally identical to the Deep Sleep state but at a lower core voltage. The control signals to the voltage regulator to initiate a transition to the Deeper Sleep state are provided on the platform. Please refer to the platform design guides listed in Table 1-1.

2.2 Enhanced Intel SpeedStep® Technology

The Pentium M processor features Enhanced Intel SpeedStep technology. Unlike previous implementations of Intel SpeedStep technology, this technology enables the processor to switch between multiple frequency and voltage points instead of two. This will enable superior performance with optimal power savings. Switching between states is software controlled unlike previous implementations where the GHI# pin is used to toggle between two states. Following are the key features of Enhanced Intel SpeedStep technology:

- Multiple voltage/frequency operating points provide optimal performance at the lowest power.
- Voltage/Frequency selection is software controlled by writing to processor MSR's (Model Specific Registers) thus eliminating chipset dependency.
  - — If the target frequency is higher than the current frequency, Vcc is ramped up by placing a new value on the VID pins and the PLL then locks to the new frequency.
  - — If the target frequency is lower than the current frequency, the PLL locks to the new frequency and the Vcc is changed through the VID pin mechanism.
  - — Software transitions are accepted at any time. If a previous transition is in progress, the new transition is deferred until its completion.
- The processor controls voltage ramp rates internally to ensure glitch free transitions.
- Low transition latency and large number of transitions possible per second.
  - — Processor core (including L2 cache) is unavailable for up to 10 µs during the frequency transition
  - — The bus protocol (BNR# mechanism) is used to block snooping
- No bus master arbiter disable required prior to transition and no processor cache flush necessary.
- Improved Intel® Thermal Monitor mode.
  - — When the on-die thermal sensor indicates that the die temperature is too high, the processor can automatically perform a transition to a lower frequency/voltage specified in a software programmable MSR.
  - — The processor waits for a fixed time period. If the die temperature is down to acceptable levels, an up transition to the previous frequency/voltage point occurs.
  - — An interrupt is generated for the up and down Intel Thermal Monitor transitions enabling better system level thermal management.

2.3 Front Side Bus Low Power Enhancements

The Pentium M processor incorporates the following front side bus (processor system bus) low power enhancements:

- Dynamic FSB Power Down
- BPRI# control for address and control input buffers
- Dynamic On Die Termination disabling
- Low VCCP (I/O termination voltage)

The Pentium M processor incorporates the DPWR# signal that controls the data bus input buffers on the processor. The DPWR# signal disables the buffers when not used and activates them only when data bus activity occurs, resulting in significant power savings with no performance impact. BPRI# control also allows the processor address and control input buffers to be turned off when the BPRI# signal is inactive. The on-die termination on the processor FSB buffers is disabled when the signals are driven low, resulting in additional power savings. The low I/O termination voltage is on a dedicated voltage plane independent of the core voltage, enabling low I/O switching power at all times.

2.4 Processor Power Status Indicator (PSI#) Signal

The Pentium M processor incorporates the PSI# signal that is asserted when the processor is in a low power (Deep Sleep or Deeper Sleep) state. This signal is asserted upon Deep Sleep entry and deasserted upon exit. PSI# can be used to improve the light load efficiency of the voltage regulator, resulting in platform power savings and extended battery life. PSI# can also be used to simplify voltage regulator designs since it removes the need for integrated 100 µs timers required to mask the PWRGOOD signal during Deeper Sleep transitions. It also helps loosen PWRGOOD monitoring requirements in the Deeper Sleep state.

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3 Electrical Specifications

3.1 Power and Ground Pins

For clean, on-chip power distribution, the Pentium M processor has a large number of V_{CC} (power) and V_{SS} (ground) inputs. All power pins must be connected to V_{CC} power planes while all V_{SS} pins must be connected to system ground planes. Use of multiple power and ground planes is recommended to reduce I*R drop. Please refer to the platform design guides for more details. The processor V_{CC} pins must be supplied the voltage determined by the VID (Voltage ID) pins.

3.1.1 FSB Clock (BCLK[1:0]) and Processor Clocking

BCLK[1:0] directly controls the system bus interface speed as well as the core frequency of the processor. As in previous generation processors, the Pentium M processor core frequency is a multiple of the BCLK[1:0] frequency. In regards to processor clocking, the Pentium M processor uses a differential clocking implementation.

3.2 Voltage Identification

The Pentium M processor uses six voltage identification pins, VID[5:0], to support automatic selection of power supply voltages. The VID pins for the Pentium M processor are CMOS outputs driven by the processor VID circuitry. Table 3-1 specifies the voltage level corresponding to the state of VID[5:0]. A “1” in this refers to a high-voltage level and a “0” refers to low-voltage level.

Table 3-1. Voltage Identification Definition

VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	V_{CC} V	VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	V_{CC} V
0	0	0	0	0	0	1.708	1	0	0	0	0	0	1.196
0	0	0	0	0	1	1.692	1	0	0	0	0	1	1.180
0	0	0	0	1	0	1.676	1	0	0	0	1	0	1.164
0	0	0	0	1	1	1.660	1	0	0	0	1	1	1.148
0	0	0	1	0	0	1.644	1	0	0	1	0	0	1.132
0	0	0	1	0	1	1.628	1	0	0	1	0	1	1.116
0	0	0	1	1	0	1.612	1	0	0	1	1	0	1.100
0	0	0	1	1	1	1.596	1	0	0	1	1	1	1.084
0	0	1	0	0	0	1.580	1	0	1	0	0	0	1.068
0	0	1	0	0	1	1.564	1	0	1	0	0	1	1.052
0	0	1	0	1	0	1.548	1	0	1	0	1	0	1.036
0	0	1	0	1	1	1.532	1	0	1	0	1	1	1.020
0	0	1	1	0	0	1.516	1	0	1	1	0	0	1.004
0	0	1	1	0	1	1.500	1	0	1	1	0	1	0.988
0	0	1	1	1	0	1.484	1	0	1	1	1	0	0.972
0	0	1	1	1	1	1.468	1	0	1	1	1	1	0.956
0	1	0	0	0	0	1.452	1	1	0	0	0	0	0.940
0	1	0	0	0	1	1.436	1	1	0	0	0	1	0.924
0	1	0	0	1	0	1.420	1	1	0	0	1	0	0.908
0	1	0	0	1	1	1.404	1	1	0	0	1	1	0.892
0	1	0	1	0	0	1.388	1	1	0	1	0	0	0.876
0	1	0	1	0	1	1.372	1	1	0	1	0	1	0.860
0	1	0	1	1	0	1.356	1	1	0	1	1	0	0.844
0	1	0	1	1	1	1.340	1	1	0	1	1	1	0.828
0	1	1	0	0	0	1.324	1	1	1	0	0	0	0.812
0	1	1	0	0	1	1.308	1	1	1	0	0	1	0.796
0	1	1	0	1	0	1.292	1	1	1	0	1	0	0.780
0	1	1	0	1	1	1.276	1	1	1	0	1	1	0.764
0	1	1	1	0	0	1.260	1	1	1	1	0	0	0.748
0	1	1	1	0	1	1.244	1	1	1	1	0	1	0.732
0	1	1	1	1	0	1.228	1	1	1	1	1	0	0.716
0	1	1	1	1	1	1.212	1	1	1	1	1	1	0.700

3.3 Catastrophic Thermal Protection

The Pentium M processor supports the THERMTRIP# signal for catastrophic thermal protection. An external thermal sensor should also be used to protect the processor and the system against excessive temperatures. Even with the activation of THERMTRIP#, which halts all processor internal clocks and activity, leakage current can be high enough such that the processor cannot be protected in all conditions without the removal of power to the processor. If the external thermal sensor detects a catastrophic processor temperature of 125 °C (maximum), or if the THERMTRIP# signal is asserted, the VCC supply to the processor must be turned off within 500 ms to prevent permanent silicon damage due to thermal runaway.

3.4 Signal Terminations and Unused Pins

All RSVD (RESERVED) pins must remain unconnected. Connection of these pins to V_{CC}, V_{SS}, or to any other signal (including each other) can result in component malfunction or incompatibility with future Pentium M processors. See Section 4.2 for a pin listing of the processor and the location of all RSVD pins.

For reliable operation, always connect unused inputs or bidirectional signals to an appropriate signal level. Unused active low AGTL+ inputs may be left as no connects if AGTL+ termination is provided on the processor silicon. Unused active high inputs should be connected through a resistor to ground (V_{SS}). Unused outputs can be left unconnected.

For details on signal terminations, please refer to the platform design guides.

The TEST1 and TEST2 pins must have a stuffing option connection to V_{SS} separately via 1-kΩ, pull-down resistors.

3.5 FSB Frequency Select Signals (BSEL[1:0])

These signals are used to select the FSB clock frequency. They should be connected between the processor and the chipset MCH and clock generator on Intel 915 Express chipset family based platforms. These signals must be left unconnected on platforms designed with the Intel 855 chipset family. On these platforms, FSB clock frequency should be configured on the motherboard.

3.6 FSB Signal Groups

In order to simplify the following discussion, the FSB signals have been combined into groups by buffer type. AGTL+ input signals have differential input buffers, which use GTLREF as a reference level. In this document, the term "AGTL+ Input" refers to the AGTL+ input group as well as the AGTL+ I/O group when receiving. Similarly, "AGTL+ Output" refers to the AGTL+ output group as well as the AGTL+ I/O group when driving.

With the implementation of a source synchronous data bus comes the need to specify two sets of timing parameters. One set is for common clock signals which are dependant upon the rising edge of BCLK0 (ADS#, HIT#, HITM#, etc.) and the second set is for the source synchronous signals which are relative to their respective strobe lines (data and address) as well as the rising edge of BCLK0. Asychronous signals are still present (A20M#, IGNNE#, etc.) and can become active at any time during the clock cycle. Table 3-2 identifies which signals are common clock, source synchronous, and asynchronous.

Table 3-2. FSB Pin Groups

<table>
<tr><th>Signal Group</th><th>Type</th><th>Signals[1]</th></tr>
<tr><td>AGTL+ Common Clock Input</td><td>Synchronous to BCLK[1:0]</td><td>BPRI#, DEFER#, DPWR#, PREQ#, RESET#, RS[2:0]#, TRDY#</td></tr>
<tr><td>AGTL+ Common Clock I/O</td><td>Synchronous to BCLK[1:0]</td><td>ADS#, BNR#, BPM[3:0]#, BR0#, DBSY#, DRDY#, HIT#, HITM#, LOCK#, PRDY#</td></tr>
<tr><td>AGTL+ Source Synchronous I/O</td><td>Synchronous to assoc. strobe</td><td><table>
<tr><th>Signals</th><th>Associated Strobe</th></tr>
<tr><td>REQ[4:0]#, A[16:3]#</td><td>ADSTB[0]#</td></tr>
<tr><td>A[31:17]#</td><td>ADSTB[1]#</td></tr>
<tr><td>D[15:0]#, DINV0#</td><td>DSTBP0#, DSTBN0#</td></tr>
<tr><td>D[31:16]#, DINV1#</td><td>DSTBP1#, DSTBN1#</td></tr>
<tr><td>D[47:32]#, DINV2#</td><td>DSTBP2#, DSTBN2#</td></tr>
<tr><td>D[63:48]#, DINV3#</td><td>DSTBP3#, DSTBN3#</td></tr>
</table></td></tr>
<tr><td>AGTL+ Strobes</td><td>Synchronous to BCLK[1:0]</td><td>ADSTB[1:0]#, DSTBP[3:0]#, DSTBN[3:0]#</td></tr>
<tr><td>CMOS Input</td><td>Asynchronous</td><td>A20M#, DPSLP#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PWRGOOD, SMI#, SLP#, STPCLK#</td></tr>
<tr><td>Open Drain Output</td><td>Asynchronous</td><td>FERR#, IERR#, PROCHOT#, THERMTRIP#</td></tr>
<tr><td>CMOS Output</td><td>Asynchronous</td><td>PSI#, VID[5:0], BSEL[1:0]</td></tr>
<tr><td>CMOS Input</td><td>Synchronous to TCK</td><td>TCK, TDI, TMS, TRST#</td></tr>
<tr><td>Open Drain Output</td><td>Synchronous to TCK</td><td>TDO</td></tr>
<tr><td>FSB Clock</td><td>Clock</td><td>BCLK[1:0], ITP_CLK[1:0][2]</td></tr>
<tr><td>Power/Other</td><td></td><td>COMP[3:0], DBR#[2], GTLREF, RSVD, TEST2, TEST1, THERMDA, THERMDC, V_{CC}, V_{CCA}[3:0], V_{CCP}, V_{CCQ}[1:0], V_{CC_SENSE}, V_{SS}, V_{SS_SENSE}</td></tr>
</table>

NOTES:
1. Refer to Chapter 4 for signal descriptions and termination requirements.
2. BPM[2:0}# and PRDY# are AGTL+ output only signals.
3. In processor systems where there is no debug port implemented on the system board, these signals are used to support a debug port interposer. In systems with the debug port implemented on the system board, these signals are no connects.

3.7 CMOS Signals

CMOS input signals are shown in Table 3-2. Legacy output FERR#, IERR# and other non-AGTL+ signals (THERMTRIP# and PROCHOT#) utilize Open Drain output buffers. These signals do not have setup or hold time specifications in relation to BCLK[1:0]. However, all of the CMOS signals are required to be asserted for at least three BCLKs in order for the processor to recognize them. See Section 3.9 for the DC and AC specifications for the CMOS signal groups.

3.8 Maximum Ratings

Table 3-3 lists the processor's maximum environmental stress ratings. The processor should not receive a clock while subjected to these conditions. Functional operating parameters are listed in the AC and DC tables. Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the processor contains protective circuitry to resist damage from electro static discharge (ESD), one should always take precautions to avoid high static voltages or electric fields.

Table 3-3. Processor DC Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
TSTORAGE	Processor storage temperature	-40	85	°C	2
V_{CC}	Any processor supply voltage with respect to V_{SS}	-0.3	1.6	V	1
$V_{inAGTL+}$	AGTL+ buffer DC input voltage with respect to V_{SS}	-0.1	1.6	V	1, 2
$V_{inAsynch\_CMOS}$	CMOS buffer DC input voltage with respect to V_{SS}	-0.1	1.6	V	1, 2

NOTES:
1. This rating applies to any processor pin.
2. Contact Intel for storage requirements in excess of one year.

3.9 Processor DC Specifications

The processor DC specifications in this section are defined at the processor core (pads) unless noted otherwise. See Table 4-3 for the pin signal definitions and signal pin assignments. The DC specifications for these signals are listed in Table 3-24 and Table 3-25.

Table 3-4 through Table 3-25 list the DC specifications for the Pentium M processor and are valid only while meeting specifications for junction temperature, clock frequency, and input voltages. The Highest Frequency mode (HFM) and Lowest Frequency mode (LFM) refer to the highest and lowest core operating frequencies supported on the processor. Active mode load line specifications apply in all states except in the Deep Sleep and Deeper Sleep states. $V_{CC,BOOT}$ is the default voltage driven by the voltage regulator at power up in order to set the VID values. Unless specified otherwise, all specifications for the Pentium M processor are at Tjunction = 100° C. Care should be taken to read all notes associated with each parameter.

Table 3-4. Voltage and Current Specifications - Standard Voltage Processors (Sheet 1 of 2)

Symbol	Parameter	VID#A Typical	VID#B Typical	VID#C Typical	VID#D Typical	VID#E Typical	Unit	Notes
V_{CCD765}	Intel® Pentium® M Processor 765 Core $V_{CC\ FOR}$ Enhanced Intel SpeedStep® Technology Operating Points:						V	1, 2
	2.1 GHz	1.340	1.324	1.308		1.356		
	1.8 GHz	1.276	1.260	1.244		1.292		
	1.6 GHz	1.228	1.212	1.212		1.244		
	1.4 GHz	1.180	1.180	1.164		1.196		
	1.2 GHz	1.132	1.132	1.116		1.148		
	1.0 GHz	1.084	1.084	1.084		1.100		
	800 MHz	1.036	1.036	1.036		1.052		
	600 MHz	0.988	0.988	0.988		0.988		
V_{CCD755}	Pentium M Processor 755 Core V_{CC} for Enhanced Intel SpeedStep Technology Operating Points:						V	1, 2
	2.0 GHz	1.340	1.324	1.308	1.276			
	1.8 GHz	1.292	1.276	1.276	1.244			
	1.6 GHz	1.244	1.228	1.228	1.196			
	1.4 GHz	1.196	1.180	1.180	1.164			
	1.2 GHz	1.148	1.132	1.132	1.116			
	1.0 GHz	1.100	1.084	1.084	1.084			
	800 MHz	1.052	1.036	1.036	1.036			
	600 MHz	0.988	0.988	0.988	0.988			
V_{CCD745}	Pentium M Processor 745 Core V_{CC} for Enhanced Intel SpeedStep Technology Operating Points:						V	1, 2
	1.8 GHz	1.340	1.324	1.308	1.276			
	1.6 GHz	1.292	1.276	1.260	1.228			
	1.4 GHz	1.228	1.212	1.212	1.180			
	1.2 GHz	1.164	1.164	1.148	1.132			
	1.0 GHz	1.116	1.100	1.100	1.084			
	800 MHz	1.052	1.052	1.052	1.036			
	600 MHz	0.988	0.988	0.988	0.988			

Table 3-4. Voltage and Current Specifications - Standard Voltage Processors (Sheet 2 of 2)

Symbol	Parameter	VID#A Typical	VID#B Typical	VID#C Typical	VID#D Typical	VID#E Typical	Unit	Notes
V_{CCD735}	Pentium M Processor 735 Core V_{CC} for Enhanced Intel SpeedStep Technology Operating Points:						V	1, 2
	1.7 GHz	1.340	1.324	1.308	1.276			
	1.4 GHz	1.244	1.244	1.228	1.212			
	1.2 GHz	1.180	1.180	1.164	1.148			
	1.0 GHz	1.116	1.116	1.116	1.100			
	800 MHz	1.052	1.052	1.052	1.052			
	600 MHz	0.988	0.988	0.988	0.988			
V_{CCD725}	Pentium M Processor 725 Core V_{CC} for Enhanced Intel SpeedStep Technology Operating Points:						V	1, 2
	1.6 GHz	1.340	1.324	1.308	1.276			
	1.4 GHz	1.276	1.260	1.244	1.228			
	1.2 GHz	1.212	1.196	1.180	1.164			
	1.0 GHz	1.132	1.132	1.116	1.116			
	800 MHz	1.068	1.068	1.052	1.052			
	600 MHz	0.988	0.988	0.988	0.988			
V_{CCD715}	Pentium M Processor 715 Core V_{CC} for Enhanced Intel SpeedStep Technology Operating Points:						V	1, 2
	1.5 GHz	1.340	1.324	1.308	1.276			
	1.2 GHz	1.228	1.212	1.212	1.180			
	1.0 GHz	1.148	1.148	1.132	1.116			
	800 MHz	1.068	1.068	1.068	1.052			
	600 MHz	0.988	0.988	0.988	0.988			

NOTES:
1. The typical values shown are the VID encoded voltages. Static and ripple tolerances (for minimum and maximum voltages) are defined in the load line tables, Table 3-8 through Table 3-21. Adherence to loadline specifications for the Pentium M processor is required to ensure reliable processor operation.
2. The voltage specifications are assumed to be measured at a via on the motherboard's opposite side of the processor's socket (or BGA) ball with a 100-MHz bandwidth oscilloscope, 1.5-pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.

Table 3-5. Voltage and Current Specifications - Low Voltage Processors (Sheet 1 of 2)

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{CCD778}	Intel® Pentium® M Processor, Low Voltage 778 Core VCC for Enhanced Intel SpeedStep® Technology Operating Points:				V	1, 2
	1.6 GHz		1.116			
	1.5 GHz		1.116			
	1.4 GHz		1.100			
	1.3 GHz		1.084			
	1.2 GHz		1.068			
	1.1 GHz		1.052			
	1.0 GHz		1.052			
	900 GHz		1.036			
	800 MHz		1.020			
	600 MHz		0.988			
V_{CCD758}	Pentium M Processor, Low Voltage, 758 Core VCC for Enhanced Intel SpeedStep Technology Operating Points:				V	1, 2
	1.5 GHz		1.116			
	1.4 GHz		1.116			
	1.3 GHz		1.100			
	1.2 GHz		1.084			
	1.1 GHz		1.068			
	1.0 GHz		1.052			
	900 GHz		1.036			
	800 MHz		1.020			
	600 MHz		0.988			

Table 3-5. Voltage and Current Specifications - Low Voltage Processors (Sheet 2 of 2)

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{CCD738}	Pentium M Processor, Low Voltage, 738 Core VCC for Enhanced Intel SpeedStep Technology Operating Points:				V	1, 2
	1.4 GHz		1.116			
	1.3 GHz		1.116			
	1.2 GHz		1.100			
	1.1 GHz		1.068			
	1.0 GHz		1.052			
	900 GHz		1.036			
	800 MHz		1.020			
	600 MHz		0.988			

NOTES:

1. The typical values shown are the VID encoded voltages. Static and ripple tolerances (for minimum and maximum voltages) are defined in the load line tables, Table 3-8 through Table 3-21. Adherence to loadline specifications for the Pentium M processor is required to ensure reliable processor operation.
2. The voltage specifications are assumed to be measured at a via on the motherboard's opposite side of the processor's socket (or BGA) ball with a 100-MHz bandwidth oscilloscope, 1.5-pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.

Table 3-6. Voltage and Current Specifications - Ultra Low Voltage Processors (Sheet 1 of 2)

Symbol	Parameter	Min	Typ	Max	VID# GTyp	VID# HTyp	VID#I Typ	VID# J Typ	VID# K Typ	VID# L Typ	Unit	Note
V_{CCD773}	Intel® Pentium® M Processor, Ultra Low Voltage, 773 Core VCC for Enhanced Intel SpeedStep® Technology Operating Points:										V	2, 3
	1.3 GHz				0.956	0.940	0.924	0.908	0.892	0.876		
	1.2 GHz				0.940	0.924	0.908	0.908	0.892	0.876		
	1.1 GHz				0.924	0.908	0.892	0.892	0.876	0.860		
	1.0 GHz				0.908	0.892	0.876	0.876	0.860	0.860		
	900 MHz				0.876	0.876	0.860	0.860	0.860	0.844		
	800 MHz				0.860	0.860	0.844	0.844	0.844	0.844		
	600 MHz				0.812	0.812	0.812	0.812	0.812	0.812		
V_{CCD753}	Pentium M Processor, Ultra Low Voltage, 753 Core VCC for Enhanced Intel SpeedStep Technology Operating Points:										V	2, 3
	1.2 GHz				0.956	0.940	0.924	0.908	0.892	0.876		
	1.1 GHz				0.940	0.924	0.908	0.892	0.892	0.876		
	1.0 GHz				0.908	0.908	0.892	0.876	0.876	0.860		
	900 MHz				0.892	0.876	0.876	0.860	0.860	0.844		
	800 MHz				0.860	0.860	0.860	0.844	0.844	0.844		
	600 MHz				0.812	0.812	0.812	0.812	0.812	0.812		
$V_{CCD733J}$	Pentium M Processor, Ultra Low Voltage, 733J Core VCC for Enhanced Intel SpeedStep Technology operating points:										V	2, 3, 4
	1.1 GHz				0.956	0.940	0.924	0.908	0.892	0.876		
	1.0 GHz				0.940	0.924	0.908	0.892	0.876	0.876		
	900 MHz				0.908	0.892	0.892	0.876	0.860	0.860		
	800 MHz				0.876	0.876	0.860	0.860	0.844	0.844		
	600 MHz				0.812	0.812	0.812	0.812	0.812	0.812		

Table 3-6. Voltage and Current Specifications - Ultra Low Voltage Processors (Sheet 2 of 2)

Symbol	Parameter	Min	Typ	Max	VID# GTyp	VID# HTyp	VID#I Typ	VID# J Typ	VID# K Typ	VID# L Typ	Unit	Note
V_{CCD733}	Pentium M Processor, Ultra Low Voltage, 733 Core VCC for Enhanced Intel SpeedStep Technology Operating Points:										V	1, 3
	1.1 GHz		0.940									
	1.0 GHz		0.924									
	900 MHz		0.892									
	800 MHz		0.876									
	600 MHz		0.812									
V_{CCD723}	Pentium M Processor, Ultra Low Voltage, 723 Core VCC for Enhanced Intel SpeedStep Technology Operating Points:										V	1, 3
	1.0 GHz		0.940									
	900 MHz		0.908									
	800 MHz		0.876									
	600 MHz		0.812									

NOTES:
1. The typical values shown are the VID encoded voltages. Static and ripple tolerances (for minimum and maximum voltages) are defined in the load line tables, Table 3-8 through Table 3-21. Adherence to loadline specifications for the Pentium M processor is required to ensure reliable processor operation.
2. These are VID values. Individual processor VID values may be calibrated during manufacturing such that two devices at the same speed may have different VID settings. Actual voltage supplied to the processor should be as specified in the load lines in Figure 3-11 and Figure 3-12. Adherence to load line specifications is required to ensure reliable processor operation.
3. The voltage specifications are assumed to be measured at a via on the motherboard's opposite side of the processor's socket (or BGA) ball with a 100-MHz bandwidth oscilloscope, 1.5-pF maximum probe capacitance, and 1-MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
4. For 733J, CPU signature = 06D8h.

Table 3-7. Voltage and Current Specifications (Continued) (Sheet 1 of 3)

Symbol	Parameter	Min	Typ	Max	Unit	Note
$V_{CC,BOOT}$	Default V_{CC} Voltage for Initial Power-Up	1.14	1.20	1.26	V	2
V_{CCP}	AGTL+ Termination voltage	0.997	1.05	1.102	V	2
V_{CCA}	PLL Supply Voltage	1.71	1.8	1.89	V	2,
V_{CCA} for 778, 758, 738 and 753,733J, 733, 723	PLL Supply Voltage for Pentium M Processors				V	2, 8
	778/758/738	1.71	1.8	1.89		
	753/733J/733/723	1.425	1.5	1.575		
$V_{CCDPRSLP,TR1}$	Transient Deeper Sleep Voltage	0.695	0.748	0.795	V	2
$V_{CCDPRSLP,ST1}$	Static Deeper Sleep Voltage	0.705	0.748	0.785	V	2
$V_{CCDPRSLP,TR2}$	Transient Deeper Sleep Voltage	0.669	0.726	0.783	V	2, 9
$V_{CCDPRSLP,ST2}$	Static Deeper Sleep Voltage	0.679	0.726	0.793	V	2, 9
I_{CCDES}	I_{CC} for Pentium M Processors Recommended Design Target			25	A	5
I_{CC}	I_{CC} for Pentium M Processors:				A	3, 10
	765/755/745/778/758/738/735/725/715 at LFM Vcc			8.1		
	765/755/745/735/725/715 at HFM Vcc			21.0		
	778/758/738 at HFM Vcc			12.0		
	773/753/733J/733/723 at LFM Vcc			4.0		
	773/753/733J at HFM Vcc			7.5		
	773/733/723 at HFM Vcc			7.0		

Table 3-7. Voltage and Current Specifications (Continued) (Sheet 2 of 3)

Symbol	Parameter	Min	Typ	Max	Unit	Note
I_{AH}, I_{SGNT}	I_{CC} Auto-Halt & Stop-Grant for Pentium M Processors:				A	4, 10
	765/755/745/778/758/738/735/725/715 at LFM Vcc			6.0		
	765/755/745/735/725/715 at HFM Vcc			15.1		
	778/758/738 at HFM Vcc			6.4		
	773/753/733J at LFM Vcc			2.3		
	733/723 at LFM Vcc			2.1		
	773/753/733J HFM Vcc			3.3		
	733/723 at HFM Vcc			3.1		
I_{SLP}	I_{CC} Sleep for Pentium M Processors:				A	4, 10
	765/755/745/778/758/738/735/725/715 at LFM Vcc			5.9		
	765/755/745/735/725/715 at HFM Vcc			14.8		
	778/758/738 at HFM Vcc			6.2		
	773/753/733J at LFM Vcc			2.2		
	733/723 at LFM Vcc			2.0		
	773/753/733J at HFM Vcc			3.2		
	733/723 at HFM Vcc			3.0		
I_{DSLP}	I_{CC} Deep Sleep for Pentium M Processors:				A	4, 10
	765/755/745/778/758/738/735/725/715 at LFM Vcc			5.8		
	765/755/745/735/725/715 at HFM Vcc			14.2		
	778/758/738 at HFM Vcc			5.7		
	773/753/733J at LFM Vcc			2.1		
	733/723 at LFM Vcc			1.9		
	773/753/733J at HFM Vcc			2.9		
	733/723 at HFM Vcc			2.7		

Table 3-7. Voltage and Current Specifications (Continued) (Sheet 3 of 3)

Symbol	Parameter	Min	Typ	Max	Unit	Note
$I_{DPRSLP1}$	I_{CC} Deeper Sleep @ 0.748 V for Pentium M Processors:				A	4, 9, 10
	765/755/745/778/758/738/ 735/725/715			2.5		
	753/733J/733/723			1.6		
$I_{DPRSLP1}$	I_{CC} Deeper Sleep @ 0.726 V for Pentium M Processors:				A	4, 9, 10
	765/755/745/778/758/738/ 735/725/715			2.3		
	753/733J/733/723			1.3		
$dI_{CC/DT}$	V_{CC} power supply current slew rate			0.5	A/ns	6, 7
I_{CCA}	I_{CC} for V_{CCA} supply			120	mA	
I_{CCP}	I_{CC} for V_{CCP} supply			2.5	A	

NOTES:
1. The typical values shown are the VID encoded voltages. Static and ripple tolerances (for minimum and maximum voltages) are defined in the load line tables i.e., Table 3-8 through Table 3-21. Adherence to loadline specifications for the Pentium M processor is required to ensure reliable processor operation.
2. The voltage specifications are assumed to be measured at a via on the motherboard's opposite side of the processor's socket (or BGA) ball with a 100-MHz bandwidth oscilloscope, 1.5-pF maximum probe capacitance, and 1-Mohm minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
3. Specified at $V_{CC,STATIC}$ (nominal) under maximum signal loading conditions.
4. Specified at the VID voltage.
5. The I_{CCDES}(max) specification comprehends future processor HFM frequencies. Platforms should be designed to this specification.
6. Based on simulations and averaged over the duration of any change in current. Specified by design/ characterization at nominal V_{CC}. Not 100% tested.
7. Measured at the bulk capacitors on the motherboard.
8. Pentium M processors LV and ULV will support VCCA supply voltages of both 1.8 V ±5% and1.5 V ±5%.
9. Deeper sleep voltage of 0.726 V (typical) is supported on LV and ULV Pentium M processors with CPU signature =06D8h. A typical voltage setting between 0.726 V and 0.748 V may be used but the minimum and maximum voltages specified in Table 3-7 should not be exceeded.
10. For 733J, CPU signature = 06D8h.

Table 3-8. Voltage Tolerances for the Intel® Pentium® M Processor (Active State) VID#A

MODE	Highest Frequency Mode: VID=1.340V, Offset=0%						Lowest Frequency Mode: VID=0.988V, Offset=0%					
	I_{CC}, A	V_{CC}, V	STATIC		Ripple		I_{CC}, A	V_{CC}, V	STATIC		Ripple	
			Min	Max	Min	Max			Min	Max	Min	Max
ACTIVE	0	1.340	1.320	1.360	1.310	1.370	0.0	0.988	0.973	1.003	0.963	1.013
	0.9	1.337	1.317	1.357	1.307	1.367	0.4	0.987	0.972	1.002	0.962	1.012
	1.9	1.334	1.314	1.355	1.304	1.365	0.9	0.985	0.971	1.000	0.961	1.010
	2.8	1.332	1.312	1.352	1.302	1.362	1.3	0.984	0.969	0.999	0.959	1.009
	3.7	1.329	1.309	1.349	1.299	1.359	1.7	0.983	0.968	0.998	0.958	1.008
	4.6	1.326	1.306	1.346	1.296	1.356	2.1	0.982	0.967	0.996	0.957	1.006
	5.6	1.323	1.303	1.343	1.293	1.353	2.6	0.980	0.966	0.995	0.956	1.005
	6.5	1.321	1.300	1.341	1.290	1.351	3.0	0.979	0.964	0.994	0.954	1.004
	7.4	1.318	1.298	1.338	1.288	1.348	3.4	0.978	0.963	0.993	0.953	1.003
	8.3	1.315	1.295	1.335	1.285	1.345	3.8	0.976	0.962	0.991	0.952	1.001
	9.3	1.312	1.292	1.332	1.282	1.342	4.3	0.975	0.960	0.990	0.950	1.000
	10.2	1.309	1.289	1.330	1.279	1.340	4.7	0.974	0.959	0.989	0.949	0.999
	11.1	1.307	1.287	1.327	1.277	1.337	5.1	0.973	0.958	0.987	0.948	0.997
	12.0	1.304	1.284	1.324	1.274	1.334	5.5	0.971	0.957	0.986	0.947	0.996
	13.0	1.301	1.281	1.321	1.271	1.331	6.0	0.970	0.955	0.985	0.945	0.995
	13.9	1.298	1.278	1.318	1.268	1.328	6.4	0.969	0.954	0.984	0.944	0.994
	14.8	1.296	1.275	1.316	1.265	1.326	6.8	0.968	0.953	0.982	0.943	0.992
	15.7	1.293	1.273	1.313	1.263	1.323	7.2	0.966	0.951	0.981	0.941	0.991
	16.7	1.290	1.270	1.310	1.260	1.320	7.7	0.965	0.950	0.980	0.940	0.990
	17.6	1.287	1.267	1.307	1.257	1.317	**8.1**	**0.964**	**0.949**	**0.979**	**0.939**	**0.989**
	18.5	1.284	1.264	1.305	1.254	1.315						
	19.4	1.282	1.262	1.302	1.252	1.312						
	20.4	1.279	1.259	1.299	1.249	1.309						
	21.3	1.276	1.256	1.296	1.246	1.306						
	22.2	1.273	1.253	1.293	1.243	1.303						
	23.1	1.271	1.250	1.291	1.240	1.301						
	24.1	1.268	1.248	1.288	1.238	1.298						
	25.0	**1.265**	**1.245**	**1.285**	**1.235**	**1.295**						

Figure 3-1. Illustration of Active State V_{CC} Static and Ripple Tolerances (HFM- VID#A)

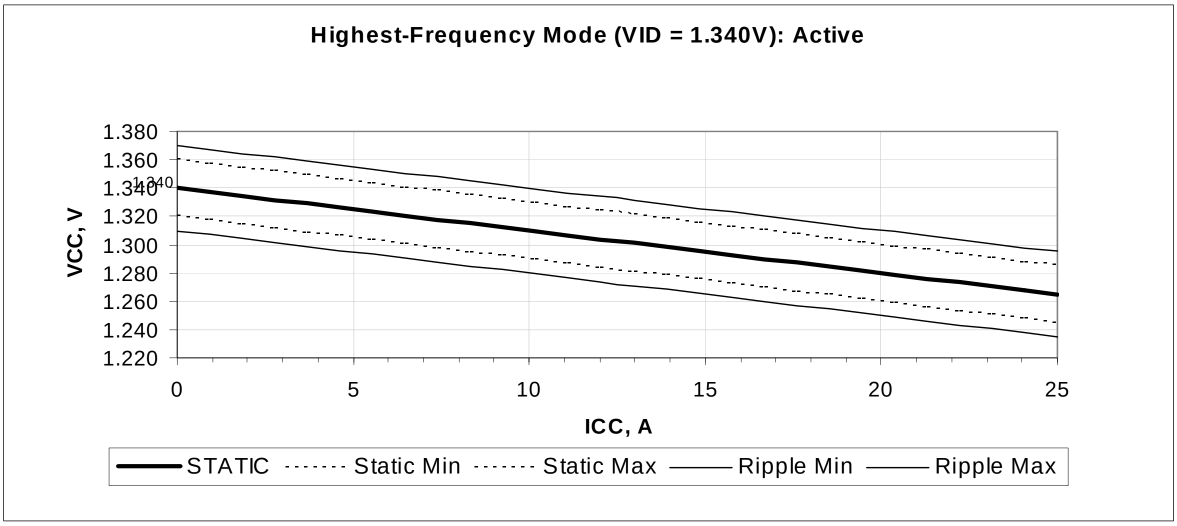


Table 3-9. Voltage Tolerances for the Intel® Pentium® M Processor (Deep Sleep State) VID#A

MODE	Highest Frequency Mode: VID=1.340V, Offset=-1.2%						Lowest Frequency Mode: VID=0.988V, Offset=-1.2%					
	I_{CC}, A	V_{CC}, V	STATIC		Ripple		I_{CC}, A	V_{CC}, V	STATIC		Ripple	
			Min	Max	Min	Max			Min	Max	Min	Max
Deep Sleep	0.0	1.324	1.304	1.344	1.294	1.354	0.0	0.976	0.961	0.991	0.951	1.001
	0.9	1.321	1.301	1.341	1.291	1.351	0.4	0.975	0.960	0.990	0.950	1.000
	1.9	1.318	1.298	1.338	1.288	1.348	0.8	0.974	0.959	0.989	0.949	0.999
	2.8	1.315	1.295	1.336	1.285	1.346	1.2	0.973	0.958	0.987	0.948	0.997
	3.8	1.313	1.292	1.333	1.282	1.343	1.5	0.972	0.957	0.986	0.947	0.996
	4.7	1.310	1.290	1.330	1.280	1.340	1.9	0.970	0.956	0.985	0.946	0.995
	5.7	1.307	1.287	1.327	1.277	1.337	2.3	0.969	0.954	0.984	0.944	0.994
	6.6	1.304	1.284	1.324	1.274	1.334	2.7	0.968	0.953	0.983	0.943	0.993
	7.6	1.301	1.281	1.321	1.271	1.331	3.1	0.967	0.952	0.982	0.942	0.992
	8.5	1.298	1.278	1.318	1.268	1.328	3.5	0.966	0.951	0.981	0.941	0.991
	9.5	1.296	1.275	1.316	1.265	1.326	3.9	0.965	0.950	0.979	0.940	0.989
	10.4	1.293	1.273	1.313	1.263	1.323	4.3	0.963	0.949	0.978	0.939	0.988
	11.4	1.290	1.270	1.310	1.260	1.320	4.6	0.962	0.947	0.977	0.937	0.987
	12.3	1.287	1.267	1.307	1.257	1.317	5.0	0.961	0.946	0.976	0.936	0.986
	13.3	1.284	1.264	1.304	1.254	1.314	5.4	0.960	0.945	0.975	0.935	0.985
	14.2	**1.281**	**1.261**	**1.301**	**1.251**	**1.311**	**5.8**	**0.959**	**0.944**	**0.974**	**0.934**	**0.984**

Figure 3-2. Illustration of Deep Sleep State V_{CC} Static and Ripple Tolerances (LFM- VID#A)

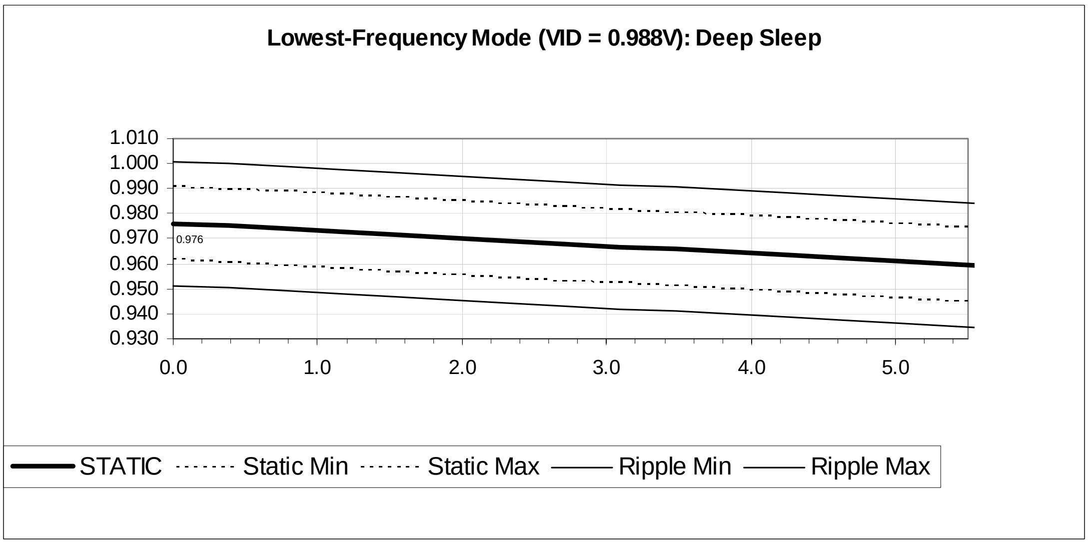


Table 3-10. Voltage Tolerances for the Intel® Pentium® M Processor (Active State) VID#B

MODE	Highest Frequency Mode: VID=1.324V, Offset=0%						Lowest Frequency Mode: VID=0.988V, Offset=0%					
	I_{CC}, A	V_{CC}, V	STATIC		Ripple		I_{CC}, A	V_{CC}, V	STATIC		Ripple	
			Min	Max	Min	Max			Min	Max	Min	Max
ACTIVE	0	1.324	1.304	1.344	1.294	1.354	0.0	0.988	0.973	1.003	0.963	1.013
	0.9	1.321	1.301	1.341	1.291	1.351	0.4	0.987	0.972	1.002	0.962	1.012
	1.9	1.318	1.299	1.338	1.289	1.348	0.9	0.985	0.971	1.000	0.961	1.010
	2.8	1.316	1.296	1.336	1.286	1.346	1.3	0.984	0.969	0.999	0.959	1.009
	3.7	1.313	1.293	1.333	1.283	1.343	1.7	0.983	0.968	0.998	0.958	1.008
	4.6	1.310	1.290	1.330	1.280	1.340	2.1	0.982	0.967	0.996	0.957	1.006
	5.6	1.307	1.287	1.327	1.277	1.337	2.6	0.980	0.966	0.995	0.956	1.005
	6.5	1.305	1.285	1.324	1.275	1.334	3.0	0.979	0.964	0.994	0.954	1.004
	7.4	1.302	1.282	1.322	1.272	1.332	3.4	0.978	0.963	0.993	0.953	1.003
	8.3	1.299	1.279	1.319	1.269	1.329	3.8	0.976	0.962	0.991	0.952	1.001
	9.3	1.296	1.276	1.316	1.266	1.326	4.3	0.975	0.960	0.990	0.950	1.000
	10.2	1.293	1.274	1.313	1.264	1.323	4.7	0.974	0.959	0.989	0.949	0.999
	11.1	1.291	1.271	1.311	1.261	1.321	5.1	0.973	0.958	0.987	0.948	0.997
	12.0	1.288	1.268	1.308	1.258	1.318	5.5	0.971	0.957	0.986	0.947	0.996
	13.0	1.285	1.265	1.305	1.255	1.315	6.0	0.970	0.955	0.985	0.945	0.995
	13.9	1.282	1.262	1.302	1.252	1.312	6.4	0.969	0.954	0.984	0.944	0.994
	14.8	1.280	1.260	1.299	1.250	1.309	6.8	0.968	0.953	0.982	0.943	0.992
	15.7	1.277	1.257	1.297	1.247	1.307	7.2	0.966	0.951	0.981	0.941	0.991
	16.7	1.274	1.254	1.294	1.244	1.304	7.7	0.965	0.950	0.980	0.940	0.990
	17.6	1.271	1.251	1.291	1.241	1.301	**8.1**	**0.964**	**0.949**	**0.979**	**0.939**	**0.989**
	18.5	1.268	1.249	1.288	1.239	1.298						
	19.4	1.266	1.246	1.286	1.236	1.296						
	20.4	1.263	1.243	1.283	1.233	1.293						
	21.3	1.260	1.240	1.280	1.230	1.290						
	22.2	1.257	1.237	1.277	1.227	1.287						
	23.1	1.255	1.235	1.274	1.225	1.284						
	24.1	1.252	1.232	1.272	1.222	1.282						
	25.0	**1.249**	**1.229**	**1.269**	**1.219**	**1.279**						

Figure 3-3. Illustration of Active State V_{CC} Static and Ripple Tolerances (HFM- VID#B)

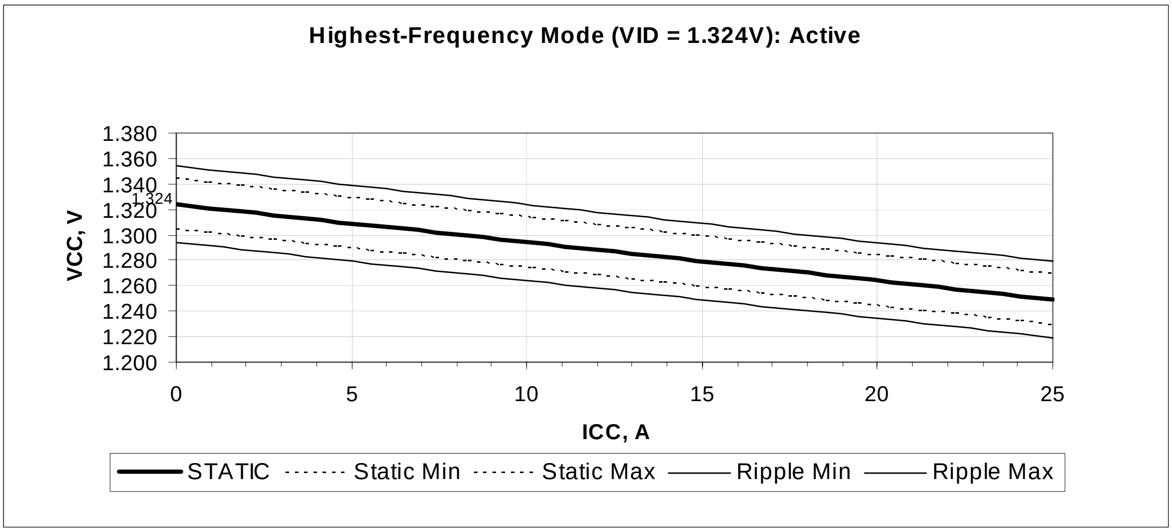


Table 3-11. Voltage Tolerances for the Intel® Pentium® M Processor (Deep Sleep State) VID#B

MODE	Highest Frequency Mode: VID=1.324V, Offset=1.2%						Lowest Frequency Mode: VID=0.988V, Offset=1.2%					
	I_{CC}, A	V_{CC}, V	STATIC		Ripple		I_{CC}, A	V_{CC}, V	STATIC		Ripple	
			Min	Max	Min	Max			Min	Max	Min	Max
Deep Sleep	0.0	1.308	1.288	1.328	1.278	1.338	0.0	0.976	0.961	0.991	0.951	1.001
	0.9	1.305	1.285	1.325	1.275	1.335	0.4	0.975	0.960	0.990	0.950	1.000
	1.9	1.302	1.283	1.322	1.273	1.332	0.8	0.974	0.959	0.989	0.949	0.999
	2.8	1.300	1.280	1.319	1.270	1.329	1.2	0.973	0.958	0.987	0.948	0.997
	3.8	1.297	1.277	1.317	1.267	1.327	1.5	0.972	0.957	0.986	0.947	0.996
	4.7	1.294	1.274	1.314	1.264	1.324	1.9	0.970	0.956	0.985	0.946	0.995
	5.7	1.291	1.271	1.311	1.261	1.321	2.3	0.969	0.954	0.984	0.944	0.994
	6.6	1.288	1.268	1.308	1.258	1.318	2.7	0.968	0.953	0.983	0.943	0.993
	7.6	1.285	1.266	1.305	1.256	1.315	3.1	0.967	0.952	0.982	0.942	0.992
	8.5	1.283	1.263	1.302	1.253	1.312	3.5	0.966	0.951	0.981	0.941	0.991
	9.5	1.280	1.260	1.300	1.250	1.310	3.9	0.965	0.950	0.979	0.940	0.989
	10.4	1.277	1.257	1.297	1.247	1.307	4.3	0.963	0.949	0.978	0.939	0.988
	11.4	1.274	1.254	1.294	1.244	1.304	4.6	0.962	0.947	0.977	0.937	0.987
	12.3	1.271	1.251	1.291	1.241	1.301	5.0	0.961	0.946	0.976	0.936	0.986
	13.3	1.268	1.248	1.288	1.238	1.298	5.4	0.960	0.945	0.975	0.935	0.985
	14.2	**1.266**	**1.246**	**1.285**	**1.236**	**1.295**	**5.8**	**0.959**	**0.944**	**0.974**	**0.934**	**0.984**

Figure 3-4. Illustration of Deep Sleep State V_{CC} Static and Ripple Tolerances (LFM- VID#B)

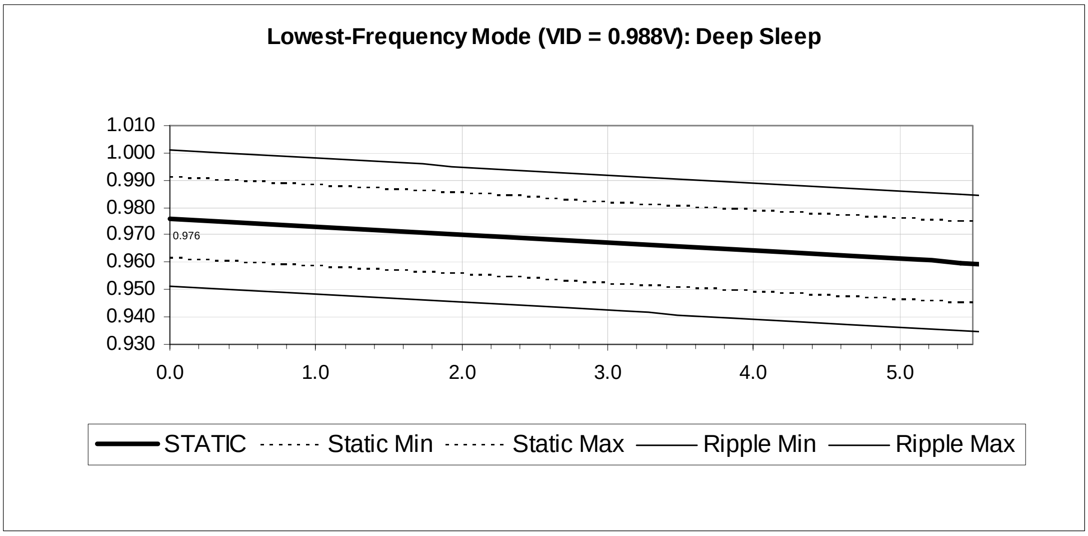


Table 3-12. Voltage Tolerances for the Intel® Pentium® M Processor (Active State) VID#C

MODE	Highest Frequency Mode: VID=1.308V, Offset=0%						Lowest Frequency Mode: VID=0.988V, Offset=0%					
	I_{CC}, A	V_{CC}, V	STATIC		Ripple		I_{CC}, A	V_{CC}, V	STATIC		Ripple	
			Min	Max	Min	Max			Min	Max	Min	Max
ACTIVE	0	1.308	1.288	1.328	1.278	1.338	0.0	0.988	0.973	1.003	0.963	1.013
	0.9	1.305	1.286	1.325	1.276	1.335	0.4	0.987	0.972	1.002	0.962	1.012
	1.9	1.302	1.283	1.322	1.273	1.332	0.9	0.985	0.971	1.000	0.961	1.010
	2.8	1.300	1.280	1.319	1.270	1.329	1.3	0.984	0.969	0.999	0.959	1.009
	3.7	1.297	1.277	1.317	1.267	1.327	1.7	0.983	0.968	0.998	0.958	1.008
	4.6	1.294	1.274	1.314	1.264	1.324	2.1	0.982	0.967	0.996	0.957	1.006
	5.6	1.291	1.272	1.311	1.262	1.321	2.6	0.980	0.966	0.995	0.956	1.005
	6.5	1.289	1.269	1.308	1.259	1.318	3.0	0.979	0.964	0.994	0.954	1.004
	7.4	1.286	1.266	1.305	1.256	1.315	3.4	0.978	0.963	0.993	0.953	1.003
	8.3	1.283	1.263	1.303	1.253	1.313	3.8	0.976	0.962	0.991	0.952	1.001
	9.3	1.280	1.261	1.300	1.251	1.310	4.3	0.975	0.960	0.990	0.950	1.000
	10.2	1.277	1.258	1.297	1.248	1.307	4.7	0.974	0.959	0.989	0.949	0.999
	11.1	1.275	1.255	1.294	1.245	1.304	5.1	0.973	0.958	0.987	0.948	0.997
	12.0	1.272	1.252	1.292	1.242	1.302	5.5	0.971	0.957	0.986	0.947	0.996
	13.0	1.269	1.249	1.289	1.239	1.299	6.0	0.970	0.955	0.985	0.945	0.995
	13.9	1.266	1.247	1.286	1.237	1.296	6.4	0.969	0.954	0.984	0.944	0.994
	14.8	1.264	1.244	1.283	1.234	1.293	6.8	0.968	0.953	0.982	0.943	0.992
	15.7	1.261	1.241	1.280	1.231	1.290	7.2	0.966	0.951	0.981	0.941	0.991
	16.7	1.258	1.238	1.278	1.228	1.288	7.7	0.965	0.950	0.980	0.940	0.990
	17.6	1.255	1.236	1.275	1.226	1.285	**8.1**	**0.964**	**0.949**	**0.979**	**0.939**	**0.989**
	18.5	1.252	1.233	1.272	1.223	1.282						
	19.4	1.250	1.230	1.269	1.220	1.279						
	20.4	1.247	1.227	1.267	1.217	1.277						
	21.3	1.244	1.224	1.264	1.214	1.274						
	22.2	1.241	1.222	1.261	1.212	1.271						
	23.1	1.239	1.219	1.258	1.209	1.268						
	24.1	1.236	1.216	1.255	1.206	1.265						
	25.0	**1.233**	**1.213**	**1.253**	**1.203**	**1.263**						

Figure 3-5. Illustration of Active State V_{CC} Static and Ripple Tolerances (HFM- VID#C)

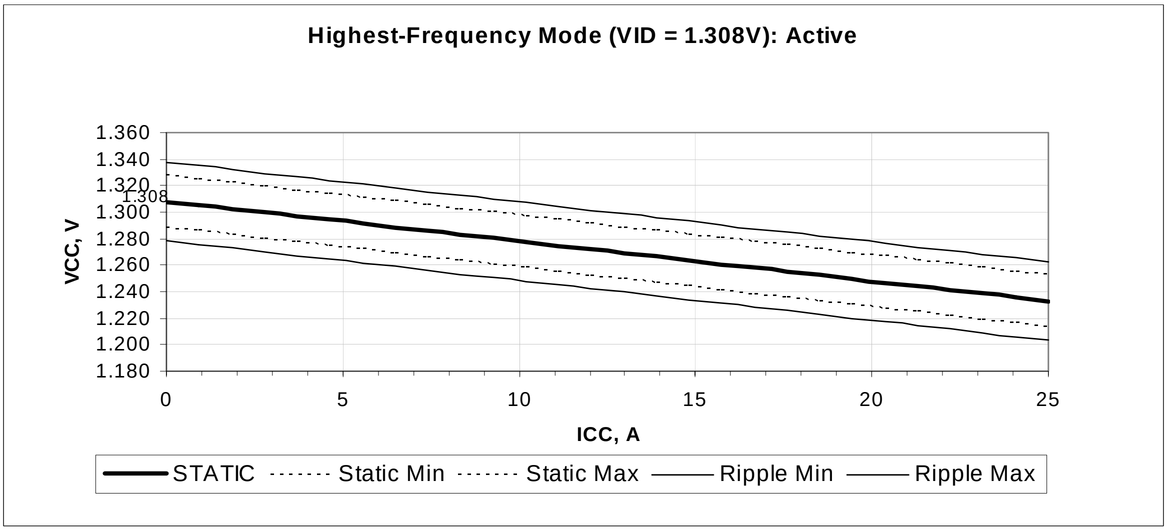


Table 3-13. Voltage Tolerances for the Intel® Pentium® M Processor (Deep Sleep State) VID#C

MODE	Highest Frequency Mode: VID=1.308V, Offset=-1.2%						Lowest Frequency Mode: VID=0.988V, Offset=-1.2%					
	I_{CC}, A	V_{CC}, V	STATIC		Ripple		I_{CC}, A	V_{CC}, V	STATIC		Ripple	
			Min	Max	Min	Max			Min	Max	Min	Max
Deep Sleep	0.0	1.292	1.273	1.312	1.263	1.322	0.0	0.976	0.961	0.991	0.951	1.001
	0.9	1.289	1.270	1.309	1.260	1.319	0.4	0.975	0.960	0.990	0.950	1.000
	1.9	1.287	1.267	1.306	1.257	1.316	0.8	0.974	0.959	0.989	0.949	0.999
	2.8	1.284	1.264	1.303	1.254	1.313	1.2	0.973	0.958	0.987	0.948	0.997
	3.8	1.281	1.261	1.301	1.251	1.311	1.5	0.972	0.957	0.986	0.947	0.996
	4.7	1.278	1.258	1.298	1.248	1.308	1.9	0.970	0.956	0.985	0.946	0.995
	5.7	1.275	1.256	1.295	1.246	1.305	2.3	0.969	0.954	0.984	0.944	0.994
	6.6	1.272	1.253	1.292	1.243	1.302	2.7	0.968	0.953	0.983	0.943	0.993
	7.6	1.270	1.250	1.289	1.240	1.299	3.1	0.967	0.952	0.982	0.942	0.992
	8.5	1.267	1.247	1.286	1.237	1.296	3.5	0.966	0.951	0.981	0.941	0.991
	9.5	1.264	1.244	1.284	1.234	1.294	3.9	0.965	0.950	0.979	0.940	0.989
	10.4	1.261	1.241	1.281	1.231	1.291	4.3	0.963	0.949	0.978	0.939	0.988
	11.4	1.258	1.239	1.278	1.229	1.288	4.6	0.962	0.947	0.977	0.937	0.987
	12.3	1.255	1.236	1.275	1.226	1.285	5.0	0.961	0.946	0.976	0.936	0.986
	13.3	1.253	1.233	1.272	1.223	1.282	5.4	0.960	0.945	0.975	0.935	0.985
	14.2	**1.250**	**1.230**	**1.269**	**1.220**	**1.279**	**5.8**	**0.959**	**0.944**	**0.974**	**0.934**	**0.984**

Figure 3-6. Illustration of Deep Sleep State V_{CC} Static and Ripple Tolerances (LFM- VID#C)

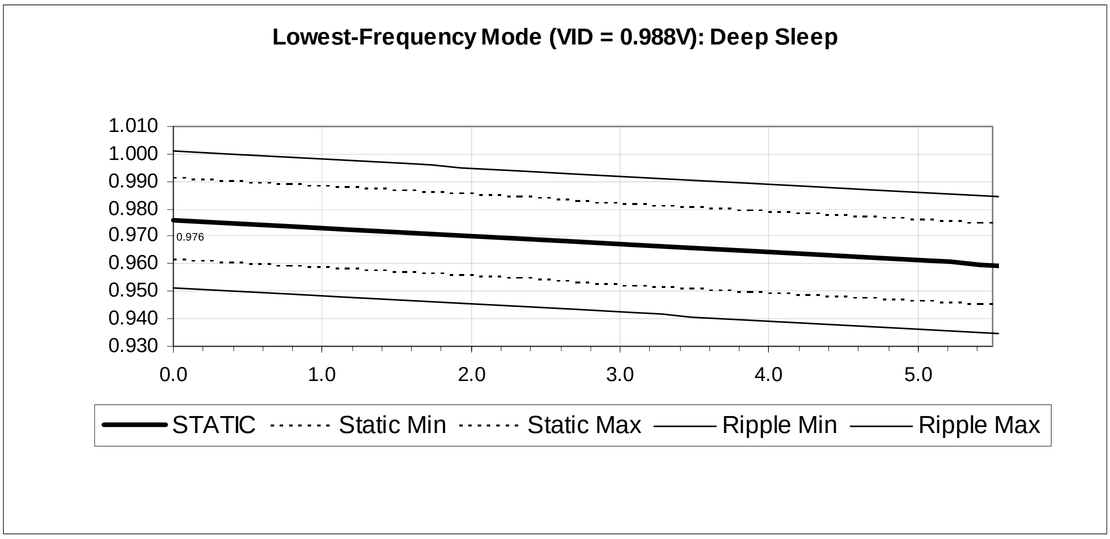


Table 3-14. Voltage Tolerances for the Intel® Pentium® M Processor (Active State) VID#D

MODE	Highest Frequency Mode: VID=1.276V, Offset=0%						Lowest Frequency Mode: VID=0.988V, Offset=0%					
	I_{CC}, A	V_{CC}, V	STATIC		Ripple		I_{CC}, A	V_{CC}, V	STATIC		Ripple	
			Min	Max	Min	Max			Min	Max	Min	Max
ACTIVE	0	1.276	1.257	1.295	1.247	1.305	0.0	0.988	0.973	1.003	0.963	1.013
	0.9	1.273	1.254	1.292	1.244	1.302	0.4	0.987	0.972	1.002	0.962	1.012
	1.9	1.270	1.251	1.290	1.241	1.300	0.9	0.985	0.971	1.000	0.961	1.010
	2.8	1.268	1.249	1.287	1.239	1.297	1.3	0.984	0.969	0.999	0.959	1.009
	3.7	1.265	1.246	1.284	1.236	1.294	1.7	0.983	0.968	0.998	0.958	1.008
	4.6	1.262	1.243	1.281	1.233	1.291	2.1	0.982	0.967	0.996	0.957	1.006
	5.6	1.259	1.240	1.278	1.230	1.288	2.6	0.980	0.966	0.995	0.956	1.005
	6.5	1.257	1.237	1.276	1.227	1.286	3.0	0.979	0.964	0.994	0.954	1.004
	7.4	1.254	1.235	1.273	1.225	1.283	3.4	0.978	0.963	0.993	0.953	1.003
	8.3	1.251	1.232	1.270	1.222	1.280	3.8	0.976	0.962	0.991	0.952	1.001
	9.3	1.248	1.229	1.267	1.219	1.277	4.3	0.975	0.960	0.990	0.950	1.000
	10.2	1.245	1.226	1.265	1.216	1.275	4.7	0.974	0.959	0.989	0.949	0.999
	11.1	1.243	1.224	1.262	1.214	1.272	5.1	0.973	0.958	0.987	0.948	0.997
	12.0	1.240	1.221	1.259	1.211	1.269	5.5	0.971	0.957	0.986	0.947	0.996
	13.0	1.237	1.218	1.256	1.208	1.266	6.0	0.970	0.955	0.985	0.945	0.995
	13.9	1.234	1.215	1.253	1.205	1.263	6.4	0.969	0.954	0.984	0.944	0.994
	14.8	1.232	1.212	1.251	1.202	1.261	6.8	0.968	0.953	0.982	0.943	0.992
	15.7	1.229	1.210	1.248	1.200	1.258	7.2	0.966	0.951	0.981	0.941	0.991
	16.7	1.226	1.207	1.245	1.197	1.255	7.7	0.965	0.950	0.980	0.940	0.990
	17.6	1.223	1.204	1.242	1.194	1.252	**8.1**	**0.964**	**0.949**	**0.979**	**0.939**	**0.989**
	18.5	1.220	1.201	1.240	1.191	1.250						
	19.4	1.218	1.199	1.237	1.189	1.247						
	20.4	1.215	1.196	1.234	1.186	1.244						
	21.3	1.212	1.193	1.231	1.183	1.241						
	22.2	1.209	1.190	1.228	1.180	1.238						
	23.1	1.207	1.187	1.226	1.177	1.236						
	24.1	1.204	1.185	1.223	1.175	1.233						
	25.0	**1.201**	**1.182**	**1.220**	**1.172**	**1.230**						

Figure 3-7. Illustration of Active State V_{CC} Static and Ripple Tolerances (HFM- VID#D)

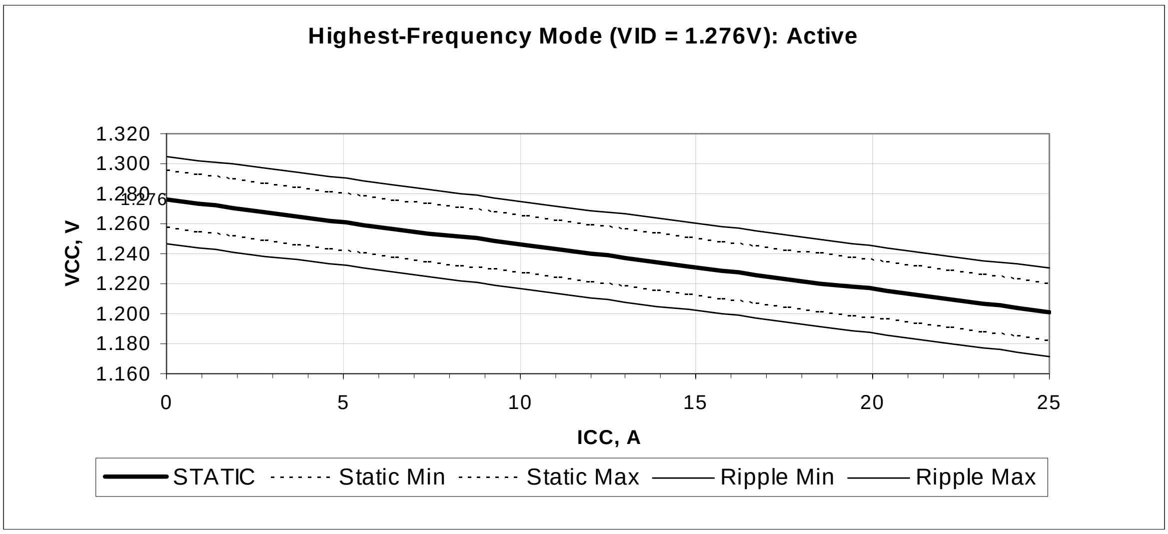


Table 3-15. Voltage Tolerances for the Intel® Pentium® M Processor (Deep Sleep State) VID#D

MODE	Highest Frequency Mode: VID=1.276V, Offset=-1.2%						Lowest Frequency Mode: VID=0.988V, Offset=-1.2%					
	I_{CC}, A	V_{CC}, V	STATIC		Ripple		I_{CC}, A	V_{CC}, V	STATIC		Ripple	
			Min	Max	Min	Max			Min	Max	Min	Max
Deep Sleep	0.0	1.261	1.242	1.280	1.232	1.290	0.0	0.976	0.961	0.991	0.951	1.001
	0.9	1.258	1.239	1.277	1.229	1.287	0.4	0.975	0.960	0.990	0.950	1.000
	1.9	1.255	1.236	1.274	1.226	1.284	0.8	0.974	0.959	0.989	0.949	0.999
	2.8	1.252	1.233	1.271	1.223	1.281	1.2	0.973	0.958	0.987	0.948	0.997
	3.8	1.249	1.230	1.268	1.220	1.278	1.5	0.972	0.957	0.986	0.947	0.996
	4.7	1.246	1.227	1.266	1.217	1.276	1.9	0.970	0.956	0.985	0.946	0.995
	5.7	1.244	1.225	1.263	1.215	1.273	2.3	0.969	0.954	0.984	0.944	0.994
	6.6	1.241	1.222	1.260	1.212	1.270	2.7	0.968	0.953	0.983	0.943	0.993
	7.6	1.238	1.219	1.257	1.209	1.267	3.1	0.967	0.952	0.982	0.942	0.992
	8.5	1.235	1.216	1.254	1.206	1.264	3.5	0.966	0.951	0.981	0.941	0.991
	9.5	1.232	1.213	1.251	1.203	1.261	3.9	0.965	0.950	0.979	0.940	0.989
	10.4	1.229	1.210	1.249	1.200	1.259	4.3	0.963	0.949	0.978	0.939	0.988
	11.4	1.227	1.207	1.246	1.197	1.256	4.6	0.962	0.947	0.977	0.937	0.987
	12.3	1.224	1.205	1.243	1.195	1.253	5.0	0.961	0.946	0.976	0.936	0.986
	13.3	1.221	1.202	1.240	1.192	1.250	5.4	0.960	0.945	0.975	0.935	0.985
	14.2	**1.218**	**1.199**	**1.237**	**1.189**	**1.247**	**5.8**	**0.959**	**0.944**	**0.974**	**0.934**	**0.984**

Figure 3-8. Illustration of Deep Sleep State V_{CC} Static and Ripple Tolerances (LFM- VID#D)

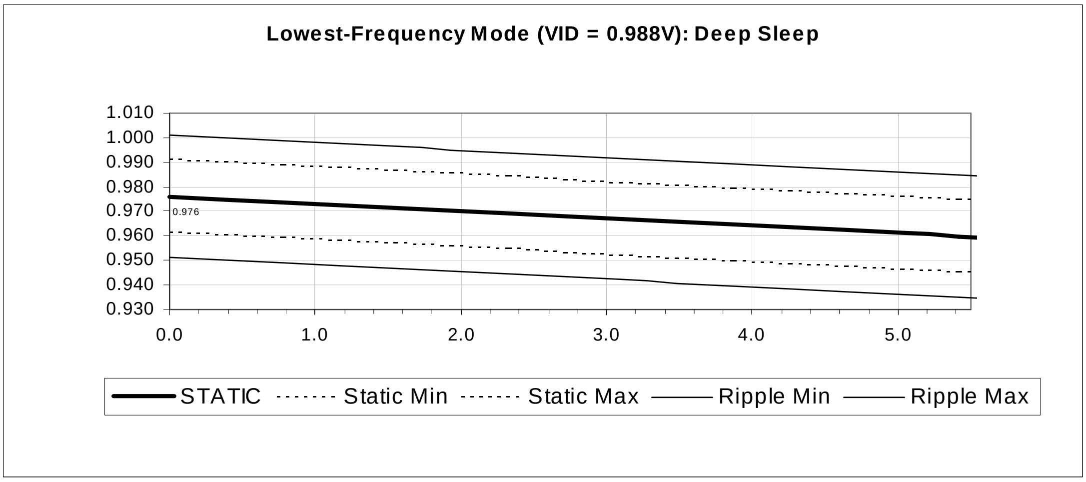


Table 3-16. Voltage Tolerances for the Intel® Pentium® M Processor (Active State) VID#E

MODE	Highest Frequency Mode: VID=1.356V, Offset=0%						Lowest Frequency Mode: VID=0.988V, Offset=0%					
	I_{CC}, A	V_{CC}, V	STATIC		Ripple		I_{CC}, A	V_{CC}, V	STATIC		Ripple	
			Min	Max	Min	Max			Min	Max	Min	Max
ACTIVE	0	1.356	1.336	1.376	1.326	1.386	0.0	0.988	0.973	1.003	0.963	1.013
	0.9	1.353	1.333	1.374	1.323	1.384	0.4	0.987	0.972	1.002	0.962	1.012
	1.9	1.350	1.330	1.371	1.320	1.381	0.9	0.985	0.971	1.000	0.961	1.010
	2.8	1.348	1.327	1.368	1.317	1.378	1.3	0.984	0.969	0.999	0.959	1.009
	3.7	1.345	1.325	1.365	1.315	1.375	1.7	0.983	0.968	0.998	0.958	1.008
	4.6	1.342	1.322	1.362	1.312	1.372	2.1	0.982	0.967	0.996	0.957	1.006
	5.6	1.339	1.319	1.360	1.309	1.370	2.6	0.980	0.966	0.995	0.956	1.005
	6.5	1.337	1.316	1.357	1.306	1.367	3.0	0.979	0.964	0.994	0.954	1.004
	7.4	1.334	1.313	1.354	1.303	1.364	3.4	0.978	0.963	0.993	0.953	1.003
	8.3	1.331	1.311	1.351	1.301	1.361	3.8	0.976	0.962	0.991	0.952	1.001
	9.3	1.328	1.308	1.349	1.298	1.359	4.3	0.975	0.960	0.990	0.950	1.000
	10.2	1.325	1.305	1.346	1.295	1.356	4.7	0.974	0.959	0.989	0.949	0.999
	11.1	1.323	1.302	1.343	1.292	1.353	5.1	0.973	0.958	0.987	0.948	0.997
	12.0	1.320	1.300	1.340	1.290	1.350	5.5	0.971	0.957	0.986	0.947	0.996
	13.0	1.317	1.297	1.337	1.287	1.347	6.0	0.970	0.955	0.985	0.945	0.995
	13.9	1.314	1.294	1.335	1.284	1.345	6.4	0.969	0.954	0.984	0.944	0.994
	14.8	1.312	1.291	1.332	1.281	1.342	6.8	0.968	0.953	0.982	0.943	0.992
	15.7	1.309	1.288	1.329	1.278	1.339	7.2	0.966	0.951	0.981	0.941	0.991
	16.7	1.306	1.286	1.326	1.276	1.336	7.7	0.965	0.950	0.980	0.940	0.990
	17.6	1.303	1.283	1.324	1.273	1.334	**8.1**	**0.964**	**0.949**	**0.979**	**0.939**	**0.989**
	18.5	1.300	1.280	1.321	1.270	1.331						
	19.4	1.298	1.277	1.318	1.267	1.328						
	20.4	1.295	1.275	1.315	1.265	1.325						
	21.3	1.292	1.272	1.312	1.262	1.322						
	22.2	1.289	1.269	1.310	1.259	1.320						
	23.1	1.287	1.266	1.307	1.256	1.317						
	24.1	1.284	1.263	1.304	1.253	1.314						
	25.0	**1.281**	**1.261**	**1.301**	**1.251**	**1.311**						

Figure 3-9. Illustration of Active State V_{CC} Static and Ripple Tolerances (HFM- VID#E)

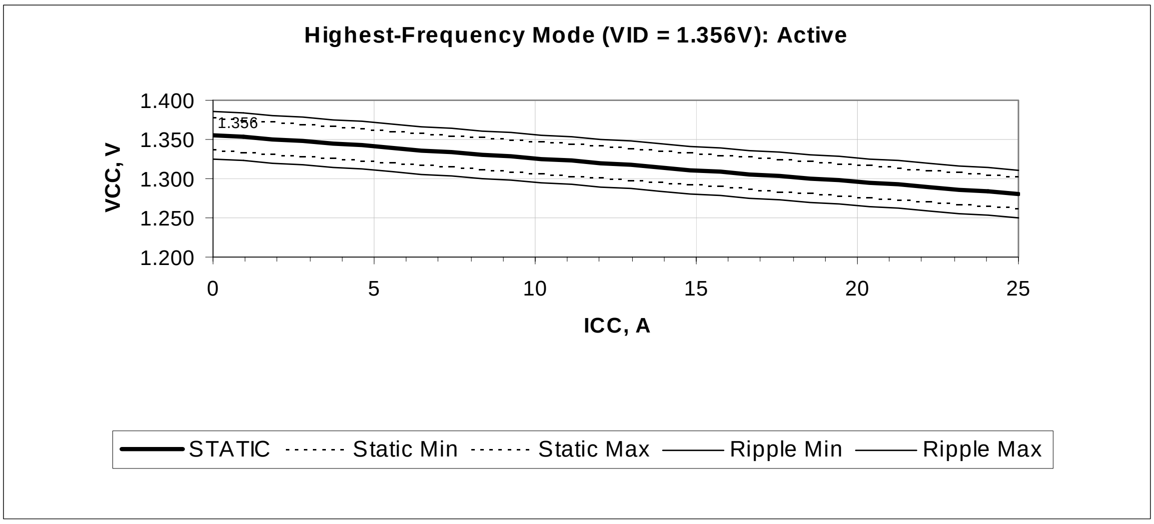


Table 3-17. Voltage Tolerances for the Intel® Pentium® M Processor (Deep Sleep State) VID#E

MODE	Highest Frequency Mode: VID=1.356V, Offset=-1.2%						Lowest Frequency Mode: VID=0.988V, Offset=-1.2%					
	I_{CC}, A	V_{CC}, V	STATIC		Ripple		I_{CC}, A	V_{CC}, V	STATIC		Ripple	
			Min	Max	Min	Max			Min	Max	Min	Max
Deep Sleep	0.0	1.340	1.319	1.360	1.309	1.370	0.0	0.976	0.961	0.991	0.951	1.001
	0.9	1.337	1.317	1.357	1.307	1.367	0.4	0.975	0.960	0.990	0.950	1.000
	1.9	1.334	1.314	1.354	1.304	1.364	0.8	0.974	0.959	0.989	0.949	0.999
	2.8	1.331	1.311	1.352	1.301	1.362	1.2	0.973	0.958	0.987	0.948	0.997
	3.8	1.328	1.308	1.349	1.298	1.359	1.5	0.972	0.957	0.986	0.947	0.996
	4.7	1.326	1.305	1.346	1.295	1.356	1.9	0.970	0.956	0.985	0.946	0.995
	5.7	1.323	1.302	1.343	1.292	1.353	2.3	0.969	0.954	0.984	0.944	0.994
	6.6	1.320	1.300	1.340	1.290	1.350	2.7	0.968	0.953	0.983	0.943	0.993
	7.6	1.317	1.297	1.337	1.287	1.347	3.1	0.967	0.952	0.982	0.942	0.992
	8.5	1.314	1.294	1.335	1.284	1.345	3.5	0.966	0.951	0.981	0.941	0.991
	9.5	1.311	1.291	1.332	1.281	1.342	3.9	0.965	0.950	0.979	0.940	0.989
	10.4	1.308	1.288	1.329	1.278	1.339	4.3	0.963	0.949	0.978	0.939	0.988
	11.4	1.306	1.285	1.326	1.275	1.336	4.6	0.962	0.947	0.977	0.937	0.987
	12.3	1.303	1.282	1.323	1.272	1.333	5.0	0.961	0.946	0.976	0.936	0.986
	13.3	1.300	1.280	1.320	1.270	1.330	5.4	0.960	0.945	0.975	0.935	0.985
	14.2	**1.297**	**1.277**	**1.317**	**1.267**	**1.327**	**5.8**	**0.959**	**0.944**	**0.974**	**0.934**	**0.984**

Figure 3-10. Illustration of Deep Sleep State V_{CC} Static and Ripple Tolerances (LFM- VID#E)

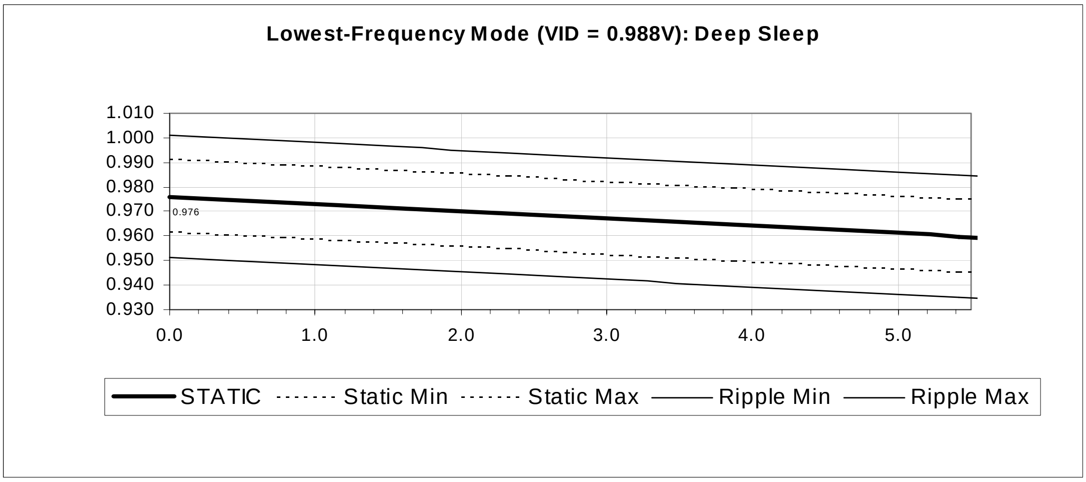


Table 3-18. Voltage Tolerances for the Intel® Pentium® M Processor LV (Active State)

MODE	Highest Frequency Mode: VID=1.116V, Offset=0%						Lowest Frequency Mode: VID=0.988V, Offset=0%					
	I_{CC}, A	V_{CC}, V	STATIC		Ripple		I_{CC}, A	V_{CC}, V	STATIC		Ripple	
			Min	Max	Min	Max			Min	Max	Min	Max
ACTIVE	0	1.116	1.099	1.133	1.089	1.143	0.0	0.988	0.973	1.003	0.963	1.013
	0.4	1.115	1.098	1.131	1.088	1.141	0.4	0.987	0.972	1.002	0.962	1.012
	0.9	1.113	1.097	1.130	1.087	1.140	0.9	0.985	0.971	1.000	0.961	1.010
	1.3	1.112	1.095	1.129	1.085	1.139	1.3	0.984	0.969	0.999	0.959	1.009
	1.8	1.111	1.094	1.127	1.084	1.137	1.7	0.983	0.968	0.998	0.958	1.008
	2.2	1.109	1.093	1.126	1.083	1.136	2.1	0.982	0.967	0.996	0.957	1.006
	2.7	1.108	1.091	1.125	1.081	1.135	2.6	0.980	0.966	0.995	0.956	1.005
	3.1	1.107	1.090	1.123	1.080	1.133	3.0	0.979	0.964	0.994	0.954	1.004
	3.6	1.105	1.089	1.122	1.079	1.132	3.4	0.978	0.963	0.993	0.953	1.003
	4.0	1.104	1.087	1.121	1.077	1.131	3.8	0.976	0.962	0.991	0.952	1.001
	4.4	1.103	1.086	1.119	1.076	1.129	4.3	0.975	0.960	0.990	0.950	1.000
	4.9	1.101	1.085	1.118	1.075	1.128	4.7	0.974	0.959	0.989	0.949	0.999
	5.3	1.100	1.083	1.117	1.073	1.127	5.1	0.973	0.958	0.987	0.948	0.997
	5.8	1.099	1.082	1.115	1.072	1.125	5.5	0.971	0.957	0.986	0.947	0.996
	6.2	1.097	1.081	1.114	1.071	1.124	6.0	0.970	0.955	0.985	0.945	0.995
	6.7	1.096	1.079	1.113	1.069	1.123	6.4	0.969	0.954	0.984	0.944	0.994
	7.1	1.095	1.078	1.111	1.068	1.121	6.8	0.968	0.953	0.982	0.943	0.992
	7.6	1.093	1.077	1.110	1.067	1.120	7.2	0.966	0.951	0.981	0.941	0.991
	8.0	1.092	1.075	1.109	1.065	1.119	7.7	0.965	0.950	0.980	0.940	0.990
	8.4	1.091	1.074	1.107	1.064	1.117	**8.1**	**0.964**	**0.949**	**0.979**	**0.939**	**0.989**
	8.9	1.089	1.073	1.106	1.063	1.116						
	9.3	1.088	1.071	1.105	1.061	1.115						
	9.8	1.087	1.070	1.103	1.060	1.113						
	10.2	1.085	1.069	1.102	1.059	1.112						
	10.7	1.084	1.067	1.101	1.057	1.111						
	11.1	1.083	1.066	1.099	1.056	1.109						
	11.6	1.081	1.065	1.098	1.055	1.108						
	12.0	**1.080**	**1.063**	**1.097**	**1.053**	**1.107**						

Table 3-19. Voltage Tolerances for the Intel® Pentium® M Processor LV (Deep Sleep State)

MODE	Highest Frequency Mode: VID=1.116V, Offset=-1.2%						Lowest Frequency Mode: VID=0.988V, Offset=-1.2%					
	I_{CC}, A	V_{CC}, V	STATIC		Ripple		I_{CC}, A	V_{CC}, V	STATIC		Ripple	
			Min	Max	Min	Max			Min	Max	Min	Max
Deep Sleep	0.0	1.103	1.086	1.119	1.076	1.129	0.0	0.976	0.961	0.991	0.951	1.001
	0.4	1.101	1.085	1.118	1.075	1.128	0.4	0.975	0.960	0.990	0.950	1.000
	0.8	1.100	1.083	1.117	1.073	1.127	0.8	0.974	0.959	0.989	0.949	0.999
	1.2	1.099	1.082	1.116	1.072	1.126	1.2	0.973	0.958	0.987	0.948	0.997
	1.6	1.098	1.081	1.114	1.071	1.124	1.5	0.972	0.957	0.986	0.947	0.996
	2.0	1.097	1.080	1.113	1.070	1.123	1.9	0.970	0.956	0.985	0.946	0.995
	2.4	1.095	1.079	1.112	1.069	1.122	2.3	0.969	0.954	0.984	0.944	0.994
	2.8	1.094	1.077	1.111	1.067	1.121	2.7	0.968	0.953	0.983	0.943	0.993
	3.3	1.093	1.076	1.110	1.066	1.120	3.1	0.967	0.952	0.982	0.942	0.992
	3.7	1.092	1.075	1.108	1.065	1.118	3.5	0.966	0.951	0.981	0.941	0.991
	4.1	1.090	1.074	1.107	1.064	1.117	3.9	0.965	0.950	0.979	0.940	0.989
	4.5	1.089	1.072	1.106	1.062	1.116	4.3	0.963	0.949	0.978	0.939	0.988
	4.9	1.088	1.071	1.105	1.061	1.115	4.6	0.962	0.947	0.977	0.937	0.987
	5.3	1.087	1.070	1.103	1.060	1.113	5.0	0.961	0.946	0.976	0.936	0.986
	5.7	1.086	1.069	1.102	1.059	1.112	5.4	0.960	0.945	0.975	0.935	0.985
	6.1	**1.084**	**1.068**	**1.101**	**1.058**	**1.111**	**5.8**	**0.959**	**0.944**	**0.974**	**0.934**	**0.984**

Table 3-20. Voltage Tolerances for the Intel® Pentium® M Processor ULV (Active State)

MODE	Highest Frequency Mode: VID=0.940V, Offset=0%						Lowest Frequency Mode: VID=0.812V, Offset=0%					
	I_{CC}, A	V_{CC}, V	STATIC		Ripple		I_{CC}, A	V_{CC}, V	STATIC		Ripple	
			Min	Max	Min	Max			Min	Max	Min	Max
ACTIVE	0	0.940	0.926	0.954	0.916	0.964	0.0	0.812	0.799	0.825	0.789	0.835
	0.3	0.939	0.925	0.953	0.915	0.963	0.2	0.811	0.799	0.824	0.789	0.834
	0.5	0.938	0.924	0.953	0.914	0.963	0.4	0.811	0.798	0.823	0.788	0.833
	0.8	0.938	0.924	0.952	0.914	0.962	0.6	0.810	0.797	0.823	0.787	0.833
	1.0	0.937	0.923	0.951	0.913	0.961	0.8	0.809	0.797	0.822	0.787	0.832
	1.3	0.936	0.922	0.950	0.912	0.960	1.1	0.809	0.796	0.822	0.786	0.832
	1.6	0.935	0.921	0.949	0.911	0.959	1.3	0.808	0.796	0.821	0.786	0.831
	1.8	0.935	0.920	0.949	0.910	0.959	1.5	0.808	0.795	0.820	0.785	0.830
	2.1	0.934	0.920	0.948	0.910	0.958	1.7	0.807	0.794	0.820	0.784	0.830
	2.3	0.933	0.919	0.947	0.909	0.957	1.9	0.806	0.794	0.819	0.784	0.829
	2.6	0.932	0.918	0.946	0.908	0.956	2.1	0.806	0.793	0.818	0.783	0.828
	2.9	0.931	0.917	0.946	0.907	0.956	2.3	0.805	0.792	0.818	0.782	0.828
	3.1	0.931	0.917	0.945	0.907	0.955	2.5	0.804	0.792	0.817	0.782	0.827
	3.4	0.930	0.916	0.944	0.906	0.954	2.7	0.804	0.791	0.816	0.781	0.826
	3.6	0.929	0.915	0.943	0.905	0.953	2.9	0.803	0.790	0.816	0.780	0.826
	3.9	0.928	0.914	0.942	0.904	0.952	3.2	0.803	0.790	0.815	0.780	0.825
	4.1	0.928	0.913	0.942	0.903	0.952	3.4	0.802	0.789	0.815	0.779	0.825
	4.4	0.927	0.913	0.941	0.903	0.951	3.6	0.801	0.789	0.814	0.779	0.824
	4.7	0.926	0.912	0.940	0.902	0.950	3.8	0.801	0.788	0.813	0.778	0.823
	4.9	0.925	0.911	0.939	0.901	0.949	**4.0**	**0.800**	**0.787**	**0.813**	**0.777**	**0.823**
	5.2	0.924	0.910	0.939	0.900	0.949						
	5.4	0.924	0.910	0.938	0.900	0.948						
	5.7	0.923	0.909	0.937	0.899	0.947						
	6.0	0.922	0.908	0.936	0.898	0.946						
	6.2	0.921	0.907	0.935	0.897	0.945						
	6.5	0.921	0.906	0.935	0.896	0.945						
	6.7	0.920	0.906	0.934	0.896	0.944						
	7.0	**0.919**	**0.905**	**0.933**	**0.895**	**0.943**						

Table 3-21. Voltage Tolerances for the Intel® Pentium® M Processor ULV (Deep Sleep State)

MODE	Highest Frequency Mode: VID=0.940V, Offset=-1.2%						Lowest Frequency Mode: VID=0.812V, Offset=-1.2%					
	I_{CC}, A	V_{CC}, V	STATIC		Ripple		I_{CC}, A	V_{CC}, V	STATIC		Ripple	
			Min	Max	Min	Max			Min	Max	Min	Max
Deep Sleep	0.0	0.929	0.915	0.943	0.905	0.953	0.0	0.802	0.758	0.847	0.757	0.848
	0.2	0.928	0.914	0.942	0.904	0.952	0.1	0.802	0.757	0.847	0.756	0.847
	0.4	0.928	0.913	0.942	0.903	0.952	0.3	0.801	0.757	0.846	0.756	0.847
	0.6	0.927	0.913	0.941	0.903	0.951	0.4	0.801	0.756	0.846	0.756	0.847
	0.8	0.926	0.912	0.940	0.902	0.950	0.5	0.801	0.756	0.845	0.755	0.846
	1.0	0.926	0.912	0.940	0.902	0.950	0.7	0.800	0.756	0.845	0.755	0.846
	1.2	0.925	0.911	0.939	0.901	0.949	0.8	0.800	0.755	0.845	0.754	0.845
	1.4	0.925	0.910	0.939	0.900	0.949	0.9	0.799	0.755	0.844	0.754	0.845
	1.6	0.924	0.910	0.938	0.900	0.948	1.1	0.799	0.754	0.844	0.754	0.845
	1.8	0.923	0.909	0.937	0.899	0.947	1.2	0.799	0.754	0.843	0.753	0.844
	2.0	0.923	0.909	0.937	0.899	0.947	1.3	0.798	0.754	0.843	0.753	0.844
	2.2	0.922	0.908	0.936	0.898	0.946	1.5	0.798	0.753	0.843	0.752	0.843
	2.4	0.922	0.907	0.936	0.897	0.946	1.6	0.797	0.753	0.842	0.752	0.843
	2.6	0.921	0.907	0.935	0.897	0.945	1.7	0.797	0.752	0.842	0.752	0.843
	2.8	0.920	0.906	0.934	0.896	0.944	1.9	0.797	0.752	0.841	0.751	0.842
	3.0	**0.920**	**0.906**	**0.934**	**0.896**	**0.944**	**2.0**	**0.796**	**0.752**	**0.841**	**0.751**	**0.842**

Figure 3-11. Active V_{CC} and I_{CC} Load Line

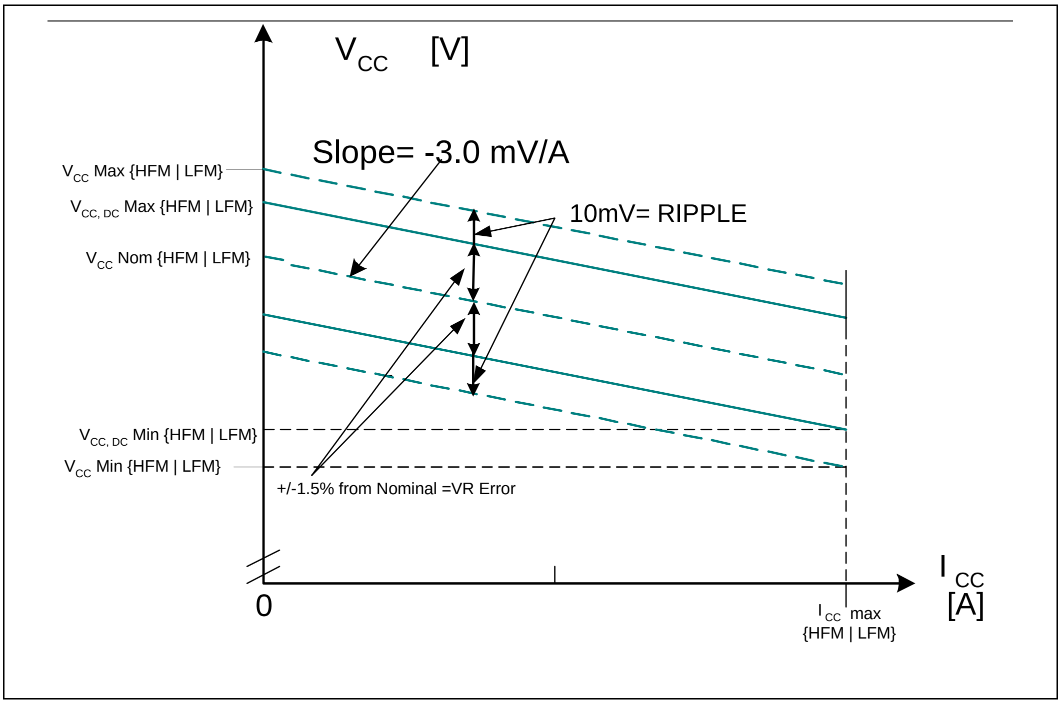


Figure 3-12. Deep Sleep V_{CC} and I_{CC} Load Line

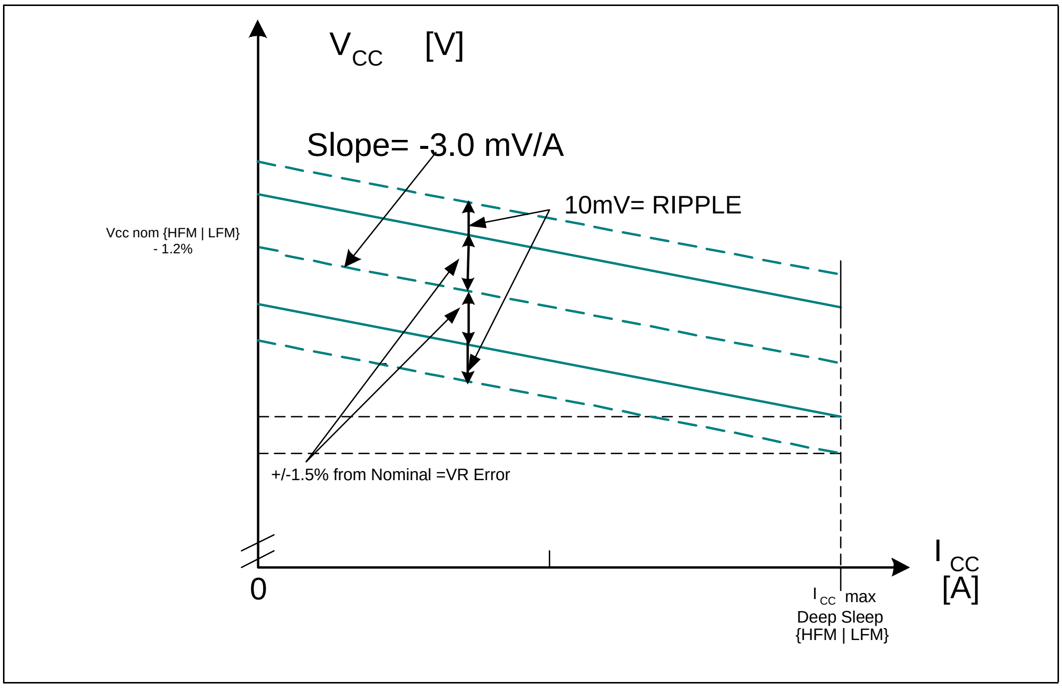


Table 3-22. FSB Differential BCLK Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
V_L	Input Low Voltage		0		V	
V_H	Input High Voltage	0.660	0.710	0.850	V	
V_{CROSS}	Crossing Voltage	0.25	0.35	0.55	V	2
ΔV_{CROSS}	Range of Crossing Points	N/A	N/A	0.140	V	6
V_{TH}	Threshold Region	V_{CROSS} -0.100		V_{CROSS}+0.100	V	3
I_{LI}	Input Leakage Current			± 100	µA	4
Cpad	Pad Capacitance	1.8	2.3	2.75	pF	5

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Crossing Voltage is defined as absolute voltage where rising edge of BCLK0 is equal to the falling edge of BCLK1.
3. Threshold Region is defined as a region entered about the crossing voltage in which the differential receiver switches. It includes input threshold hysteresis.
4. For Vin between 0 V and V_H.
5. Cpad includes die capacitance only. No package parasitics are included.
6. VCROSS is defined as the total variation of all crossing voltages as defined in note 2

Table 3-23. AGTL+ Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
VCCP	I/O Voltage	0.997	1.05	1.102	V	
GTLREF	Reference Voltage	2/3 VCCP - 2%	2/3 VCCP	2/3 VCCP + 2%	V	6
V_{IH}	Input High Voltage	GTLREF+0.1		VCCP+0.1	V	3,6
V_{IL}	Input Low Voltage	-0.1		GTLREF-0.1	V	2,4
V_{OH}	Output High Voltage		VCCP			6
R_{TT}	Termination Resistance	47	55	63	Ω	7
R_{ON}	Buffer On Resistance	17.7	24.7	32.9	Ω	5
I_{LI}	Input Leakage Current			± 100	µA	8
Cpad	Pad Capacitance	1.8	2.3	2.75	pF	9

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
4. V_{IH} and V_{OH} may experience excursions above VCCP. However, input signal drivers must comply with the signal quality specifications in Chapter 3.
5. This is the pull down driver resistance. Refer to processor I/O buffer models for I/V characteristics. Measured at 0.31*VCCP. R_{ON} (min) = 0.38*R_{TT}, R_{ON} (typ) = 0.45*R_{TT}, R_{ON} (max) = 0.52*R_{TT}.
6. GTLREF should be generated from VCCP with a 1% tolerance resistor divider. The VCCP referred to in these specifications is the instantaneous VCCP.
7. R_{TT} is the on-die termination resistance measured at V_{OL} of the AGTL+ output driver. Measured at 0.31*VCCP. R_{TT} is connected to VCCP on die. Refer to processor I/O buffer models for I/V characteristics.
8. Specified with on die R_{TT} and R_{ON} are turned off.
9. Cpad includes die capacitance only. No package parasitics are included.

Table 3-24. CMOS Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
VCCP	I/O Voltage	0.997	1.05	1.102	V	
V_{IL}	Input Low Voltage CMOS	-0.1		0.3*VCCP	V	2, 3
V_{IH}	Input High Voltage	0.7*VCCP		VCCP+0.1	V	2
V_{OL}	Output Low Voltage	-0.1	0	0.1*VCCP	V	2
V_{OH}	Output High Voltage	0.9*VCCP	VCCP	VCCP+0.1	V	2
I_{OL}	Output Low Current	1.49		4.08	mA	4
I_{OH}	Output High Current	1.49		4.08	mA	5
I_{LI}	Leakage Current			± 100	µA	6
Cpad	Pad Capacitance	1.0	2.3	3.0	pF	

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The VCCP referred to in these specifications refers to instantaneous VCCP.
3. Refer to the processor I/O buffer models for I/V characteristics.
4. Measured at 0.1*VCCP.
5. Measured at 0.9*VCCP.
6. For Vin between 0 V and VCCP. Measured when the driver is tristated.
7. Cpad includes die capacitance only. No package parasitics are included

Table 3-25. Open Drain Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
V_{OH}	Output High Voltage		VCCP		V	3
V_{OL}	Output Low Voltage	0		0.20	V	
I_{OL}	Output Low Current	16		50	mA	2
I_{LO}	Leakage Current			± 200	µA	4
Cpad	Pad Capacitance	1.7	2.3	3.0	pF	5

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Measured at 0.2 V.
3. V_{OH} is determined by value of the external pullup resistor to VCCP. Please refer to the platform design guides for details.
4. For Vin between 0 V and V_{OH}.
5. Cpad includes die capacitance only. No package parasitics are included.

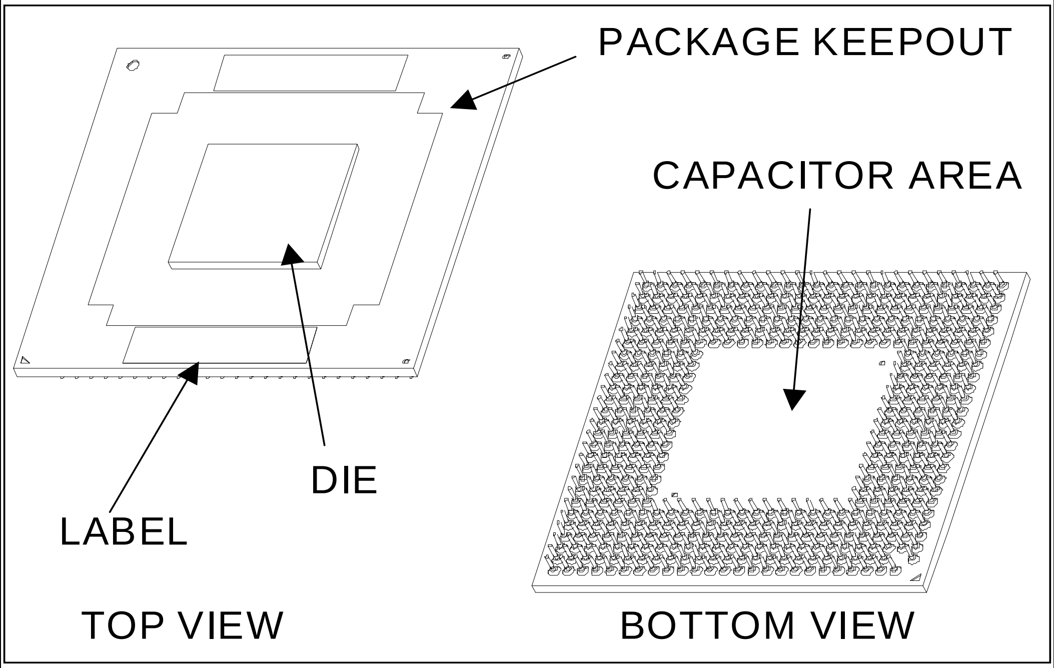
§

4 Package Mechanical Specifications and Pin Information

The Pentium M Processor is available in 478-pin, Micro-FCPGA and 479-ball, Micro-FCBGA packages. Different views of the Micro-FCPGA package are shown in Figure 4-1 through Figure 4-3. Package dimensions are shown in Table 4-1. Different views of the Micro-FCBGA package are shown in Figure 4-4 through Figure 4-6. Package dimensions are shown in Table 4-2.

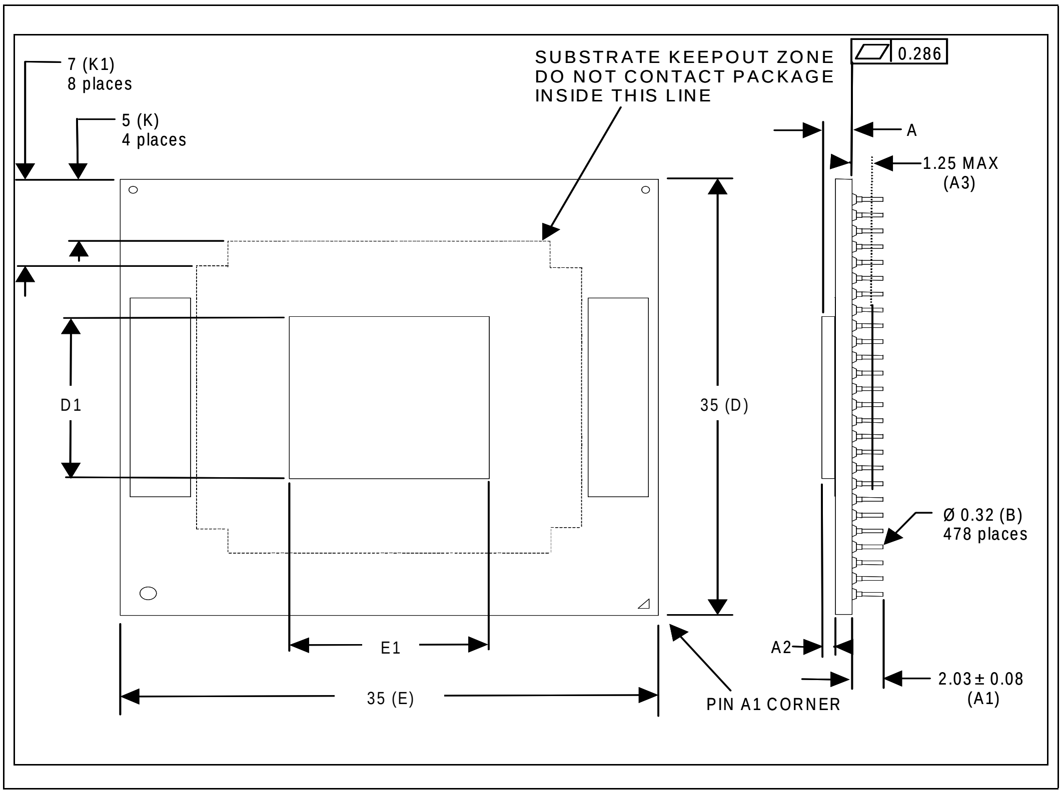
The Micro-FCBGA package may have capacitors placed in the area surrounding the die. Because the die-side capacitors are electrically conductive, and only slightly shorter than the die height, care should be taken to avoid contacting the capacitors with electrically conductive materials. Doing so may short the capacitors, and possibly damage the device or render it inactive. The use of an insulating material between the capacitors and any thermal solution should be considered to prevent capacitor shorting.

Figure 4-1. Micro-FCPGA Package Top and Bottom Isometric Views



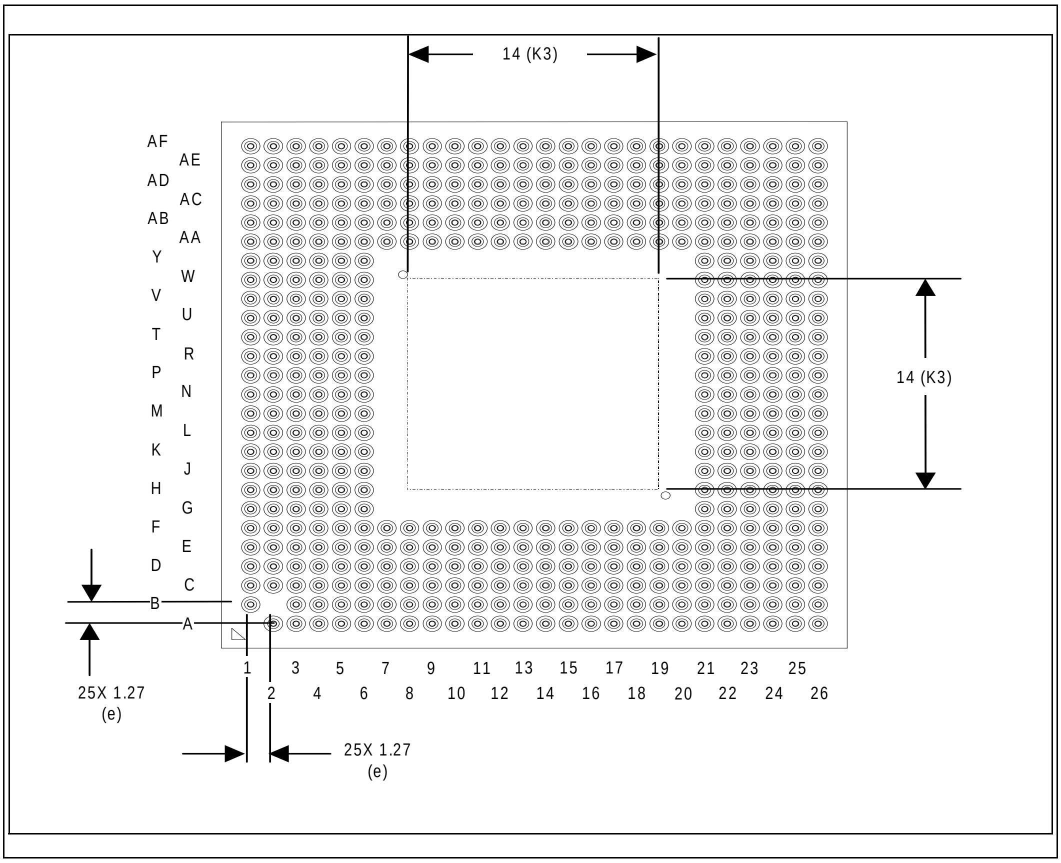
NOTE: All dimensions in millimeters. Values shown for reference only. Refer to Table 4-1 for details.

Figure 4-2. Micro-FCPGA Package - Top and Side Views



NOTE: MDie is centered on the Package. All dimensions in millimeters. Values shown for reference only. Refer to Table 4-1 for details.

Figure 4-3. Micro-FCPGA Package - Bottom View



NOTE: All dimensions in millimeters. Values shown for reference only. Refer to Table 4-1 for details.

Table 4-1. Micro-FCPGA Package Dimensions

Symbol	Parameter	Min	Max	Unit
A	Overall height, top of die to package seating plane	1.88	2.02	mm
–	Overall height, top of die to PCB surface, including socket (Refer to Note 1)	4.74	5.16	mm
A1	Pin length	1.95	2.11	mm
A2	Die height	0.820		mm
A3	Pin-side capacitor height	–	1.25	mm
B	Pin diameter	0.28	0.36	mm
D	Package substrate length	34.9	35.1	mm
E	Package substrate width	34.9	35.1	mm
D1	Die length	12.54		mm
E1	Die width	6.99		mm
e	Pin Pitch	1.27		mm
K	Package edge keep-out	5		mm
K1	Package corner keep-out	7		mm
K3	Pin-side capacitor boundary	14		mm
N	Pin count	478		each
Pdie	Allowable pressure on the die for thermal solution	–	689	kPa
W	Package weight		4.5	g
⏥	Package Surface Flatness	0.286		mm

NOTE: Overall height with socket is based on design dimensions of the Micro-FCPGA package with no thermal solution attached. Values are based on design specifications and tolerances. This dimension is subject to change based on socket design, OEM motherboard design or OEM SMT process.

Figure 4-4. Micro-FCBGA Package Top and Bottom Isometric Views

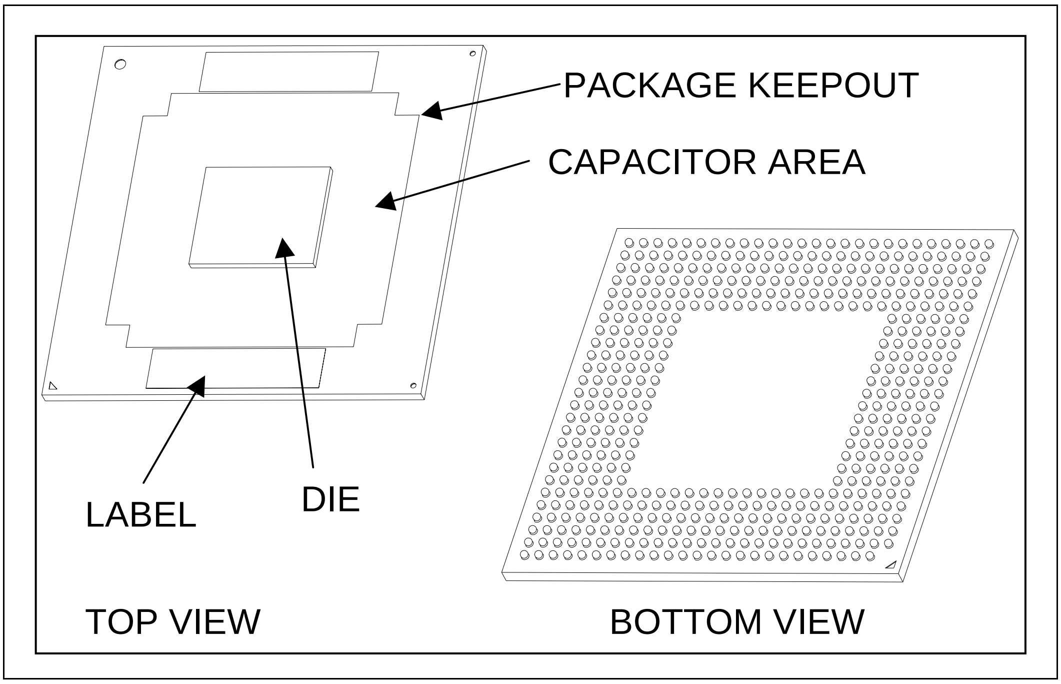
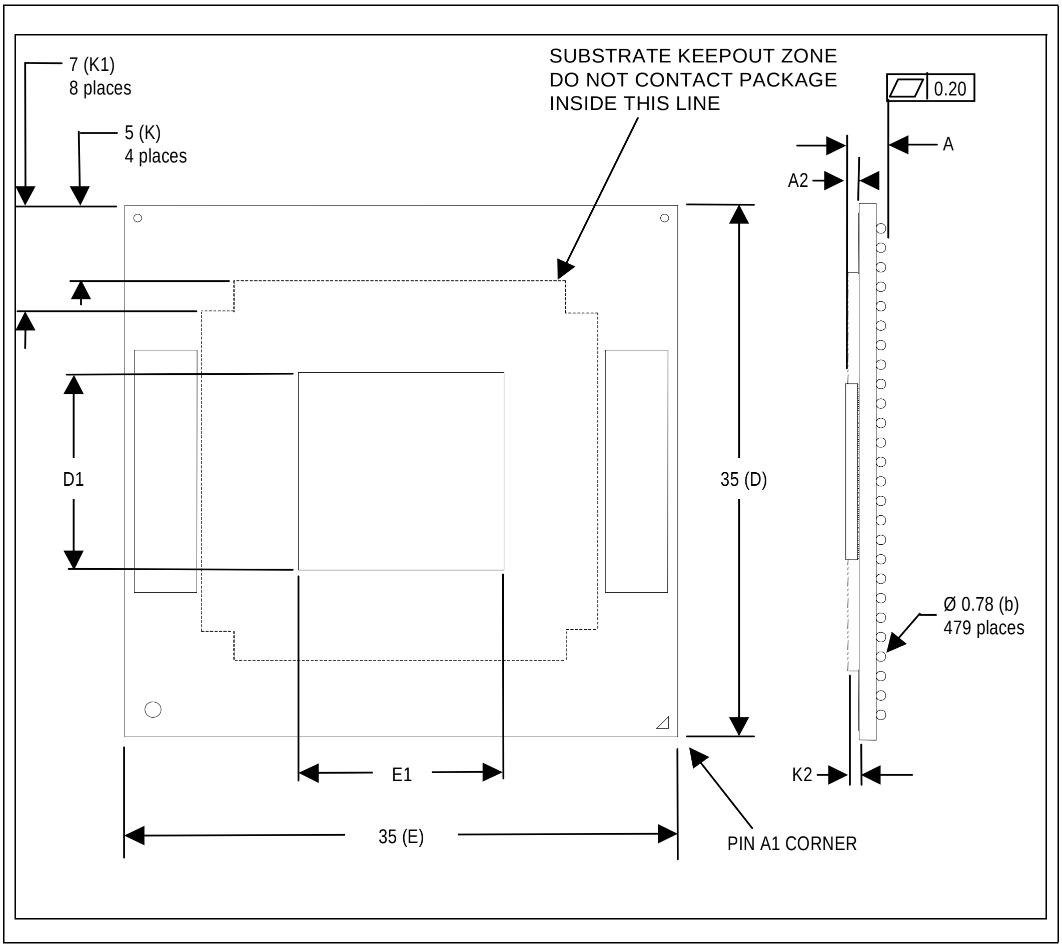


Figure 4-5. Micro-FCBGA Package Top and Side Views



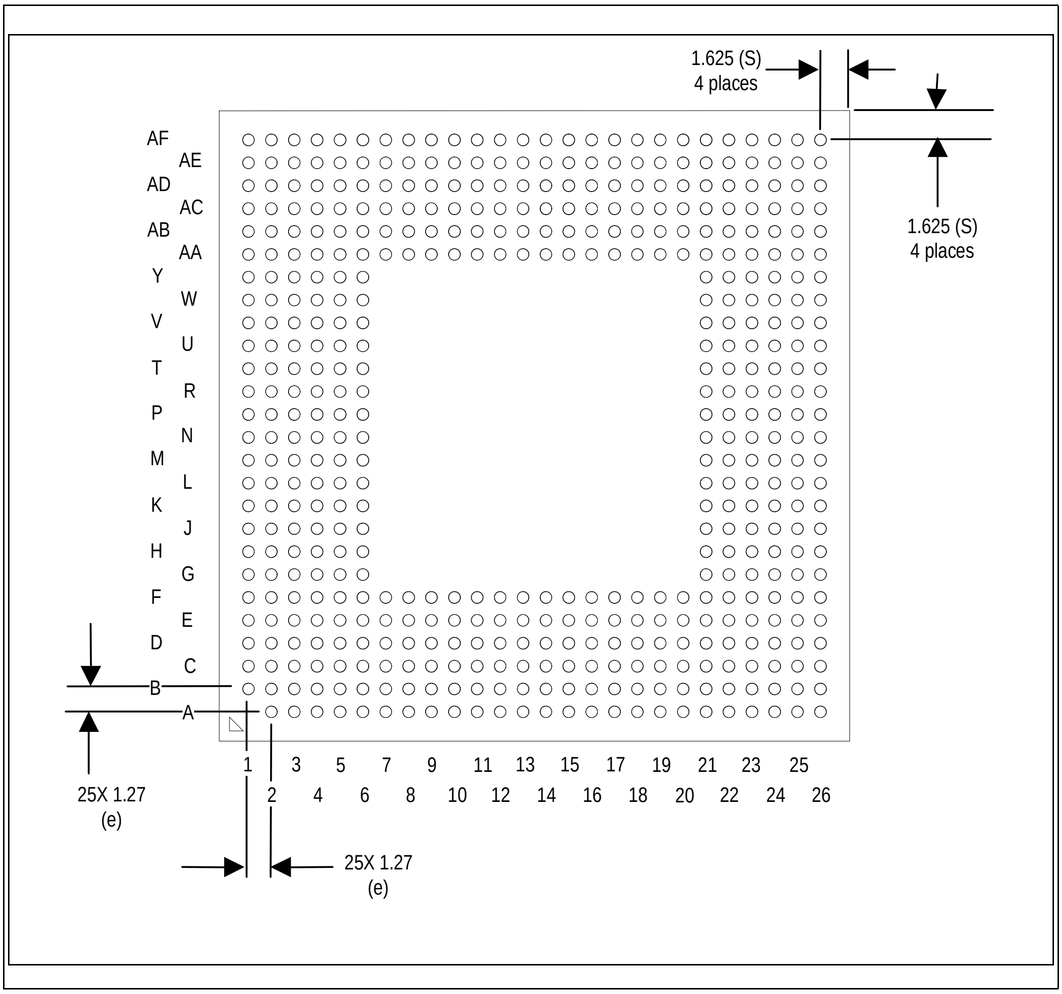
NOTE: Die is centered on the Package. All dimensions in millimeters. Values shown for reference only. Refer to Table 4-2 for details.

Table 4-2. Micro-FCBGA Package Dimensions

Symbol	Parameter	Min	Max	Unit
A	Overall height, as delivered (Refer to Note 1)	2.60	2.85	mm
A2	Die height	0.82		mm
b	Ball diameter	0.78		mm
D	Package substrate length	34.9	35.1	mm
E	Package substrate width	34.9	35.1	mm
D1	Die length	12.54		mm
E1	Die width	6.99		mm
e	Ball Pitch	1.27		mm
K	Package edge keep-out	5		mm
K1	Package corner keep-out	7		mm
K2	Die-side capacitor height	–	0.7	mm
S	Package edge to first ball center	1.625		mm
N	Ball count	479		each
–	Solder ball coplanarity	0.2		mm
Pdie	Allowable pressure on the die for thermal solution	–	689	kPa
W	Package weight		4.5	g

NOTE: Overall height as delivered. Values are based on design specifications and tolerances. This dimension is subject to change based on OEM motherboard design or OEM SMT process.

Figure 4-6. Micro-FCBGA Package Bottom View



NOTE: All dimensions in millimeters. Values shown for reference only. Refer to Table 4-2 for details.

4.1 Processor Pinout and Pin List

Figure 4-7 on the next page shows the top view pinout of the Pentium M Processor. The pin list arranged in two different formats is shown in the following pages.

Figure 4-7. The Coordinates of the Processor Pins as Viewed from the Top of the Package

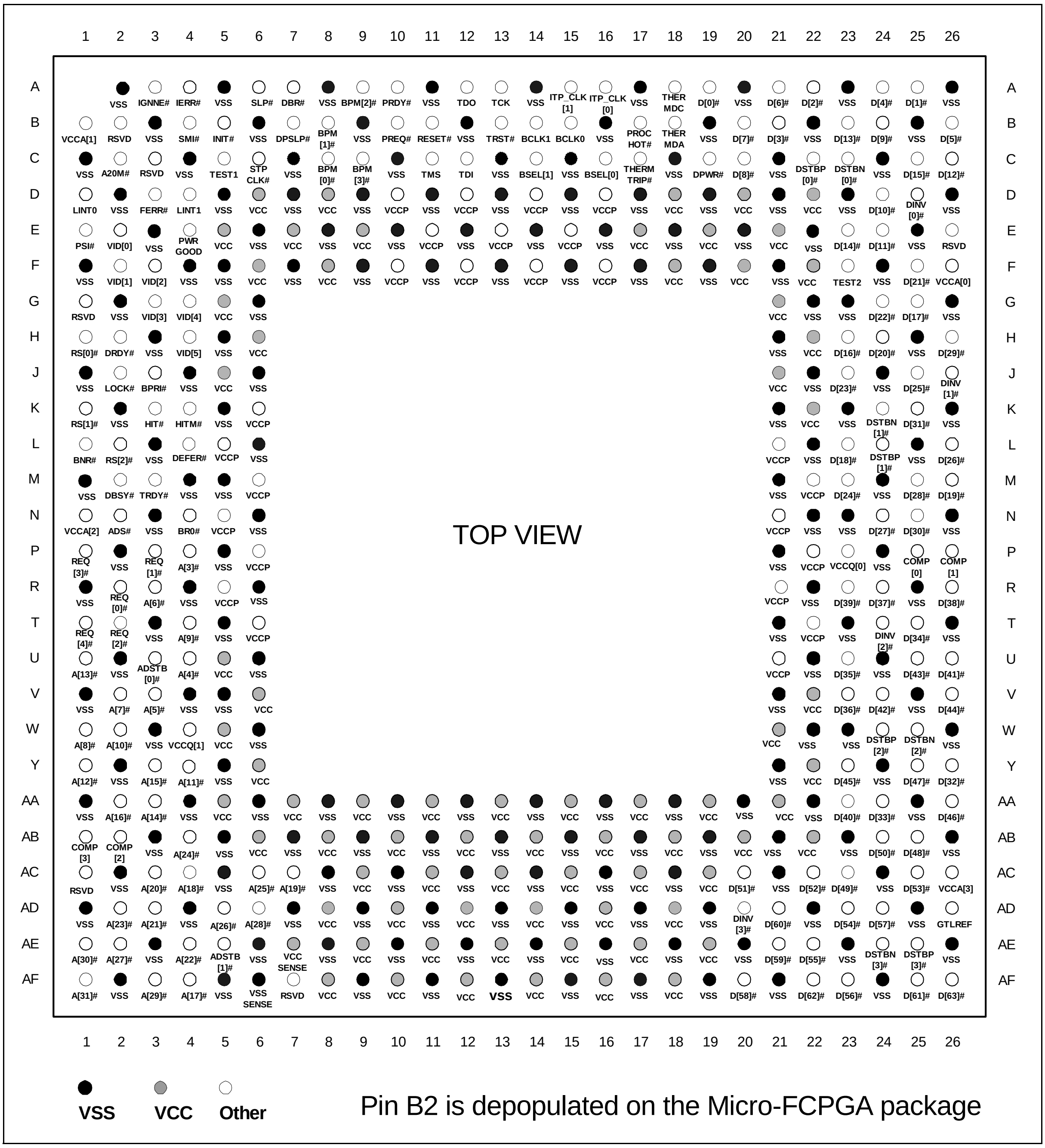


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Table 4-3. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
A[3]#	P4	Source Synch	Input/Output
A[4]#	U4	Source Synch	Input/Output
A[5]#	V3	Source Synch	Input/Output
A[6]#	R3	Source Synch	Input/Output
A[7]#	V2	Source Synch	Input/Output
A[8]#	W1	Source Synch	Input/Output
A[9]#	T4	Source Synch	Input/Output
A[10]#	W2	Source Synch	Input/Output
A[11]#	Y4	Source Synch	Input/Output
A[12]#	Y1	Source Synch	Input/Output
A[13]#	U1	Source Synch	Input/Output
A[14]#	AA3	Source Synch	Input/Output
A[15]#	Y3	Source Synch	Input/Output
A[16]#	AA2	Source Synch	Input/Output
A[17]#	AF4	Source Synch	Input/Output
A[18]#	AC4	Source Synch	Input/Output
A[19]#	AC7	Source Synch	Input/Output
A[20]#	AC3	Source Synch	Input/Output
A[21]#	AD3	Source Synch	Input/Output
A[22]#	AE4	Source Synch	Input/Output
A[23]#	AD2	Source Synch	Input/Output
A[24]#	AB4	Source Synch	Input/Output
A[25]#	AC6	Source Synch	Input/Output
A[26]#	AD5	Source Synch	Input/Output
A[27]#	AE2	Source Synch	Input/Output
A[28]#	AD6	Source Synch	Input/Output
A[29]#	AF3	Source Synch	Input/Output
A[30]#	AE1	Source Synch	Input/Output
A[31]#	AF1	Source Synch	Input/Output
A20M#	C2	CMOS	Input
ADS#	N2	Common Clock	Input/Output
ADSTB[0]#	U3	Source Synch	Input/Output
ADSTB[1]#	AE5	Source Synch	Input/Output
BCLK[0]	B15	Bus Clock	Input
BCLK[1]	B14	Bus Clock	Input
BNR#	L1	Common Clock	Input/Output
BPM[0]#	C8	Common Clock	Output

Table 4-3. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
BPM[1]#	B8	Common Clock	Output
BPM[2]#	A9	Common Clock	Output
BPM[3]#	C9	Common Clock	Input/Output
BPRI#	J3	Common Clock	Input
BR0#	N4	Common Clock	Input/Output
BSEL[1]	C14	CMOS	Output
BSEL[0]	C16	CMOS	Output
COMP[0]	P25	Power/Other	Input/Output
COMP[1]	P26	Power/Other	Input/Output
COMP[2]	AB2	Power/Other	Input/Output
COMP[3]	AB1	Power/Other	Input/Output
D[0]#	A19	Source Synch	Input/Output
D[1]#	A25	Source Synch	Input/Output
D[2]#	A22	Source Synch	Input/Output
D[3]#	B21	Source Synch	Input/Output
D[4]#	A24	Source Synch	Input/Output
D[5]#	B26	Source Synch	Input/Output
D[6]#	A21	Source Synch	Input/Output
D[7]#	B20	Source Synch	Input/Output
D[8]#	C20	Source Synch	Input/Output
D[9]#	B24	Source Synch	Input/Output
D[10]#	D24	Source Synch	Input/Output
D[11]#	E24	Source Synch	Input/Output
D[12]#	C26	Source Synch	Input/Output
D[13]#	B23	Source Synch	Input/Output
D[14]#	E23	Source Synch	Input/Output
D[15]#	C25	Source Synch	Input/Output
D[16]#	H23	Source Synch	Input/Output
D[17]#	G25	Source Synch	Input/Output
D[18]#	L23	Source Synch	Input/Output
D[19]#	M26	Source Synch	Input/Output
D[20]#	H24	Source Synch	Input/Output
D[21]#	F25	Source Synch	Input/Output
D[22]#	G24	Source Synch	Input/Output
D[23]#	J23	Source Synch	Input/Output
D[24]#	M23	Source Synch	Input/Output
D[25]#	J25	Source Synch	Input/Output
D[26]#	L26	Source Synch	Input/Output

Table 4-3. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
D[27]#	N24	Source Synch	Input/Output
D[28]#	M25	Source Synch	Input/Output
D[29]#	H26	Source Synch	Input/Output
D[30]#	N25	Source Synch	Input/Output
D[31]#	K25	Source Synch	Input/Output
D[32]#	Y26	Source Synch	Input/Output
D[33]#	AA24	Source Synch	Input/Output
D[34]#	T25	Source Synch	Input/Output
D[35]#	U23	Source Synch	Input/Output
D[36]#	V23	Source Synch	Input/Output
D[37]#	R24	Source Synch	Input/Output
D[38]#	R26	Source Synch	Input/Output
D[39]#	R23	Source Synch	Input/Output
D[40]#	AA23	Source Synch	Input/Output
D[41]#	U26	Source Synch	Input/Output
D[42]#	V24	Source Synch	Input/Output
D[43]#	U25	Source Synch	Input/Output
D[44]#	V26	Source Synch	Input/Output
D[45]#	Y23	Source Synch	Input/Output
D[46]#	AA26	Source Synch	Input/Output
D[47]#	Y25	Source Synch	Input/Output
D[48]#	AB25	Source Synch	Input/Output
D[49]#	AC23	Source Synch	Input/Output
D[50]#	AB24	Source Synch	Input/Output
D[51]#	AC20	Source Synch	Input/Output
D[52]#	AC22	Source Synch	Input/Output
D[53]#	AC25	Source Synch	Input/Output
D[54]#	AD23	Source Synch	Input/Output
D[55]#	AE22	Source Synch	Input/Output
D[56]#	AF23	Source Synch	Input/Output
D[57]#	AD24	Source Synch	Input/Output
D[58]#	AF20	Source Synch	Input/Output
D[59]#	AE21	Source Synch	Input/Output
D[60]#	AD21	Source Synch	Input/Output
D[61]#	AF25	Source Synch	Input/Output
D[62]#	AF22	Source Synch	Input/Output
D[63]#	AF26	Source Synch	Input/Output
DBR#	A7	CMOS	Output

Table 4-3. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
DBSY#	M2	Common Clock	Input/Output
DEFER#	L4	Common Clock	Input
DINV[0]#	D25	Source Synch	Input/Output
DINV[1]#	J26	Source Synch	Input/Output
DINV[2]#	T24	Source Synch	Input/Output
DINV[3]#	AD20	Source Synch	Input/Output
DPSLP#	B7	CMOS	Input
DPWR#	C19	Common Clock	Input
DRDY#	H2	Common Clock	Input/Output
DSTBN[0]#	C23	Source Synch	Input/Output
DSTBN[1]#	K24	Source Synch	Input/Output
DSTBN[2]#	W25	Source Synch	Input/Output
DSTBN[3]#	AE24	Source Synch	Input/Output
DSTBP[0]#	C22	Source Synch	Input/Output
DSTBP[1]#	L24	Source Synch	Input/Output
DSTBP[2]#	W24	Source Synch	Input/Output
DSTBP[3]#	AE25	Source Synch	Input/Output
FERR#	D3	Open Drain	Output
GTLREF	AD26	Power/Other	Input
HIT#	K3	Common Clock	Input/Output
HITM#	K4	Common Clock	Input/Output
IERR#	A4	Open Drain	Output
IGNNE#	A3	CMOS	Input
INIT#	B5	CMOS	Input
ITP_CLK[0]	A16	CMOS	input
ITP_CLK[1]	A15	CMOS	input
LINT0	D1	CMOS	Input
LINT1	D4	CMOS	Input
LOCK#	J2	Common Clock	Input/Output
PRDY#	A10	Common Clock	Output
PREQ#	B10	Common Clock	Input
PROCHOT#	B17	Open Drain	Output
PSI#	E1	CMOS	Output
PWRGOOD	E4	CMOS	Input
REQ[0]#	R2	Source Synch	Input/Output
REQ[1]#	P3	Source Synch	Input/Output
REQ[2]#	T2	Source Synch	Input/Output
REQ[3]#	P1	Source Synch	Input/Output

Table 4-3. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
REQ[4]#	T1	Source Synch	Input/Output
RESET#	B11	Common Clock	Input
RS[0]#	H1	Common Clock	Input
RS[1]#	K1	Common Clock	Input
RS[2]#	L2	Common Clock	Input
RSVD	AF7	Reserved	
RSVD	B2	Reserved	
RSVD	C3	Reserved	
RSVD	E26	Reserved	
RSVD	G1	Reserved	
RSVD	AC1	Reserved	
SLP#	A6	CMOS	Input
SMI#	B4	CMOS	Input
STPCLK#	C6	CMOS	Input
TCK	A13	CMOS	Input
TDI	C12	CMOS	Input
TDO	A12	Open Drain	Output
TEST1	C5	Test	
TEST2	F23	Test	
THERMDA	B18	Power/Other	
THERMDC	A18	Power/Other	
THERMTRIP#	C17	Open Drain	Output
TMS	C11	CMOS	Input
TRDY#	M3	Common Clock	Input
TRST#	B13	CMOS	Input
VCC	D6	Power/Other	
VCC	D8	Power/Other	
VCC	D18	Power/Other	
VCC	D20	Power/Other	
VCC	D22	Power/Other	
VCC	E5	Power/Other	
VCC	E7	Power/Other	
VCC	E9	Power/Other	
VCC	E17	Power/Other	
VCC	E19	Power/Other	
VCC	E21	Power/Other	
VCC	F6	Power/Other	
VCC	F8	Power/Other	

Table 4-3. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VCC	F18	Power/Other	
VCC	F20	Power/Other	
VCC	F22	Power/Other	
VCC	G5	Power/Other	
VCC	G21	Power/Other	
VCC	H6	Power/Other	
VCC	H22	Power/Other	
VCC	J5	Power/Other	
VCC	J21	Power/Other	
VCC	K22	Power/Other	
VCC	U5	Power/Other	
VCC	V6	Power/Other	
VCC	V22	Power/Other	
VCC	W5	Power/Other	
VCC	W21	Power/Other	
VCC	Y6	Power/Other	
VCC	Y22	Power/Other	
VCC	AA5	Power/Other	
VCC	AA7	Power/Other	
VCC	AA9	Power/Other	
VCC	AA11	Power/Other	
VCC	AA13	Power/Other	
VCC	AA15	Power/Other	
VCC	AA17	Power/Other	
VCC	AA19	Power/Other	
VCC	AA21	Power/Other	
VCC	AB6	Power/Other	
VCC	AB8	Power/Other	
VCC	AB10	Power/Other	
VCC	AB12	Power/Other	
VCC	AB14	Power/Other	
VCC	AB16	Power/Other	
VCC	AB18	Power/Other	
VCC	AB20	Power/Other	
VCC	AB22	Power/Other	
VCC	AC9	Power/Other	
VCC	AC11	Power/Other	
VCC	AC13	Power/Other	

Table 4-3. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VCC	AC15	Power/Other	
VCC	AC17	Power/Other	
VCC	AC19	Power/Other	
VCC	AD8	Power/Other	
VCC	AD10	Power/Other	
VCC	AD12	Power/Other	
VCC	AD14	Power/Other	
VCC	AD16	Power/Other	
VCC	AD18	Power/Other	
VCC	AE9	Power/Other	
VCC	AE11	Power/Other	
VCC	AE13	Power/Other	
VCC	AE15	Power/Other	
VCC	AE17	Power/Other	
VCC	AE19	Power/Other	
VCC	AF8	Power/Other	
VCC	AF10	Power/Other	
VCC	AF12	Power/Other	
VCC	AF14	Power/Other	
VCC	AF16	Power/Other	
VCC	AF18	Power/Other	
VCCA[0]	F26	Power/Other	
VCCA[1]	B1	Power/Other	
VCCA[2]	N1	Power/Other	
VCCA[3]	AC26	Power/Other	
VCCP	D10	Power/Other	
VCCP	D12	Power/Other	
VCCP	D14	Power/Other	
VCCP	D16	Power/Other	
VCCP	E11	Power/Other	
VCCP	E13	Power/Other	
VCCP	E15	Power/Other	
VCCP	F10	Power/Other	
VCCP	F12	Power/Other	
VCCP	F14	Power/Other	
VCCP	F16	Power/Other	
VCCP	K6	Power/Other	
VCCP	L5	Power/Other	

Table 4-3. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VCCP	L21	Power/Other	
VCCP	M6	Power/Other	
VCCP	M22	Power/Other	
VCCP	N5	Power/Other	
VCCP	N21	Power/Other	
VCCP	P6	Power/Other	
VCCP	P22	Power/Other	
VCCP	R5	Power/Other	
VCCP	R21	Power/Other	
VCCP	T6	Power/Other	
VCCP	T22	Power/Other	
VCCP	U21	Power/Other	
VCCQ[0]	P23	Power/Other	
VCCQ[1]	W4	Power/Other	
VCCSENSE	AE7	Power/Other	Output
VID[0]	E2	CMOS	Output
VID[1]	F2	CMOS	Output
VID[2]	F3	CMOS	Output
VID[3]	G3	CMOS	Output
VID[4]	G4	CMOS	Output
VID[5]	H4	CMOS	Output
VSS	A2	Power/Other	
VSS	A5	Power/Other	
VSS	A8	Power/Other	
VSS	A11	Power/Other	
VSS	A14	Power/Other	
VSS	A17	Power/Other	
VSS	A20	Power/Other	
VSS	A23	Power/Other	
VSS	A26	Power/Other	
VSS	B3	Power/Other	
VSS	B6	Power/Other	
VSS	B9	Power/Other	
VSS	B12	Power/Other	
VSS	B16	Power/Other	
VSS	B19	Power/Other	
VSS	B22	Power/Other	
VSS	B25	Power/Other	

Table 4-3. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	C1	Power/Other	
VSS	C4	Power/Other	
VSS	C7	Power/Other	
VSS	C10	Power/Other	
VSS	C13	Power/Other	
VSS	C15	Power/Other	
VSS	C18	Power/Other	
VSS	C21	Power/Other	
VSS	C24	Power/Other	
VSS	D2	Power/Other	
VSS	D5	Power/Other	
VSS	D7	Power/Other	
VSS	D9	Power/Other	
VSS	D11	Power/Other	
VSS	D13	Power/Other	
VSS	D15	Power/Other	
VSS	D17	Power/Other	
VSS	D19	Power/Other	
VSS	D21	Power/Other	
VSS	D23	Power/Other	
VSS	D26	Power/Other	
VSS	E3	Power/Other	
VSS	E6	Power/Other	
VSS	E8	Power/Other	
VSS	E10	Power/Other	
VSS	E12	Power/Other	
VSS	E14	Power/Other	
VSS	E16	Power/Other	
VSS	E18	Power/Other	
VSS	E20	Power/Other	
VSS	E22	Power/Other	
VSS	E25	Power/Other	
VSS	F1	Power/Other	
VSS	F4	Power/Other	
VSS	F5	Power/Other	
VSS	F7	Power/Other	
VSS	F9	Power/Other	
VSS	F11	Power/Other	

Table 4-3. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	F13	Power/Other	
VSS	F15	Power/Other	
VSS	F17	Power/Other	
VSS	F19	Power/Other	
VSS	F21	Power/Other	
VSS	F24	Power/Other	
VSS	G2	Power/Other	
VSS	G6	Power/Other	
VSS	G22	Power/Other	
VSS	G23	Power/Other	
VSS	G26	Power/Other	
VSS	H3	Power/Other	
VSS	H5	Power/Other	
VSS	H21	Power/Other	
VSS	H25	Power/Other	
VSS	J1	Power/Other	
VSS	J4	Power/Other	
VSS	J6	Power/Other	
VSS	J22	Power/Other	
VSS	J24	Power/Other	
VSS	K2	Power/Other	
VSS	K5	Power/Other	
VSS	K21	Power/Other	
VSS	K23	Power/Other	
VSS	K26	Power/Other	
VSS	L3	Power/Other	
VSS	L6	Power/Other	
VSS	L22	Power/Other	
VSS	L25	Power/Other	
VSS	M1	Power/Other	
VSS	M4	Power/Other	
VSS	M5	Power/Other	
VSS	M21	Power/Other	
VSS	M24	Power/Other	
VSS	N3	Power/Other	
VSS	N6	Power/Other	
VSS	N22	Power/Other	
VSS	N23	Power/Other	

Table 4-3. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	N26	Power/Other	
VSS	P2	Power/Other	
VSS	P5	Power/Other	
VSS	P21	Power/Other	
VSS	P24	Power/Other	
VSS	R1	Power/Other	
VSS	R4	Power/Other	
VSS	R6	Power/Other	
VSS	R22	Power/Other	
VSS	R25	Power/Other	
VSS	T3	Power/Other	
VSS	T5	Power/Other	
VSS	T21	Power/Other	
VSS	T23	Power/Other	
VSS	T26	Power/Other	
VSS	U2	Power/Other	
VSS	U6	Power/Other	
VSS	U22	Power/Other	
VSS	U24	Power/Other	
VSS	V1	Power/Other	
VSS	V4	Power/Other	
VSS	V5	Power/Other	
VSS	V21	Power/Other	
VSS	V25	Power/Other	
VSS	W3	Power/Other	
VSS	W6	Power/Other	
VSS	W22	Power/Other	
VSS	W23	Power/Other	
VSS	W26	Power/Other	
VSS	Y2	Power/Other	
VSS	Y5	Power/Other	
VSS	Y21	Power/Other	
VSS	Y24	Power/Other	
VSS	AA1	Power/Other	
VSS	AA4	Power/Other	
VSS	AA6	Power/Other	
VSS	AA8	Power/Other	
VSS	AA10	Power/Other	

Table 4-3. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	AA12	Power/Other	
VSS	AA14	Power/Other	
VSS	AA16	Power/Other	
VSS	AA18	Power/Other	
VSS	AA20	Power/Other	
VSS	AA22	Power/Other	
VSS	AA25	Power/Other	
VSS	AB3	Power/Other	
VSS	AB5	Power/Other	
VSS	AB7	Power/Other	
VSS	AB9	Power/Other	
VSS	AB11	Power/Other	
VSS	AB13	Power/Other	
VSS	AB15	Power/Other	
VSS	AB17	Power/Other	
VSS	AB19	Power/Other	
VSS	AB21	Power/Other	
VSS	AB23	Power/Other	
VSS	AB26	Power/Other	
VSS	AC2	Power/Other	
VSS	AC5	Power/Other	
VSS	AC8	Power/Other	
VSS	AC10	Power/Other	
VSS	AC12	Power/Other	
VSS	AC14	Power/Other	
VSS	AC16	Power/Other	
VSS	AC18	Power/Other	
VSS	AC21	Power/Other	
VSS	AC24	Power/Other	
VSS	AD1	Power/Other	
VSS	AD4	Power/Other	
VSS	AD7	Power/Other	
VSS	AD9	Power/Other	
VSS	AD11	Power/Other	
VSS	AD13	Power/Other	
VSS	AD15	Power/Other	
VSS	AD17	Power/Other	
VSS	AD19	Power/Other	

Table 4-3. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	AD22	Power/Other	
VSS	AD25	Power/Other	
VSS	AE3	Power/Other	
VSS	AE6	Power/Other	
VSS	AE8	Power/Other	
VSS	AE10	Power/Other	
VSS	AE12	Power/Other	
VSS	AE14	Power/Other	
VSS	AE16	Power/Other	
VSS	AE18	Power/Other	
VSS	AE20	Power/Other	
VSS	AE23	Power/Other	
VSS	AE26	Power/Other	
VSS	AF2	Power/Other	
VSS	AF5	Power/Other	
VSS	AF9	Power/Other	
VSS	AF11	Power/Other	
VSS	AF13	Power/Other	
VSS	AF15	Power/Other	
VSS	AF17	Power/Other	
VSS	AF19	Power/Other	
VSS	AF21	Power/Other	
VSS	AF24	Power/Other	
VSSSENSE	AF6	Power/Other	Output

Table 4-4. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
A2	VSS	Power/Other	
A3	IGNNE#	CMOS	Input
A4	IERR#	Open Drain	Output
A5	VSS	Power/Other	
A6	SLP#	CMOS	Input
A7	DBR#	CMOS	Output
A8	VSS	Power/Other	
A9	BPM[2]#	Common Clock	Output
A10	PRDY#	Common Clock	Output
A11	VSS	Power/Other	
A12	TDO	Open Drain	Output

Table 4-4. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
A13	TCK	CMOS	Input
A14	VSS	Power/Other	
A15	ITP_CLK[1]	CMOS	input
A16	ITP_CLK[0]	CMOS	input
A17	VSS	Power/Other	
A18	THERMDC	Power/Other	
A19	D[0]#	Source Synch	Input/Output
A20	VSS	Power/Other	
A21	D[6]#	Source Synch	Input/Output
A22	D[2]#	Source Synch	Input/Output
A23	VSS	Power/Other	
A24	D[4]#	Source Synch	Input/Output
A25	D[1]#	Source Synch	Input/Output
A26	VSS	Power/Other	
AA1	VSS	Power/Other	
AA2	A[16]#	Source Synch	Input/Output
AA3	A[14]#	Source Synch	Input/Output
AA4	VSS	Power/Other	
AA5	VCC	Power/Other	
AA6	VSS	Power/Other	
AA7	VCC	Power/Other	
AA8	VSS	Power/Other	
AA9	VCC	Power/Other	
AA10	VSS	Power/Other	
AA11	VCC	Power/Other	
AA12	VSS	Power/Other	
AA13	VCC	Power/Other	
AA14	VSS	Power/Other	
AA15	VCC	Power/Other	
AA16	VSS	Power/Other	
AA17	VCC	Power/Other	
AA18	VSS	Power/Other	
AA19	VCC	Power/Other	
AA20	VSS	Power/Other	
AA21	VCC	Power/Other	
AA22	VSS	Power/Other	
AA23	D[40]#	Source Synch	Input/Output
AA24	D[33]#	Source Synch	Input/Output

Table 4-4. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
AA25	VSS	Power/Other	
AA26	D[46]#	Source Synch	Input/Output
AB1	COMP[3]	Power/Other	Input/Output
AB2	COMP[2]	Power/Other	Input/Output
AB3	VSS	Power/Other	
AB4	A[24]#	Source Synch	Input/Output
AB5	VSS	Power/Other	
AB6	VCC	Power/Other	
AB7	VSS	Power/Other	
AB8	VCC	Power/Other	
AB9	VSS	Power/Other	
AB10	VCC	Power/Other	
AB11	VSS	Power/Other	
AB12	VCC	Power/Other	
AB13	VSS	Power/Other	
AB14	VCC	Power/Other	
AB15	VSS	Power/Other	
AB16	VCC	Power/Other	
AB17	VSS	Power/Other	
AB18	VCC	Power/Other	
AB19	VSS	Power/Other	
AB20	VCC	Power/Other	
AB21	VSS	Power/Other	
AB22	VCC	Power/Other	
AB23	VSS	Power/Other	
AB24	D[50]#	Source Synch	Input/Output
AB25	D[48]#	Source Synch	Input/Output
AB26	VSS	Power/Other	
AC1	RSVD	Reserved	
AC2	VSS	Power/Other	
AC3	A[20]#	Source Synch	Input/Output
AC4	A[18]#	Source Synch	Input/Output
AC5	VSS	Power/Other	
AC6	A[25]#	Source Synch	Input/Output
AC7	A[19]#	Source Synch	Input/Output
AC8	VSS	Power/Other	
AC9	VCC	Power/Other	
AC10	VSS	Power/Other	

Table 4-4. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
AC11	VCC	Power/Other	
AC12	VSS	Power/Other	
AC13	VCC	Power/Other	
AC14	VSS	Power/Other	
AC15	VCC	Power/Other	
AC16	VSS	Power/Other	
AC17	VCC	Power/Other	
AC18	VSS	Power/Other	
AC19	VCC	Power/Other	
AC20	D[51]#	Source Synch	Input/Output
AC21	VSS	Power/Other	
AC22	D[52]#	Source Synch	Input/Output
AC23	D[49]#	Source Synch	Input/Output
AC24	VSS	Power/Other	
AC25	D[53]#	Source Synch	Input/Output
AC26	VCCA[3]	Power/Other	
AD1	VSS	Power/Other	
AD2	A[23]#	Source Synch	Input/Output
AD3	A[21]#	Source Synch	Input/Output
AD4	VSS	Power/Other	
AD5	A[26]#	Source Synch	Input/Output
AD6	A[28]#	Source Synch	Input/Output
AD7	VSS	Power/Other	
AD8	VCC	Power/Other	
AD9	VSS	Power/Other	
AD10	VCC	Power/Other	
AD11	VSS	Power/Other	
AD12	VCC	Power/Other	
AD13	VSS	Power/Other	
AD14	VCC	Power/Other	
AD15	VSS	Power/Other	
AD16	VCC	Power/Other	
AD17	VSS	Power/Other	
AD18	VCC	Power/Other	
AD19	VSS	Power/Other	
AD20	DINV[3]#	Source Synch	Input/Output
AD21	D[60]#	Source Synch	Input/Output
AD22	VSS	Power/Other	

Table 4-4. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
AD23	D[54]#	Source Synch	Input/Output
AD24	D[57]#	Source Synch	Input/Output
AD25	VSS	Power/Other	
AD26	GTLREF	Power/Other	
AE1	A[30]#	Source Synch	Input/Output
AE2	A[27]#	Source Synch	Input/Output
AE3	VSS	Power/Other	
AE4	A[22]#	Source Synch	Input/Output
AE5	ADSTB[1]#	Source Synch	Input/Output
AE6	VSS	Power/Other	
AE7	VCCSENSE	Power/Other	Output
AE8	VSS	Power/Other	
AE9	VCC	Power/Other	
AE10	VSS	Power/Other	
AE11	VCC	Power/Other	
AE12	VSS	Power/Other	
AE13	VCC	Power/Other	
AE14	VSS	Power/Other	
AE15	VCC	Power/Other	
AE16	VSS	Power/Other	
AE17	VCC	Power/Other	
AE18	VSS	Power/Other	
AE19	VCC	Power/Other	
AE20	VSS	Power/Other	
AE21	D[59]#	Source Synch	Input/Output
AE22	D[55]#	Source Synch	Input/Output
AE23	VSS	Power/Other	
AE24	DSTBN[3]#	Source Synch	Input/Output
AE25	DSTBP[3]#	Source Synch	Input/Output
AE26	VSS	Power/Other	
AF1	A[31]#	Source Synch	Input/Output
AF2	VSS	Power/Other	
AF3	A[29]#	Source Synch	Input/Output
AF4	A[17]#	Source Synch	Input/Output
AF5	VSS	Power/Other	
AF6	VSSSENSE	Power/Other	Output
AF7	RSVD	Reserved	
AF8	VCC	Power/Other	

Table 4-4. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
AF9	VSS	Power/Other	
AF10	VCC	Power/Other	
AF11	VSS	Power/Other	
AF12	VCC	Power/Other	
AF13	VSS	Power/Other	
AF14	VCC	Power/Other	
AF15	VSS	Power/Other	
AF16	VCC	Power/Other	
AF17	VSS	Power/Other	
AF18	VCC	Power/Other	
AF19	VSS	Power/Other	
AF20	D[58]#	Source Synch	Input/Output
AF21	VSS	Power/Other	
AF22	D[62]#	Source Synch	Input/Output
AF23	D[56]#	Source Synch	Input/Output
AF24	VSS	Power/Other	
AF25	D[61]#	Source Synch	Input/Output
AF26	D[63]#	Source Synch	Input/Output
B1	VCCA[1]	Power/Other	
B2	RSVD	Reserved	
B3	VSS	Power/Other	
B4	SMI#	CMOS	Input
B5	INIT#	CMOS	Input
B6	VSS	Power/Other	
B7	DPSLP#	CMOS	Input
B8	BPM[1]#	Common Clock	Output
B9	VSS	Power/Other	
B10	PREQ#	Common Clock	Input
B11	RESET#	Common Clock	Input
B12	VSS	Power/Other	
B13	TRST#	CMOS	Input
B14	BCLK[1]	Bus Clock	Input
B15	BCLK[0]	Bus Clock	Input
B16	VSS	Power/Other	
B17	PROCHOT#	Open Drain	Output
B18	THERMDA	Power/Other	
B19	VSS	Power/Other	
B20	D[7]#	Source Synch	Input/Output

Table 4-4. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
B21	D[3]#	Source Synch	Input/Output
B22	VSS	Power/Other	
B23	D[13]#	Source Synch	Input/Output
B24	D[9]#	Source Synch	Input/Output
B25	VSS	Power/Other	
B26	D[5]#	Source Synch	Input/Output
C1	VSS	Power/Other	
C2	A20M#	CMOS	Input
C3	RSVD	Reserved	
C4	VSS	Power/Other	
C5	TEST1	Test	
C6	STPCLK#	CMOS	Input
C7	VSS	Power/Other	
C8	BPM[0]#	Common Clock	Output
C9	BPM[3]#	Common Clock	Input/Output
C10	VSS	Power/Other	
C11	TMS	CMOS	Input
C12	TDI	CMOS	Input
C13	VSS	Power/Other	
C14	BSEL[1]	CMOS	Output
C15	VSS	Power/Other	
C16	BSEL[0]	CMOS	Output
C17	THERMTRIP#	Open Drain	Output
C18	VSS	Power/Other	
C19	DPWR#	Common Clock	Input
C20	D[8]#	Source Synch	Input/Output
C21	VSS	Power/Other	
C22	DSTBP[0]#	Source Synch	Input/Output
C23	DSTBN[0]#	Source Synch	Input/Output
C24	VSS	Power/Other	
C25	D[15]#	Source Synch	Input/Output
C26	D[12]#	Source Synch	Input/Output
D1	LINT0	CMOS	Input
D2	VSS	Power/Other	
D3	FERR#	Open Drain	Output
D4	LINT1	CMOS	Input
D5	VSS	Power/Other	
D6	VCC	Power/Other	

Table 4-4. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
D7	VSS	Power/Other	
D8	VCC	Power/Other	
D9	VSS	Power/Other	
D10	VCCP	Power/Other	
D11	VSS	Power/Other	
D12	VCCP	Power/Other	
D13	VSS	Power/Other	
D14	VCCP	Power/Other	
D15	VSS	Power/Other	
D16	VCCP	Power/Other	
D17	VSS	Power/Other	
D18	VCC	Power/Other	
D19	VSS	Power/Other	
D20	VCC	Power/Other	
D21	VSS	Power/Other	
D22	VCC	Power/Other	
D23	VSS	Power/Other	
D24	D[10]#	Source Synch	Input/Output
D25	DINV[0]#	Source Synch	Input/Output
D26	VSS	Power/Other	
E1	PSI#	CMOS	Output
E2	VID[0]	CMOS	Output
E3	VSS	Power/Other	
E4	PWRGOOD	CMOS	Input
E5	VCC	Power/Other	
E6	VSS	Power/Other	
E7	VCC	Power/Other	
E8	VSS	Power/Other	
E9	VCC	Power/Other	
E10	VSS	Power/Other	
E11	VCCP	Power/Other	
E12	VSS	Power/Other	
E13	VCCP	Power/Other	
E14	VSS	Power/Other	
E15	VCCP	Power/Other	
E16	VSS	Power/Other	
E17	VCC	Power/Other	
E18	VSS	Power/Other	

Table 4-4. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
E19	VCC	Power/Other	
E20	VSS	Power/Other	
E21	VCC	Power/Other	
E22	VSS	Power/Other	
E23	D[14]#	Source Synch	Input/Output
E24	D[11]#	Source Synch	Input/Output
E25	VSS	Power/Other	
E26	RSVD	Reserved	
F1	VSS	Power/Other	
F2	VID[1]	CMOS	Output
F3	VID[2]	CMOS	Output
F4	VSS	Power/Other	
F5	VSS	Power/Other	
F6	VCC	Power/Other	
F7	VSS	Power/Other	
F8	VCC	Power/Other	
F9	VSS	Power/Other	
F10	VCCP	Power/Other	
F11	VSS	Power/Other	
F12	VCCP	Power/Other	
F13	VSS	Power/Other	
F14	VCCP	Power/Other	
F15	VSS	Power/Other	
F16	VCCP	Power/Other	
F17	VSS	Power/Other	
F18	VCC	Power/Other	
F19	VSS	Power/Other	
F20	VCC	Power/Other	
F21	VSS	Power/Other	
F22	VCC	Power/Other	
F23	TEST2	Test	
F24	VSS	Power/Other	
F25	D[21]#	Source Synch	Input/Output
F26	VCCA[0]	Power/Other	
G1	RSVD	Reserved	
G2	VSS	Power/Other	
G3	VID[3]	CMOS	Output
G4	VID[4]	CMOS	Output

Table 4-4. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
G5	VCC	Power/Other	
G6	VSS	Power/Other	
G21	VCC	Power/Other	
G22	VSS	Power/Other	
G23	VSS	Power/Other	
G24	D[22]#	Source Synch	Input/Output
G25	D[17]#	Source Synch	Input/Output
G26	VSS	Power/Other	
H1	RS[0]#	Common Clock	Input
H2	DRDY#	Common Clock	Input/Output
H3	VSS	Power/Other	
H4	VID[5]	CMOS	Output
H5	VSS	Power/Other	
H6	VCC	Power/Other	
H21	VSS	Power/Other	
H22	VCC	Power/Other	
H23	D[16]#	Source Synch	Input/Output
H24	D[20]#	Source Synch	Input/Output
H25	VSS	Power/Other	
H26	D[29]#	Source Synch	Input/Output
J1	VSS	Power/Other	
J2	LOCK#	Common Clock	Input/Output
J3	BPRI#	Common Clock	Input
J4	VSS	Power/Other	
J5	VCC	Power/Other	
J6	VSS	Power/Other	
J21	VCC	Power/Other	
J22	VSS	Power/Other	
J23	D[23]#	Source Synch	Input/Output
J24	VSS	Power/Other	
J25	D[25]#	Source Synch	Input/Output
J26	DINV[1]#	Source Synch	Input/Output
K1	RS[1]#	Common Clock	Input
K2	VSS	Power/Other	
K3	HIT#	Common Clock	Input/Output
K4	HITM#	Common Clock	Input/Output
K5	VSS	Power/Other	
K6	VCCP	Power/Other	

Table 4-4. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
K21	VSS	Power/Other	
K22	VCC	Power/Other	
K23	VSS	Power/Other	
K24	DSTBN[1]#	Source Synch	Input/Output
K25	D[31]#	Source Synch	Input/Output
K26	VSS	Power/Other	
L1	BNR#	Common Clock	Input/Output
L2	RS[2]#	Common Clock	Input
L3	VSS	Power/Other	
L4	DEFER#	Common Clock	Input
L5	VCCP	Power/Other	
L6	VSS	Power/Other	
L21	VCCP	Power/Other	
L22	VSS	Power/Other	
L23	D[18]#	Source Synch	Input/Output
L24	DSTBP[1]#	Source Synch	Input/Output
L25	VSS	Power/Other	
L26	D[26]#	Source Synch	Input/Output
M1	VSS	Power/Other	
M2	DBSY#	Common Clock	Input/Output
M3	TRDY#	Common Clock	Input
M4	VSS	Power/Other	
M5	VSS	Power/Other	
M6	VCCP	Power/Other	
M21	VSS	Power/Other	
M22	VCCP	Power/Other	
M23	D[24]#	Source Synch	Input/Output
M24	VSS	Power/Other	
M25	D[28]#	Source Synch	Input/Output
M26	D[19]#	Source Synch	Input/Output
N1	VCCA[2]	Power/Other	
N2	ADS#	Common Clock	Input/Output
N3	VSS	Power/Other	
N4	BR0#	Common Clock	Input/Output
N5	VCCP	Power/Other	
N6	VSS	Power/Other	
N21	VCCP	Power/Other	
N22	VSS	Power/Other	

Table 4-4. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
N23	VSS	Power/Other	
N24	D[27]#	Source Synch	Input/Output
N25	D[30]#	Source Synch	Input/Output
N26	VSS	Power/Other	
P1	REQ[3]#	Source Synch	Input/Output
P2	VSS	Power/Other	
P3	REQ[1]#	Source Synch	Input/Output
P4	A[3]#	Source Synch	Input/Output
P5	VSS	Power/Other	
P6	VCCP	Power/Other	
P21	VSS	Power/Other	
P22	VCCP	Power/Other	
P23	VCCQ[0]	Power/Other	
P24	VSS	Power/Other	
P25	COMP[0]	Power/Other	Input/Output
P26	COMP[1]	Power/Other	Input/Output
R1	VSS	Power/Other	
R2	REQ[0]#	Source Synch	Input/Output
R3	A[6]#	Source Synch	Input/Output
R4	VSS	Power/Other	
R5	VCCP	Power/Other	
R6	VSS	Power/Other	
R21	VCCP	Power/Other	
R22	VSS	Power/Other	
R23	D[39]#	Source Synch	Input/Output
R24	D[37]#	Source Synch	Input/Output
R25	VSS	Power/Other	
R26	D[38]#	Source Synch	Input/Output
T1	REQ[4]#	Source Synch	Input/Output
T2	REQ[2]#	Source Synch	Input/Output
T3	VSS	Power/Other	
T4	A[9]#	Source Synch	Input/Output
T5	VSS	Power/Other	
T6	VCCP	Power/Other	
T21	VSS	Power/Other	
T22	VCCP	Power/Other	
T23	VSS	Power/Other	
T24	DINV[2]#	CMOS	Input/Output

Table 4-4. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
T25	D[34]#	Source Synch	Input/Output
T26	VSS	Power/Other	
U1	A[13]#	Source Synch	Input/Output
U2	VSS	Power/Other	
U3	ADSTB[0]#	Source Synch	Input/Output
U4	A[4]#	Source Synch	Input/Output
U5	VCC	Power/Other	
U6	VSS	Power/Other	
U21	VCCP	Power/Other	
U22	VSS	Power/Other	
U23	D[35]#	Source Synch	Input/Output
U24	VSS	Power/Other	
U25	D[43]#	Source Synch	Input/Output
U26	D[41]#	Source Synch	Input/Output
V1	VSS	Power/Other	
V2	A[7]#	Source Synch	Input/Output
V3	A[5]#	Source Synch	Input/Output
V4	VSS	Power/Other	
V5	VSS	Power/Other	
V6	VCC	Power/Other	
V21	VSS	Power/Other	
V22	VCC	Power/Other	
V23	D[36]#	Source Synch	Input/Output
V24	D[42]#	Source Synch	Input/Output
V25	VSS	Power/Other	
V26	D[44]#	Source Synch	Input/Output
W1	A[8]#	Source Synch	Input/Output
W2	A[10]#	Source Synch	Input/Output
W3	VSS	Power/Other	
W4	VCCQ[1]	Power/Other	
W5	VCC	Power/Other	
W6	VSS	Power/Other	
W21	VCC	Power/Other	
W22	VSS	Power/Other	
W23	VSS	Power/Other	
W24	DSTBP[2]#	Source Synch	Input/Output
W25	DSTBN[2]#	Source Synch	Input/Output
W26	VSS	Power/Other	

Table 4-4. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
Y1	A[12]#	Source Synch	Input/Output
Y2	VSS	Power/Other	
Y3	A[15]#	Source Synch	Input/Output
Y4	A[11]#	Source Synch	Input/Output
Y5	VSS	Power/Other	
Y6	VCC	Power/Other	
Y21	VSS	Power/Other	
Y22	VCC	Power/Other	
Y23	D[45]#	Source Synch	Input/Output
Y24	VSS	Power/Other	
Y25	D[47]#	Source Synch	Input/Output
Y26	D[32]#	Source Synch	Input/Output

4.2 Alphabetical Signals Reference

Table 4-5. Signal Description (Sheet 1 of 7)

Name	Type	Description
A[31:3]#	Input/ Output	A[31:3]# (Address) define a 2^{32}-byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals must connect the appropriate pins of both agents on the Intel®Pentium® M Processor FSB. A[31:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. Address signals are used as straps which are sampled before RESET# is deasserted.
A20M#	Input	If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
ADS#	Input/ Output	ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[31:3]# and REQ[4:0]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction.
ADSTB[1:0]#	Input/ Output	Address strobes are used to latch A[31:3]# and REQ[4:0]# on their rising and falling edges. Strobes are associated with signals as shown below. **Signals** / **Associated Strobe** REQ[4:0]#, A[16:3]# / ADSTB[0]# A[31:17]# / ADSTB[1]#
BCLK[1:0]	Input	The differential pair BCLK (Bus Clock) determines the FSB frequency. All FSB agents must receive these signals to drive their outputs and latch their inputs. All external timing parameters are specified with respect to the rising edge of BCLK0 crossing V_{CROSS}.
BNR#	Input/ Output	BNR# (Block Next Request) is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.
BPM[2:0]# BPM[3]	Output Input/ Output	BPM[3:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[3:0]# should connect the appropriate pins of all Intel® Pentium® M FSB agents.This includes debug or performance monitoring tools. Please refer to the platform design guides for more detailed information.
BPRI#	Input	BPRI# (Bus Priority Request) is used to arbitrate for ownership of the FSB. It must connect the appropriate pins of both FSB agents. Observing BPRI# active (as asserted by the priority agent) causes the other agent to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.
BR0#	Input/ Output	BR0# is used by the processor to request the bus. The arbitration is done between Intel®Pentium® M (Symmetric Agent) and Intel 855 chipset family MCH-M (High Priority Agent).

Table 4-5. Signal Description (Sheet 2 of 7)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>BSEL[1:0]</td><td>Output</td><td>These signals are used to select the FSB clock frequency. They should be connected between the processor and the chipset MCH and clock generator on Intel 915 chipset family based platforms. These signals must be left unconnected on platforms designed with the Intel 855 chipset family. On these platforms, FSB clock frequency should be configured on the motherboard.</td></tr>
<tr><td>COMP[3:0]</td><td>Analog</td><td>COMP[3:0] must be terminated on the system board using precision (1% tolerance) resistors. Refer to the platform design guides for more details on implementation.</td></tr>
<tr><td>D[63:0]#</td><td>Input/
Output</td><td>D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the FSB agents, and must connect the appropriate pins on both agents. The data driver asserts DRDY# to indicate a valid data transfer.

D[63:0]# are quad-pumped signals and will thus be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to data strobes and DINV#.

Quad-Pumped Signal Groups
<table>
<tr><th>Data Group</th><th>DSTBN#/
DSTBP#</th><th>DINV#</th></tr>
<tr><td>D[15:0]#</td><td>0</td><td>0</td></tr>
<tr><td>D[31:16]#</td><td>1</td><td>1</td></tr>
<tr><td>D[47:32]#</td><td>2</td><td>2</td></tr>
<tr><td>D[63:48]#</td><td>3</td><td>3</td></tr>
</table>
Furthermore, the DINV# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DINV# signal. When the DINV# signal is active, the corresponding data group is inverted and therefore sampled active high.</td></tr>
<tr><td>DBR#</td><td>Output</td><td>DBR# (Data Bus Reset) is used only in processor systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset. If a debug port is implemented in the system, DBR# is a no connect in the system. DBR# is not a processor signal.</td></tr>
<tr><td>DBSY#</td><td>Input/
Output</td><td>DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the FSB to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on both FSB agents.</td></tr>
<tr><td>DEFER#</td><td>Input</td><td>DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or Input/Output agent. This signal must connect the appropriate pins of both FSB agents.</td></tr>
</table>

Table 4-5. Signal Description (Sheet 3 of 7)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>DINV[3:0]#</td><td>Input/
Output</td><td>DINV[3:0]# (Data Bus Inversion) are source synchronous and indicate the polarity of the D[63:0]# signals. The DINV[3:0]# signals are activated when the data on the data bus is inverted. The bus agent will invert the data bus signals if more than half the bits, within the covered group, would change level in the next cycle.
DINV[3:0]# Assignment To Data Bus
<table>
<tr><th>Bus Signal</th><th>Data Bus Signals</th></tr>
<tr><td>DINV[3]#</td><td>D[63:48]#</td></tr>
<tr><td>DINV[2]#</td><td>D[47:32]#</td></tr>
<tr><td>DINV[1]#</td><td>D[31:16]#</td></tr>
<tr><td>DINV[0]#</td><td>D[15:0]#</td></tr>
</table></td></tr>
<tr><td>DPSLP#</td><td>Input</td><td>DPSLP# when asserted on the platform causes the processor to transition from the Sleep State to the Deep Sleep state. In order to return to the Sleep state, DPSLP# must be deasserted. DPSLP# is driven by the ICH4-M component and also connects to the Intel 855 chipset family MCH-M component.</td></tr>
<tr><td>DPWR#</td><td>Input</td><td>DPWR# is a control signal from the Intel® 852/855 and 915 chipset family used to reduce power on the Intel® Pentium® M data bus input buffers.</td></tr>
<tr><td>DRDY#</td><td>Input/
Output</td><td>DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of both FSB agents.</td></tr>
<tr><td>DSTBN[3:0]#</td><td>Input/
Output</td><td>Data strobe used to latch in D[63:0]#.
<table>
<tr><th>Signals</th><th>Associated Strobe</th></tr>
<tr><td>D[15:0]#, DINV[0]#</td><td>DSTBN[0]#</td></tr>
<tr><td>D[31:16]#, DINV[1]#</td><td>DSTBN[1]#</td></tr>
<tr><td>D[47:32]#, DINV[2]#</td><td>DSTBN[2]#</td></tr>
<tr><td>D[63:48]#, DINV[3]#</td><td>DSTBN[3]#</td></tr>
</table></td></tr>
<tr><td>DSTBP[3:0]#</td><td>Input/
Output</td><td>Data strobe used to latch in D[63:0]#.
<table>
<tr><th>Signals</th><th>Associated Strobe</th></tr>
<tr><td>D[15:0]#, DINV[0]#</td><td>DSTBP[0]#</td></tr>
<tr><td>D[31:16]#, DINV[1]#</td><td>DSTBP[1]#</td></tr>
<tr><td>D[47:32]#, DINV[2]#</td><td>DSTBP[2]#</td></tr>
<tr><td>D[63:48]#, DINV[3]#</td><td>DSTBP[3]#</td></tr>
</table></td></tr>
</table>

Table 4-5. Signal Description (Sheet 4 of 7)

Name	Type	Description
FERR#/PBE#	Output	FERR# (Floating-point Error)PBE#(Pending Break Event) is a multiplexed signal and its meaning is qualified with STPCLK#. When STPCLK# is not asserted, FERR#/PBE# indicates a floating point when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MS-DOS*-type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. The assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. When FERR#/PBE# is asserted, indicating a break event, it will remain asserted until STPCLK# is deasserted. Assertion of PREQ# when STPCLK# is active will also cause an FERR# break event. For additional information on the pending break event functionality, including identification of support of the feature and enable/disable information, refer to Volume 3 of the *Intel® Architecture Software Developer's Manual* and the *Intel® Processor Identification and CPUID Instruction* application note. For termination requirements please refer to the platform design guides.
GTLREF	Input	GTLREF determines the signal reference level for AGTL+ input pins. GTLREF should be set at 2/3 V_{CCP}. GTLREF is used by the AGTL+ receivers to determine if a signal is a logical 0 or logical 1. Please refer to the platform design guides for details on GTLREF implementation.
HIT# HITM#	Input/ Output Input/ Output	HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Either FSB agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
IERR#	Output	IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the FSB. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#. For termination requirements please refer to the platform design guides.
IGNNE#	Input	IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
INIT#	Input	INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output Write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction. INIT# must connect the appropriate pins of both FSB agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST) For termination requirements please refer to the platform design guides.
ITP_CLK[1:0]	Input	ITP_CLK[1:0] are copies of BCLK that are used only in processor systems where no debug port is implemented on the system board. ITP_CLK[1:0] are used as BCLK[1:0] references for a debug port implemented on an interposer. If a debug port is implemented in the system, ITP_CLK[1:0] are no connects in the system. These are not processor signals.

Table 4-5. Signal Description (Sheet 5 of 7)

Name	Type	Description
LINT[1:0]	Input	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium Processor. Both signals are asynchronous. Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after reset, operation of these pins as LINT[1:0] is the default configuration.
LOCK#	Input/ Output	LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of both FSB agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the FSB, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the FSB throughout the bus locked operation and ensure the atomicity of lock.
PRDY#	Output	Probe Ready signal used by debug tools to determine processor debug readiness. Please refer to the platform design guides for more implementation details.
PREQ#	Input	Probe Request signal used by debug tools to request debug operation of the processor. Please refer to the platform design guides for more implementation details.
PROCHOT#	Output	PROCHOT# (Processor Hot) will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit has been activated, if enabled. See Chapter 5 for more details. For termination requirements please refer to the platform design guides. This signal may require voltage translation on the motherboard. Please refer to the platform design guides for more details.
PSI#	Output	Processor Power Status Indicator signal. This signal is asserted when the processor is in a lower state (Deep Sleep and Deeper Sleep). See Section 2.1.6 for more details.
PWRGOOD	Input	PWRGOOD (Power Good) is a processor input. The processor requires this signal to be a clean indication that the clocks and power supplies are stable and within their specifications. Clean implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation. For termination requirements please refer to the platform design guides.
REQ[4:0]#	Input/ Output	REQ[4:0]# (Request Command) must connect the appropriate pins of both FSB agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB[0]#.
RESET#	Input	Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least two milliseconds after V_{CC} and BCLK have reached their proper specifications. On observing active RESET#, both FSB agents will deassert their outputs within two clocks. All processor straps must be valid within the specified setup time before RESET# is deasserted. Please refer to the *Platform Design Guides* for termination requirements and implementation details. There is a 55 ohm (nominal) on die pullup resistor on this signal.

Table 4-5. Signal Description (Sheet 6 of 7)

Name	Type	Description
RS[2:0]#	Input	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of both FSB agents.
RSVD	Reserved/ No Connect	These pins are RESERVED and must be left unconnected on the board. However, it is recommended that routing channels to these pins on the board be kept open for possible future use. Please refer to the platform design guides for more details.
SLP#	Input	SLP# (Sleep), when asserted in Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertion of the RESET# signal, deassertion of SLP#, and removal of the BCLK input while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units. If DPSLP# is asserted while in the Sleep state, the processor will exit the Sleep state and transition to the Deep Sleep state.
SMI#	Input	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enter System Management mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. If SMI# is asserted during the deassertion of RESET# the processor will tristate its outputs.
STPCLK#	Input	STPCLK# (Stop Clock), when asserted, causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the FSB and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	Input	TCK (Test Clock) provides the clock input for the processor test bus (also known as the Test Access Port). Please refer to the platform design guides for termination requirements and implementation details.
TDI	Input	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support. Please refer to the platform design guides for termination requirements and implementation details.
TDO	Output	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support. Please refer to the platform design guides for termination requirements and implementation details.
TEST1, TEST2	Input	TEST1 and TEST2 must have a stuffing option of separate pull down resistors to V_{SS}. Please refer to the platform design guides for more details.
THERMDA	Other	Thermal Diode Anode.
THERMDC	Other	Thermal Diode Cathode.
THERMTRIP#	Output	The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 125 °C. This is signalled to the system by the THERMTRIP# (Thermal Trip) pin. For termination requirements please refer to the platform design guides .

Table 4-5. Signal Description (Sheet 7 of 7)

Name	Type	Description
TMS	Input	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools. Please refer to the platform design guides for termination requirements and implementation details.
TRDY#	Input	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of both FSB agents.
TRST#	Input	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset. Please refer to the platform design guides for termination requirements and implementation details.
V_{CC}	Input	Processor core power supply.
V_{CCA}[3:0]	Input	V_{CCA} provides isolated power for the internal processor core PLL's. Refer to the platform design guides for complete implementation details.
V_{CCP}	Input	Processor I/O power supply.
V_{CCQ}[1:0]	Input	Quiet power supply for on die COMP circuitry. These pins should be connected to V_{CCP} on the motherboard. However, these connections should enable addition of decoupling on the V_{CCQ} lines if necessary.
$V_{CCSENSE}$	Output	$V_{CCSENSE}$ is an isolated low impedance connection to processor core power (V_{CC}). It can be used to sense or measure power near the silicon with little noise. Please refer to the platform design guides for termination recommendations and more details.
VID[5:0]	Output	VID[5:0] (Voltage ID) pins are used to support automatic selection of power supply voltages (Vcc). Unlike some previous generations of processors, these are CMOS signals that are driven by the Intel® Pentium® M processor. The voltage supply for these pins must be valid before the VR can supply Vcc to the processor. Conversely, the VR output must be disabled until the voltage supply for the VID pins becomes valid. The VID pins are needed to support the processor voltage specification variations. See Table 3-1 for definitions of these pins. The VR must supply the voltage that is requested by the pins, or disable itself.
$V_{SSSENSE}$	Output	$V_{SSSENSE}$ is an isolated low impedance connection to processor core V_{SS}. It can be used to sense or measure ground near the silicon with little noise. Please refer to the platform design guides for termination recommendations and more details.

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5 Thermal Specifications and Design Considerations

The Pentium M Processor requires a thermal solution to maintain temperatures within operating limits as set forth in Section 5.1. Any attempt to operate that processor outside these operating limits may result in permanent damage to the processor and potentially other components in the system. As processor technology changes, thermal management becomes increasingly crucial when building computer systems. Maintaining the proper thermal environment is key to reliable, long-term system operation. A complete thermal solution includes both component and system level thermal management features. Component level thermal solutions include active or passive heatsinks or heat exchangers attached to the processor exposed die. The solution should make firm contact to the die while maintaining processor mechanical specifications such as pressure. A typical system level thermal solution may consist of a processor fan ducted to a heat exchanger that is thermally coupled to the processor via a heat pipe or direct die attachment. A secondary fan or air from the processor fan may also be used to cool other platform components or lower the internal ambient temperature within the system.

To allow for the optimal operation and long-term reliability of Intel processor-based systems, the system/processor thermal solution should be designed such that the processor must remain within the minimum and maximum junction temperature (Tj) specifications at the corresponding thermal design power (TDP) value listed in Table 5-1. Thermal solutions not design to provide this level of thermal capability may affect the long-term reliability of the processor and system.

The maximum junction temperature is defined by an activation of the processor Intel Thermal Monitor. Refer to Section 5.1.3 for more details. Analysis indicates that real applications are unlikely to cause the processor to consume the theoretical maximum power dissipation for sustained time periods. Intel recommends that complete thermal solution designs target the TDP indicated in Table 5-1. The Intel Thermal Monitor feature is designed to help protect the processor in the unlikely event that an application exceeds the TDP recommendation for a sustained period of time. For more details on the usage of this feature, refer to Section 5.1.3. In all cases the Intel Thermal Monitor feature must be enabled for the processor to remain within specification.

Table 5-1. Power Specifications for the Intel® Pentium M Processor (Sheet 1 of 3)

Symbol	Processor Number	Core Frequency & Voltage	Thermal Design Power			Unit	Notes
TDP	765	2.1 GHz & HFM Vcc	21			W	At 100°C, Notes 1, 4, 5
	755	2.0 GHz & HFM Vcc	21				
	745	1.8 GHz & HFM Vcc	21				
	735	1.7 GHz & HFM Vcc	21				
	725	1.6 GHz & HFM Vcc	21				
	715	1.5 GHz & HFM Vcc	21				
	778	1.6 GHz & HFM Vcc	10				
	758	1.5 GHz & HFM Vcc	10				
	738	1.4 GHz & HFM Vcc	10				
	765/755/745/ 735/725/715 & 778/758/738	600 MHz & LFM Vcc	7.5				
	773	1.3 GHz & HFM Vcc		5.5			
	753	1.2 GHz & HFM Vcc	5.5				
	733J	1.1 GHz & HFM Vcc	5.5				
	733	1.1 GHz & HFM Vcc	5.0				
	723	1.0 GHz & HFM Vcc	5.0				
	773/753/733J/ 733/723	600 MHz & LFM Vcc	3.0				
Symbol	**Processor Number**	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Notes**
$P_{AH,}$ P_{SGNT}	765/755/745/ 735/725/715	Auto Halt, Stop Grant Power:				W	At 50°C, Note 2
		LFM Vcc			3.3		
		HFM Vcc			10.9		
	778/758/738	Auto Halt, Stop Grant Power:				W	At 50°C, Note 2
		LFM Vcc			3.3		
		HFM Vcc			4.2		
	773/753/733J	Auto Halt, Stop Grant Power:				W	At 50°C, Note 2, 5
		LFM Vcc			1.1		
		HFM Vcc			1.9		
	733/723	Auto Halt, Stop Grant Power:				W	At 50°C, Note 2
		LFM Vcc			1.0		
		HFM Vcc			1.8		

Table 5-1. Power Specifications for the Intel® Pentium M Processor (Sheet 2 of 3)

Symbol	Processor Number	Parameter	Min	Typ	Max	Unit	Notes
P_{SLP}	765/755/745/ 735/725/715	Sleep Power:				W	At 50 °C, Note 2
		LFM Vcc			3.2		
		HFM Vcc			10.5		
	778/758/738	Sleep Power:				W	At 50 °C, Note 2
		LFM Vcc			3.2		
		HFM Vcc			4.0		
	773/753/733J	Sleep Power:				W	At 50 °C, Note 2, 5
		LFM Vcc			1.0		
		HFM Vcc			1.7		
	733/723	Sleep Power:				W	At 50 °C, Note 2
		LFM Vcc			0.9		
		HFM Vcc			1.7		
P_{DSLP}	765/755/745/ 735/725/715	Deep Sleep Power:				W	At 35 °C, Note 2
		LFM Vcc			2.5		
		HFM Vcc			8.8		
	778/758/738	Deep Sleep Power:				W	At 35 °C, Note 2
		LFM Vcc			2.5		
		HFM Vcc			2.9		
	773/753/733J	Deep Sleep Power:				W	At 35 °C, Note 2, 5
		LFM Vcc			0.7		
		HFM Vcc			1.25		
	733/723	Deep Sleep Power:				W	At 35 °C, Note 2
		LFM Vcc			0.6		
		HFM Vcc			1.2		
$P_{DPRSLP1}$	765/755/745/ 735/725/715 & 778/758/738	Deeper Sleep Power @ 0.748V			0.8	W	At 35 °C, Note 2
	753/733J/733/ 723	Deeper Sleep Power (ULV only)@ 0.748V			0.5	W	At 35 °C, Note 2, 5

Table 5-1. Power Specifications for the Intel® Pentium M Processor (Sheet 3 of 3)

Symbol	Processor Number	Parameter	Min	Typ	Max	Unit	Notes
$P_{DPRSL P2}$	765/755/745/ 735/725/715 & 778/758/738	Deeper Sleep Power @ 0.726V			0.7	W	At 35 °C, Note 2
	753/733J/733/ 723	Deeper Sleep Power (ULV only)@ 0.726			0.4	W	At 35 °C, Note 2, 5
T_J		Junction Temperature	0		100	°C	Notes 3, 4

NOTES:
1. The Thermal Design Power (TDP) specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can dissipate.
2. Not 100% tested. These power specifications are determined by characterization of the processor currents at higher temperatures and extrapolating the values for the temperature indicated.
3. As measured by the on-die Intel Thermal Monitor. The Intel Thermal Monitor's automatic mode is used to indicate that the maximum T_J has been reached. Refer to Section 5.1 for more details.
4. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specifications.
5. For 733J, CPU Signature = 06D8h.

5.1 Thermal Specifications

5.1.1 Thermal Diode

The Pentium M Processor incorporates two methods of monitoring die temperature, the Intel Thermal Monitor and the thermal diode. The Intel Thermal Monitor (detailed in Section 5.1) must be used to determine when the maximum specified processor junction temperature has been reached. The second method, the thermal diode, can be read by an off-die analog/digital converter (a thermal sensor) located on the motherboard, or a stand-alone measurement kit. The thermal diode may be used to monitor the die temperature of the processor for thermal management or instrumentation purposes but cannot be used to indicate that the maximum T_J of the processor has been reached. When using the thermal diode, a temperature offset value must be read from a processor Model Specific register (MSR) and applied. See Section 5.1.2 for more details. Please see Section 5.1.3 for thermal diode usage recommendation when the PROCHOT# signal is not asserted. Table 5-2 and Table 5-3 provide the diode interface and specifications.

Note: The reading of the external thermal sensor (on the motherboard) connected to the processor thermal diode signals, will not necessarily reflect the temperature of the hottest location on the die. This is due to inaccuracies in the external thermal sensor, on-die temperature gradients between the location of the thermal diode and the hottest location on the die, and time based variations in the die temperature measurement. Time-based variations can occur when the sampling rate of the thermal diode (by the thermal sensor) is slower than the rate at which the T_J temperature can change.

Offset between the thermal diode based temperature reading and the Intel Thermal Monitor reading may be characterized using the Intel Thermal Monitor's Automatic mode activation of thermal control circuit. This temperature offset must be taken into account when using the processor thermal diode to implement power management events.

5.1.2 Thermal Diode Offset

A temperature offset value (specified as Toffset in Table 5-3) will be programmed into a Pentium M Processor Model Specific Register (MSR). This offset is determined by using a thermal diode ideality factor mean value of n = 1.0022 (shown in Table 5-3) as a reference. This offset must be applied to the junction temperature read by the thermal diode. Any temperature adjustments due to differences between the reference ideality value of 1.0022 and the default ideality values programmed into the on-board thermal sensors, will have to be made before the above offset is applied.

Table 5-2. Thermal Diode Interface

Signal Name	Pin/Ball Number	Signal Description
THERMDA	B18	Thermal diode anode
THERMDC	A18	Thermal diode cathode

Table 5-3. Thermal Diode Specification

Symbol	Parameter	Min	Typ	Max	Unit	Notes
I_{FW}	Forward Bias Current	5		300	µA	Note 1
Toffset	Thermal diode temperature offset	-4		11	°C	2, 6
n	Reference Diode Ideality Factor used to calculate temperature offset		1.0022			Notes 2, 3, 4
R_T	Series Resistance		3.06		Ohms	2, 3, 5

NOTES:

1. Intel does not support or recommend operation of the thermal diode under reverse bias. Intel does not support or recommend operation of the thermal diode when the processor power supplies are not within their specified tolerance range.
2. Characterized at 100 °C.
3. Not 100% tested. Specified by design/characterization.
4. The ideality factor, n, represents the deviation from ideal diode behavior as exemplified by the diode equation:
   $I_{FW}=I_S*(e^{(qV_D/nkT)}-1)$
   Where I_S = saturation current, q = electronic charge, V_D = voltage across the diode, k = Boltzmann Constant, and T = absolute temperature (Kelvin).
   Value shown in the table is not the Pentium M Processor thermal diode ideality factor. It is a reference value used to calculate the Pentium M Processor thermal diode temperature offset.
5. The series resistance, R_T, is provided to allow for a more accurate measurement of the diode junction temperature. R_T as defined includes the pins of the processor but does not include any socket resistance or board trace resistance between the socket and the external remote diode thermal sensor. R_T can be used by remote diode thermal sensors with automatic series resistance cancellation to calibrate out this error term. Another application is that a temperature offset can be manually calculated and programmed into an offset register in the remote diode thermal sensors as exemplified by the equation:
   $T_{error} = [R_T*(N-1)*I_{FWmin}]/[(no/q)*\ln N$
6. Offset value is programmed in processor Model Specific Register.

5.1.3 Intel® Thermal Monitor

The Intel Thermal Monitor helps control the processor temperature by activating the TCC when the processor silicon reaches its maximum operating temperature. The temperature at which Intel Thermal Monitor activates the thermal control circuit is not user configurable and is not software visible. Bus traffic is snooped in the normal manner, and interrupt requests are latched (and serviced during the time that the clocks are on) while the TCC is active.

With a properly designed and characterized thermal solution, it is anticipated that the TCC would only be activated for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be so minor that it would not be detectable. An under-designed thermal solution that is not able to prevent excessive activation of the TCC in the anticipated ambient environment may cause a noticeable performance loss, and may affect the long-term reliability of the processor. In addition, a thermal solution that is significantly under designed may not be capable of cooling the processor even when the TCC is active continuously.

The Intel Thermal Monitor controls the processor temperature by modulating (starting and stopping) the processor core clocks or by initiating an Enhanced Intel SpeedStep technology transition when the processor silicon reaches its maximum operating temperature. The Intel Thermal Monitor uses two modes to activate the TCC: Automatic mode and On-Demand mode. If both modes are activated, Automatic mode takes precedence.

Caution: The Intel Thermal Monitor Automatic Mode mst be enabled via BIOS for the processor to be operating within specifications.

There are two automatic modes called Intel Thermal Monitor 1 and Intel Thermal Monitor 2. These modes are selected by writing values to the Model Specific registers (MSRs) of the processor. After Automatic mode is enabled, the TCC will activate only when the internal die temperature reaches the maximum allowed value for operation.

Likewise, when Intel Thermal Monitor 2 is enabled, and a high temperature situation exists, the processor will perform an Enhanced Intel SpeedStep technology transition to a lower operating point. When the processor temperature drops below the critical level, the processor will make an Enhanced Intel SpeedStep technology transition to the last requested operating point. Intel Thermal Monitor 2 is the recommended mode on the Intel® Pentium® M processors.

If a processor load based Enhanced Intel SpeedStep technology transition (through MSR write) is initiated when an Intel Thermal Monitor 2 period is active, there are two possible results:

1. If the processor load based Enhanced Intel SpeedStep technology transition target frequency is **higher** than the Intel Thermal Monitor 2 transition based target frequency, the processor load-based transition will be deferred until the Intel Thermal Monitor 2 event has been completed.

2. If the processor load-based Enhanced Intel SpeedStep technology transition target frequency is **lower** than the Intel Thermal Monitor 2 transition based target frequency, the processor will transition to the processor load-based Enhanced Intel SpeedStep technology target frequency point.

When Intel Thermal Monitor 1 is enabled, and a high temperature situation exists, the clocks will be modulated by alternately turning the clocks off and on at a 50% duty cycle. Cycle times are processor speed dependent and will decrease linearly as processor core frequencies increase. Once the temperature has returned to a non-critical level, modulation ceases and TCC goes inactive. A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near the trip point. The duty cycle is factory configured and cannot be modified. Also, automatic mode does not require any additional hardware, software drivers, or interrupt handling routines. Processor performance will be decreased by the same amount as the duty cycle when the TCC is active, however, with a properly designed and characterized thermal solution the TCC most likely will never be activated, or only will be activated briefly during the most power intensive applications.

The TCC may also be activated via On-Demand mode. If bit 4 of the ACPI Intel Thermal Monitor Control Register is written to a 1, the TCC will be activated immediately, independent of the processor temperature. When using On-Demand mode to activate the TCC, the duty cycle of the clock modulation is programmable via bits 3:1 of the same ACPI Intel Thermal Monitor Control Register. In automatic mode, the duty cycle is fixed at 50% on, 50% off, however in On-Demand mode, the duty cycle can be programmed from 12.5% on/ 87.5% off, to 87.5% on/12.5% off in 12.5% increments. On-Demand mode may be used at the same time Automatic mode is enabled, however, if the system tries to enable the TCC via On-Demand mode at the same time automatic mode is enabled **and** a high temperature condition exists, automatic mode will take precedence.

An external signal, PROCHOT# (processor hot) is asserted when the processor detects that its temperature is above the thermal trip point. Bus snooping and interrupt latching are also active while the TCC is active.

Besides the thermal sensor and thermal control circuit, the Intel Thermal Monitor feature also includes one ACPI register, one performance counter register, three model specific registers (MSR), and one I/O pin (PROCHOT#). All are available to monitor and control the state of the Intel Thermal Monitor feature. The Intel Thermal Monitor can be configured to generate an interrupt upon the assertion or deassertion of PROCHOT#.

Note: PROCHOT# will not be asserted when the processor is in the Stop Grant, Sleep, Deep Sleep, and Deeper Sleep low power states (internal clocks stopped), hence the thermal diode reading must be used as a safeguard to maintain the processor junction temperature within the 100 °C (maximum) specification. If the platform thermal solution is not able to maintain the processor junction temperature within the maximum specification, the system must initiate an orderly shutdown to prevent damage. If the processor enters one of the above low power states with PROCHOT# already asserted, PROCHOT# will remain asserted until the processor exits the Low Power state and the processor junction temperature drops below the thermal trip point.

If automatic mode is disabled, the processor will be operating out of specification. Regardless of enabling the automatic or On-Demand modes, in the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached a temperature of approximately 125 °C. At this point the FSB signal THERMTRIP# will go active. THERMTRIP# activation is independent of processor activity and does not generate any bus cycles. When THERMTRIP# is asserted, the processor core voltage must be shut down within the time specified in Chapter 3.

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