82C55A

CMOS Programmable Peripheral Interface
iAPX86 Family

DISTINCTIVE CHARACTERISTICS

- Pin compatible with NMOS 8255A
- 24 programmable I/O pins
- Fully TTL compatible
- Bus hold circuitry on all I/O ports – eliminates pull-up resistors
- Control Word Read-Back Capability
- 2.5 mA drive capability on all I/O port outputs
- Low standby power – ICC = 10 μA
- Direct bit set/reset capability

GENERAL DESCRIPTION

The 82C55A is a high performance CMOS version of the industry standard 8255A and is manufactured using a self-aligned silicon gate CMOS process. It is a general purpose programmable I/O device which may be used with many different microprocessors. There are 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. The high performance and industry standard configuration of the 82C55A make it compatible with microprocessors, such as the 80286, 80186, 8086, 8088, 8080A, and 8085AH.

Static CMOS circuit design insures low operating power. TTL compatibility of VIH = 2.0 volts over the industrial temperature range and bus hold circuitry eliminate the need for pull-up resistors. AMD's advanced CMOS process results in performance equal to or greater than existing equivalent products at a fraction of the power.

BLOCK DIAGRAM

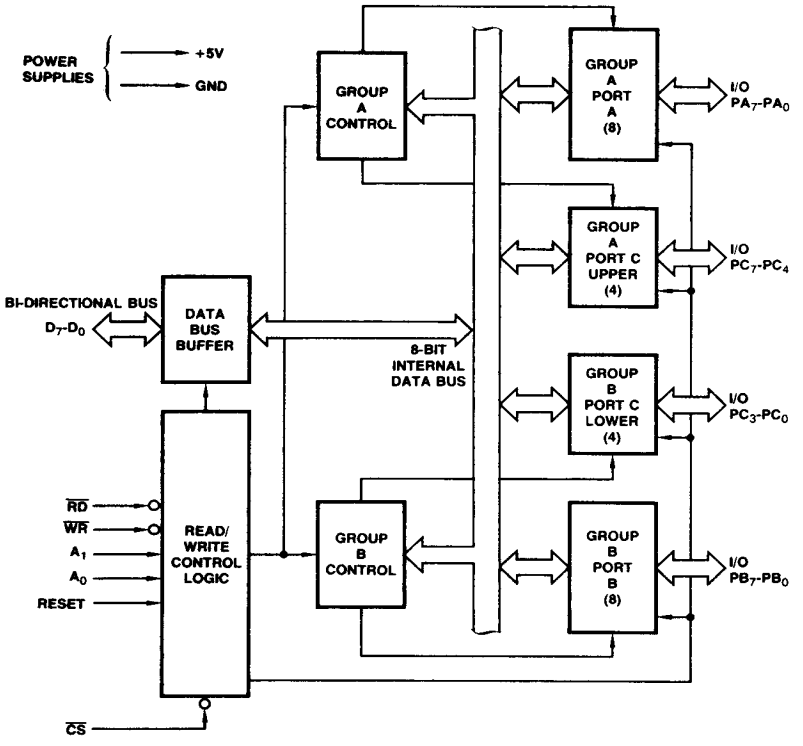

Figure 1.

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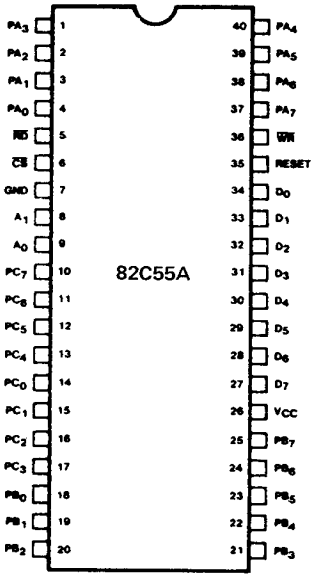
Refer to page 7-1 for Essential Information on Military Devices

CONNECTION DIAGRAM
Top View

D-40-1, P-40-1



CD005702

Figure 2.

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

82C55A

Temperature Range
Blank = Commercial 0°C to 70°C
I = Industrial −40°C to 85°C
M = Military −55°C to 125°C

40-pin Package
P = Plastic Dip
D = Ceramic Dip
J = Plastic LCC

Speed
Blank = 8MHz; T_{WW} = 60ns
-2 = 8MHz; T_{WW} = 20ns

Additional Processing
Blank = Std. Processing
B = Burn-in

DEVICE*

*A "C" in the middle of the device type denotes CMOS version of the product.

Valid Combinations	
82C55A	P, D, ID
82C55A-2	P, D, ID

Valid Combinations

Consult the local AMD sales office to confirm availability of specific valid combinations, check for newly released valid combinations and/or obtain additional data on AMD's standard military grade product.

PIN DESCRIPTION

Pin No.	Name	I/O	Pin Description
27-34	D_7-D_0	I/O	Data Bus (Bidirectional).
35	RESET	I	Reset Input.
6	$\overline{CS}$	I	Chip Select.
5	$\overline{RD}$	I	Read Input.
36	$\overline{WR}$	I	Write Input.
9, 8	A_0, A_1	I	Port Address.
37-40, 1-4	PA_7-PA_0	I/O	Port A (Bit).
25-18	PB_7-PB_0	I/O	Port B (Bit).
10-13, 17-14	PC_7-PC_0	I/O	Port C (Bit).
26	V_{CC}		+5 Volts.
7	GND		0 Volts.

DETAILED DESCRIPTION

General

The 82C55A is a programmable peripheral interface (PPI) device designed for use in microcomputer systems. Its function is that of a general purpose I/O component to interface peripheral equipment to the microcomputer system bus. The functional configuration of the 82C55A is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the 82C55A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and, in turn, issues commands to both of the Control Groups.

($\overline{CS}$)

Chip Select. A "LOW" on this input pin enables the communication between the 82C55A and the CPU.

($\overline{RD}$)

Read. A "LOW" on this input pin enables the 82C55A to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the 82C55A.

($\overline{WR}$)

Write. A "LOW" on this input pin enables the CPU to write data or control words into the 82C55A.

(A_0 and A_1)

Port Select 0 and Port Select 1. These input signals, in conjunction with the $\overline{RD}$ and $\overline{WR}$ inputs, control the selection of one of the three ports or the control word registers. They are normally connected to the least significant bits of the address bus (A_0 and A_1).

82C55A BASIC OPERATION

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	INPUT OPERATION (READ)
0	0	0	1	0	PORT A → DATA BUS
0	1	0	1	0	PORT B → DATA BUS
1	0	0	1	0	PORT C → DATA BUS
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	DATA BUS → PORT A
0	1	1	0	0	DATA BUS → PORT B
1	0	1	0	0	DATA BUS → PORT C
1	1	1	0	0	DATA BUS → CONTROL
					DISABLE FUNCTION
X	X	X	X	1	DATA BUS → 3-STATE
1	1	0	1	0	ILLEGAL CONDITION
X	X	1	1	0	DATA BUS → 3-STATE

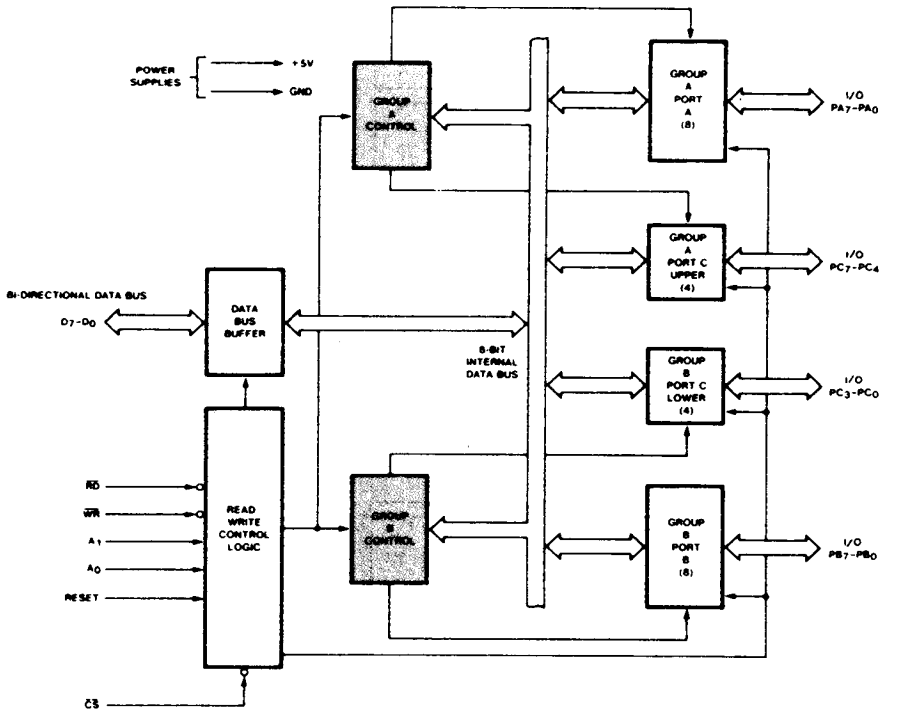


Figure 3. 82C55A Block Diagram Showing Data Bus Buffer and Read/Write Control Logic Functions

(RESET)

Reset. A "HIGH" on this input clears the control register, and all ports (A, B, C) are set to the input mode.

Group A and Group B Controls

The functional configuration of each port is programmed by the system's software. In essence, the CPU "outputs" a control word to the 82C55A. The control word contains information, such as "mode," "bit set," "bit reset," etc., that initializes the functional configuration of the 82C55A.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A — Port A and Port C upper (C7 – C4)

Control Group B — Port B and Port C lower (C3 – C0)

The Control Word Register can be both written and read as shown in the address decode table in the pin descriptions. Figure 6 shows the control word format for both Read and Write operations. When the control word is read, bit D7 will always be a logic "1," as this implies control word mode information.

Ports A, B, and C

The 82C55A contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system's software, but each has its own special features or "personality" to further enhance the power and flexibility of the 82C55A.

Port A. One 8-bit data output latch/buffer and one 8-bit data input latch. Both "pull-up" and "pull-down" bus hold devices are present on Port A.

Port B. One 8-bit data input/output latch/buffer and one 8-bit data input buffer. Only "pull-up" bus hold devices are present on Port B.

Port C. One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with Ports A and B. Only "pull-up" bus hold devices are present on Port C.

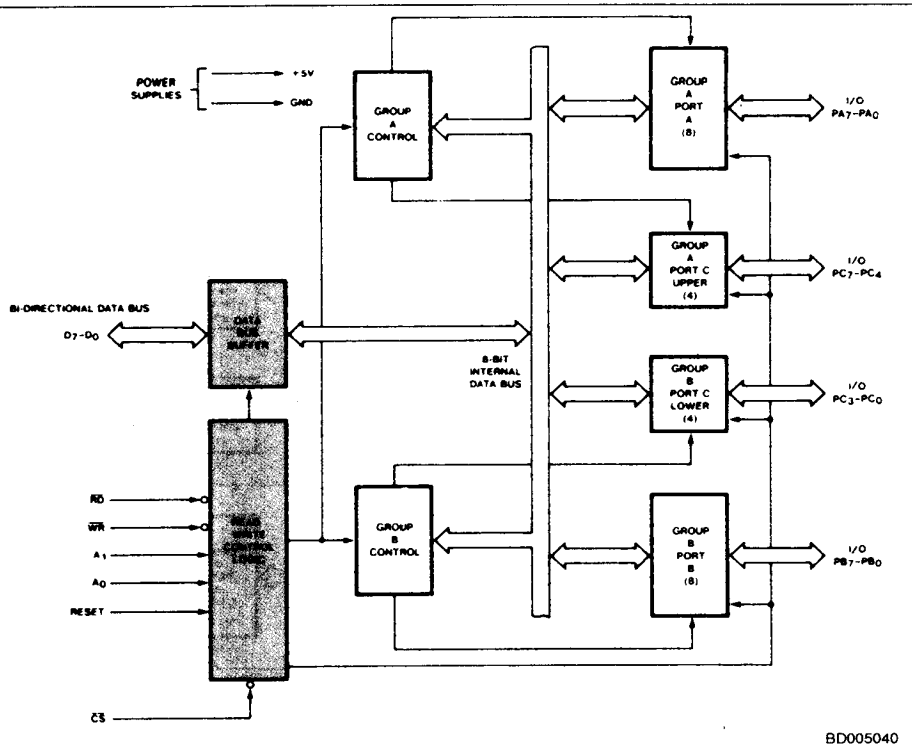


Figure 4. 82C55A Block Diagram Showing Group A and Group B Control Functions

OPERATIONAL DESCRIPTION

Mode Selection

There are three basic modes of operation that can be selected by the system software:

Mode 0 — Basic Input/Output
Mode 1 — Strobed Input/Output
Mode 2 — Bi-Directional Bus

When the reset input goes "HIGH" all ports will be set to the input mode (i.e., all 24 lines will be in the high-impedance state). After the reset is removed, the 82C55A can remain in the input mode with no additional initialization required. This eliminates the need for pull-up or pull-down resistors in "all CMOS" designs. During the execution of the system program, any of the other modes may be selected using a single output instruction. This allows a single 82C55A to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance, Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results; Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

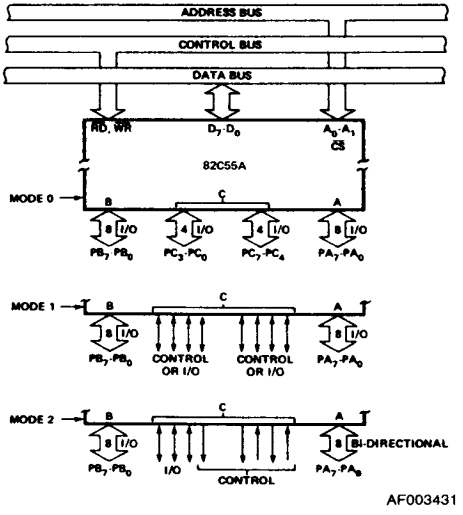


Figure 5. Basic Mode Definitions and Bus Interface

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Refer to page 7-1 for Essential Information on Military Devices

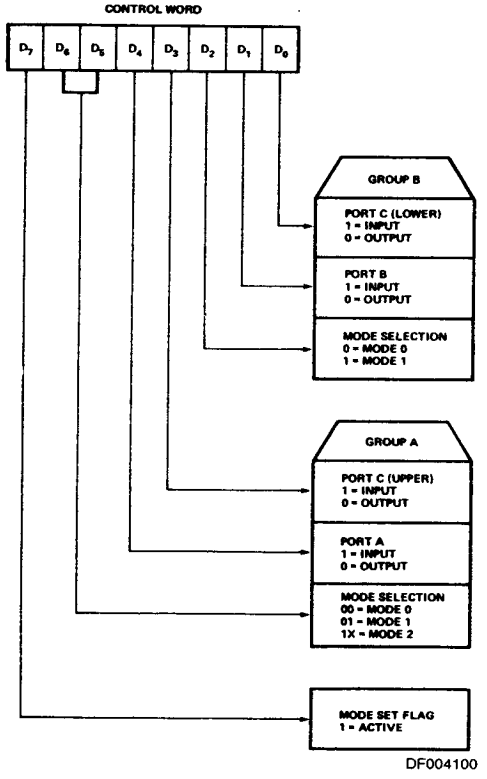


Figure 6. Mode Definition Format

The mode definitions and possible mode combinations may seem confusing at first, but after a cursory review of the complete device operation, a simple, logical I/O approach will surface. The design of the 82C55A has taken into account things, such as efficient PC board layout, control signal definition vs PC layout, and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction. This feature reduces software requirements in Control-based applications.

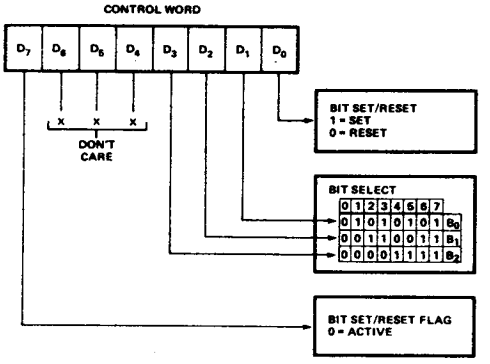


Figure 7. Bit Set/Reset Format

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using Bit Set/Reset operation just as if they were data output ports.

Interrupt Control Functions

When the 82C55A is programmed to operate in Mode 1 or Mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from Port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of Port C.

This function allows the Programmer to disallow or allow a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.

INTE flip-flop definition:

(BIT-SET) — INTE is SET — Interrupt enable
(BIT-RESET) — INTE is RESET — Interrupt disable

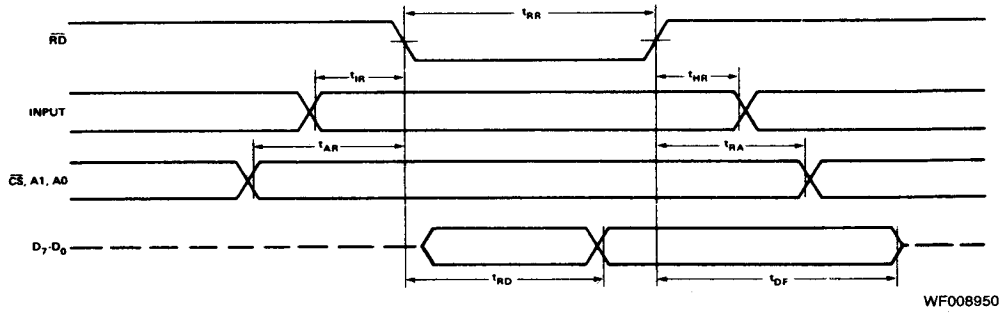
Note: All Mask flip-flops are automatically reset during mode selection and device Reset.

Operating Modes

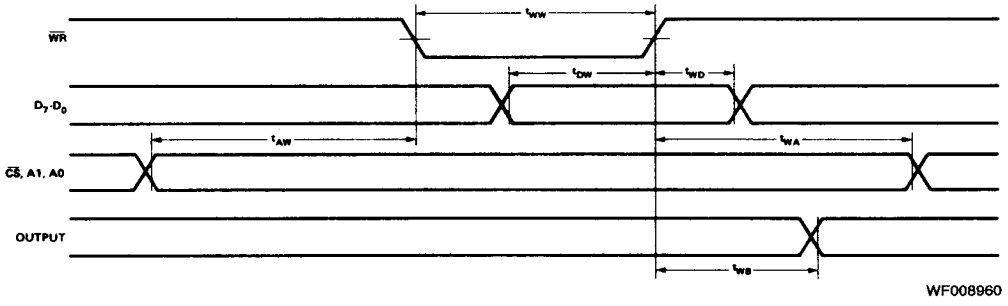
MODE 0 (Basic Input/Output). This functional configuration provides simple input and output operations for each of the three ports. No "handshaking" is required; data is simply written to or read from a specified port.

Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports.
- Any port can be input or output.
- Outputs are latched.
- Inputs are not latched.
- 16 different Input/Output configurations are possible in this Mode.



MODE 0 (Basic Input)



MODE 0 (Basic Output)

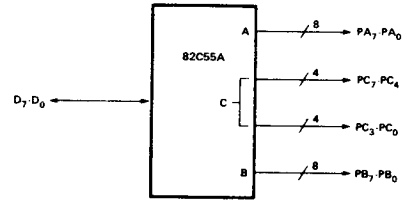
MODE 0 Port Definition

A		B		GROUP A			GROUP B	
D_4	D_3	D_1	D_0	PORT A	PORT C (UPPER)	#	PORT B	PORT C (LOWER)
0	0	0	0	OUTPUT	OUTPUT	0	OUTPUT	OUTPUT
0	0	0	1	OUTPUT	OUTPUT	1	OUTPUT	INPUT
0	0	1	0	OUTPUT	OUTPUT	2	INPUT	OUTPUT
0	0	1	1	OUTPUT	OUTPUT	3	INPUT	INPUT
0	1	0	0	OUTPUT	INPUT	4	OUTPUT	OUTPUT
0	1	0	1	OUTPUT	INPUT	5	OUTPUT	INPUT
0	1	1	0	OUTPUT	INPUT	6	INPUT	OUTPUT
0	1	1	1	OUTPUT	INPUT	7	INPUT	INPUT
1	0	0	0	INPUT	OUTPUT	8	OUTPUT	OUTPUT
1	0	0	1	INPUT	OUTPUT	9	OUTPUT	INPUT
1	0	1	0	INPUT	OUTPUT	10	INPUT	OUTPUT
1	0	1	1	INPUT	OUTPUT	11	INPUT	INPUT
1	1	0	0	INPUT	INPUT	12	OUTPUT	OUTPUT
1	1	0	1	INPUT	INPUT	13	OUTPUT	INPUT
1	1	1	0	INPUT	INPUT	14	INPUT	OUTPUT
1	1	1	1	INPUT	INPUT	15	INPUT	INPUT

MODE 0 Configurations

CONTROL WORD # 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	0	0



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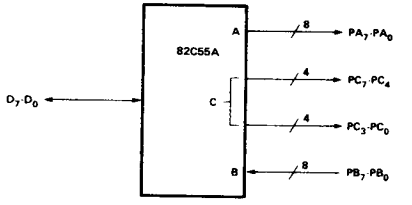
CONTROL WORD # 2

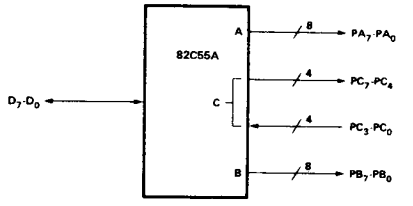
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	1	0



LS001471

CONTROL WORD #1

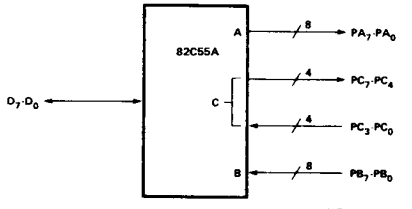
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	0	1



LS001481

CONTROL WORD #3

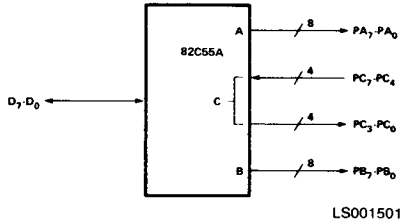
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	1	1



LS001491

CONTROL WORD # 4

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	0	0



LS001501

CONTROL WORD # 8

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
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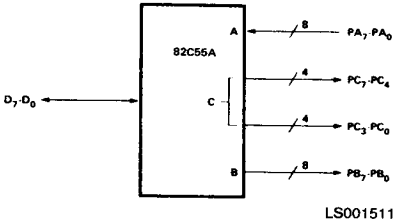
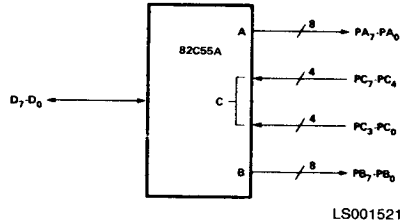


LS001511

CONTROL WORD #5

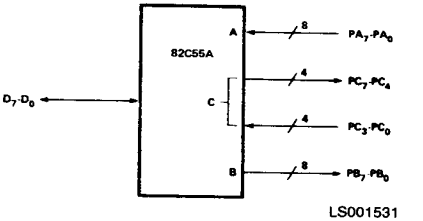
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	0	1



LS001521

CONTROL WORD #9

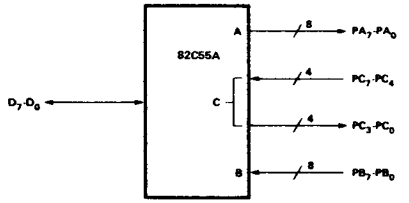
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	0	1



LS001531

CONTROL WORD #6

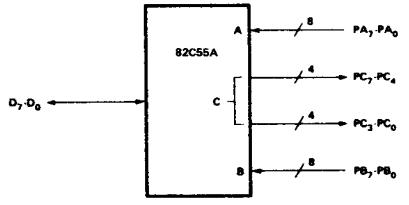
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	1	0



LS001541

CONTROL WORD #10

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	1	0



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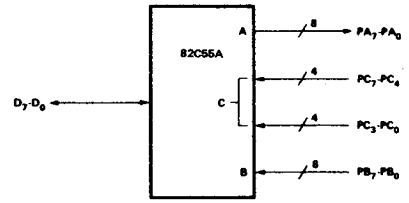
CONTROL WORD #7

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	1	1



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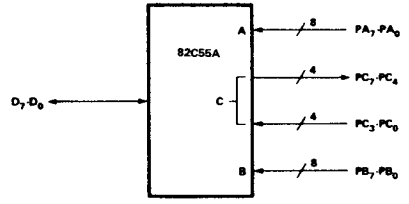
CONTROL WORD #11

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	1	1



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CONTROL WORD #12

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
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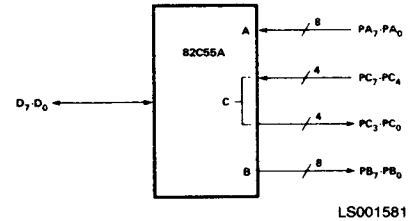
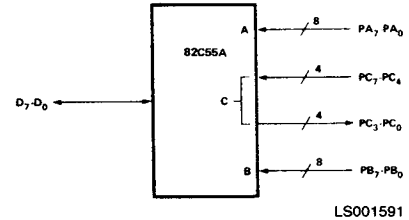


LS001581

CONTROL WORD #14

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	1	0	1	0



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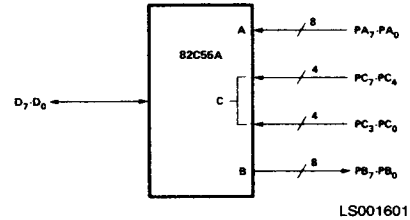
CONTROL WORD #13

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	1	0	0	1



LS001601

CONTROL WORD #15

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
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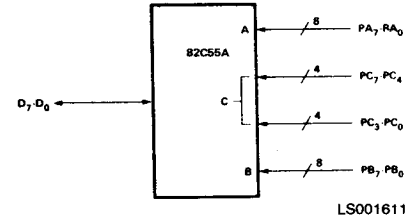

LS001611

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Refer to page 7-1 for Essential Information on Military Devices

Operating Modes

MODE 1 (Strobed Input/Output). This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In mode 1, Port A and Port B use the lines on Port C to generate or accept these "handshaking" signals.

Mode 1 Basic Functional Definitions:

- Two Groups (Group A and Group B)
- Each group contains one 8-bit data port and one 4-bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.

Input Control Signal Definition

STB (Strobe Input). A "LOW" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "HIGH" on this output indicates that the data has been loaded into the input latch — in essence, an acknowledgement. IBF is set by $\overline{STB}$ input being LOW and is reset by the rising edge of the $\overline{RD}$ input.

INTR (Interrupt Request)

A "HIGH" on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set when the $\overline{STB}$ is a "one," IBF is a "one," and INTE is a "one." It is reset by the falling edge of $\overline{RD}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A
Controlled by bit set/reset of PC_4.

INTE B
Controlled by bit set/reset of PC_2.

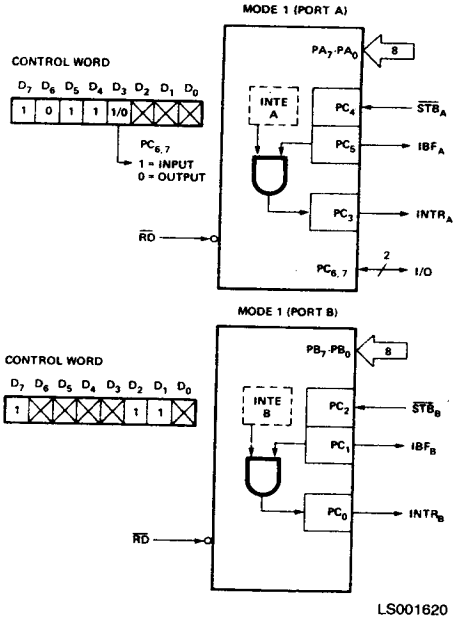


Figure 8. MODE 1 Input

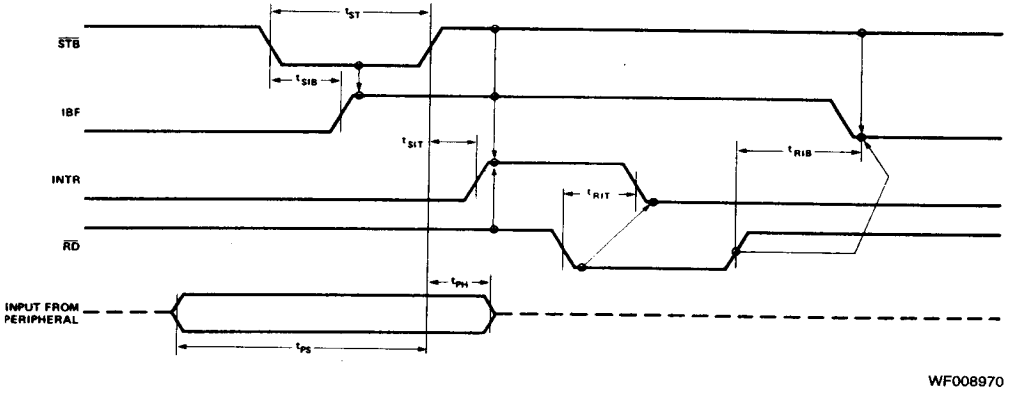


Figure 9. MODE 1 (Strobed Input)

Output Control Signal Definition

$\overline{OBF}$ (Output Buffer Full F/F). The $\overline{OBF}$ output will go "LOW" to indicate that the CPU has written data out to the specified port. The $\overline{OBF}$ F/F will be set by the rising edge of the $\overline{WR}$ input and reset by $\overline{ACK}$ Input being LOW.

$\overline{ACK}$ (Acknowledge Input). A "LOW" on this input informs the 82C55A that the data from Port A or Port B has been accepted – in essence, a response from the peripheral device indicating that it has received the data output by the CPU.

INTR (Interrupt Request). A "HIGH" on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when $\overline{ACK}$ is a "one," $\overline{OBF}$ is a "one," and INTE is a "one." It is reset by the falling edge of $\overline{WR}$.

INTE A
Controlled by bit set/reset of PC_6.

INTE B
Controlled by bit set/reset of PC_2.

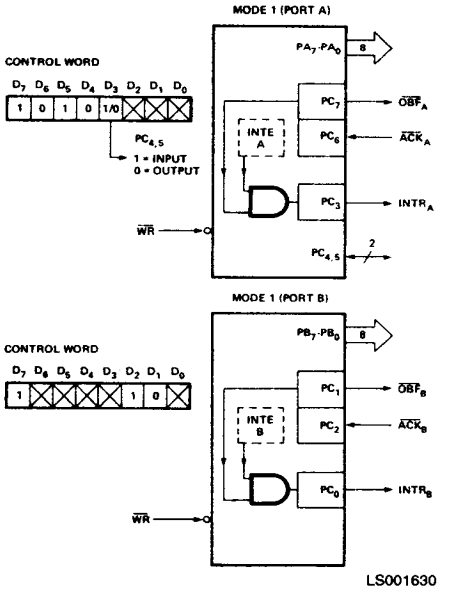


Figure 10. MODE 1 Output

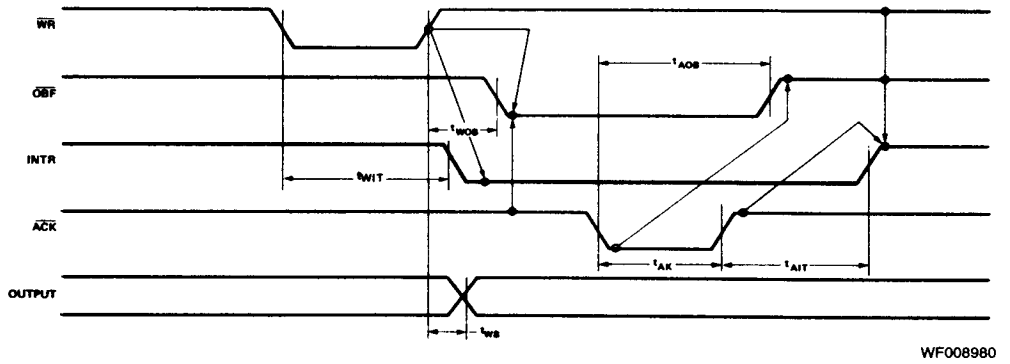
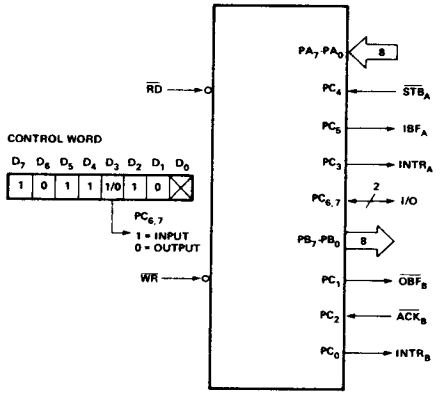


Figure 11. Mode 1 (Strobed Output)

Combinations of MODE 1

Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.



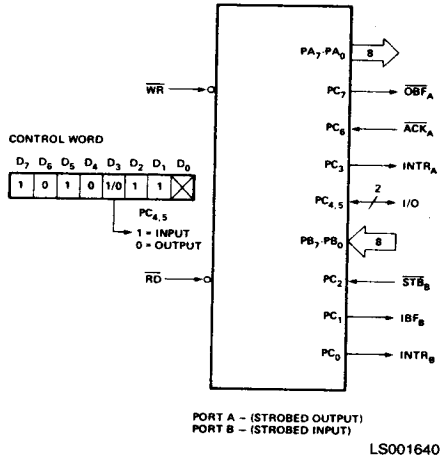


Figure 12. Combinations of MODE 1

Operating Modes

MODE 2 (Strobed Bidirectional Bus I/O). This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline in a similar manner to MODE 1. Interrupt generation and enable/disable functions are also available.

MODE 2 Basic Functional Definitions:

- Used in Group A only.
- One 8-bit, bi-directional bus Port (Port A) and a 5-bit control Port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A).

Bidirectional Bus I/O Control Signal Definition

INTR (Interrupt Request). A HIGH on this output can be used to interrupt the CPU for both input or output operations.

Output Operations

$\overline{OBF}$ (Output Buffer Ful). The $\overline{OBF}$ output will go "LOW" to indicate that the CPU has written data out to Port A.

$\overline{ACK}$ (Acknowledge). A "LOW" on this input enables the tri-state output buffer of Port A to send out the data. Otherwise, the output buffer will be in the high-impedance state.

INTE 1 (The INTE Flip-Flop Associated with $\overline{OBF}$). Controlled by bit set/reset of PC_6.

Input Operations

$\overline{STB}$ (Strobe Input). A "LOW" on this input loads data into the input latch.

IBF (Input Buffer Full F/F). A "HIGH" on this output indicates that data has been loaded into the input latch.

INTE 2 (The INTE Flip-Flop Associated with IBF). Controlled by bit set/reset of PC_4.

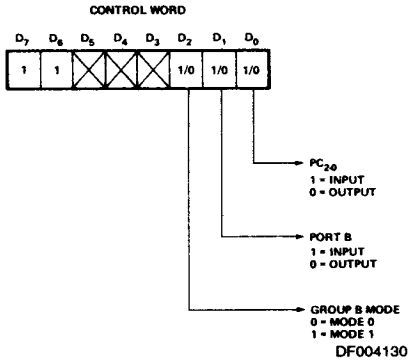


Figure 13. MODE Control Word

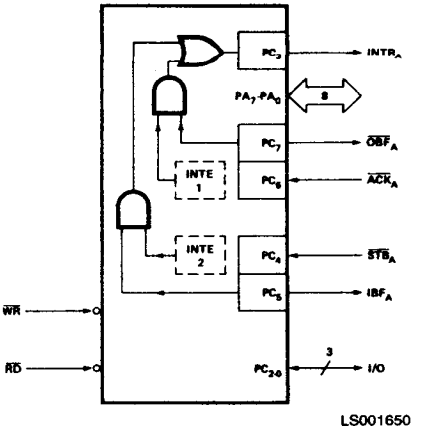


Figure 14. MODE 2

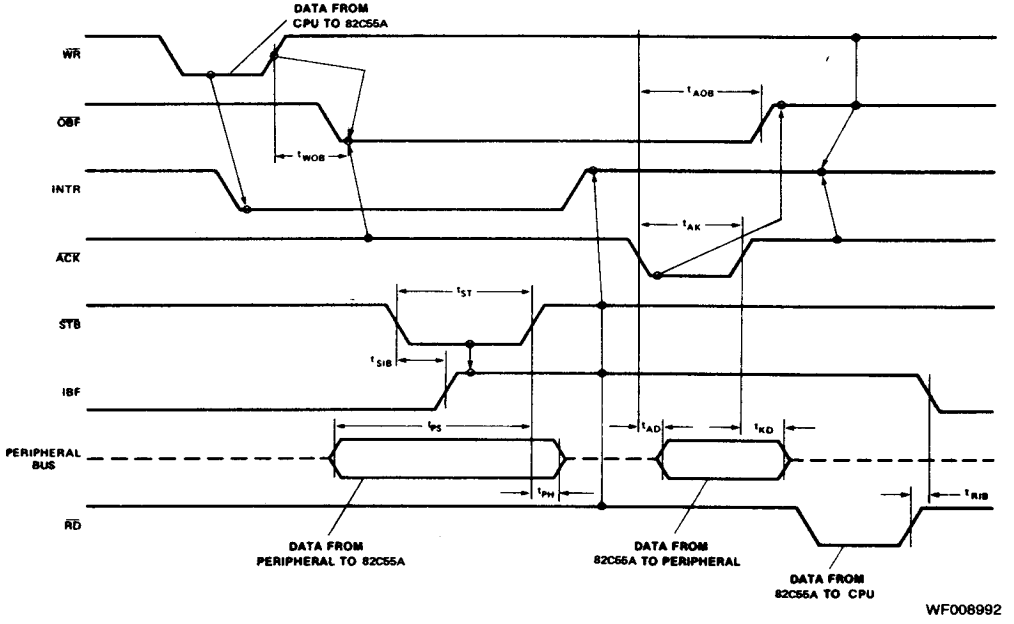
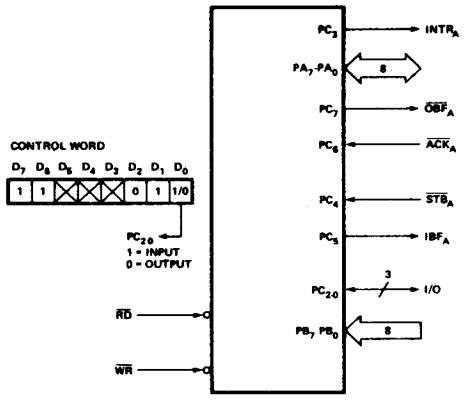


Figure 15. MODE 2 (Bidirectional)

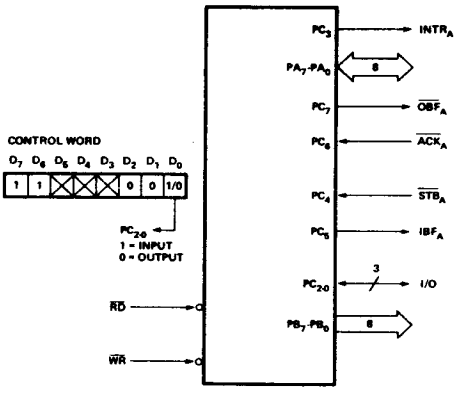
Note: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible ($INTR = IBF \cdot \overline{MASK} \cdot \overline{STB} \cdot \overline{RD} + \overline{OBF} \cdot \overline{MASK} \cdot \overline{ACK} \cdot \overline{WR}$).

MODE 2 AND MODE 0 (INPUT)



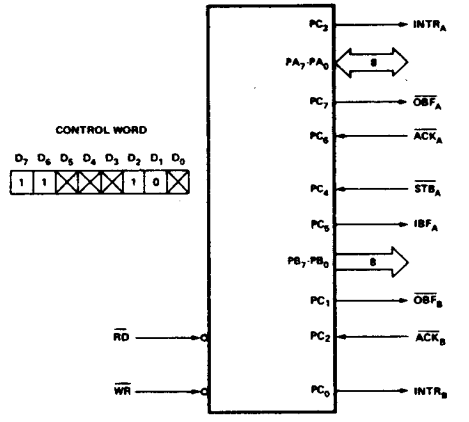
LS001671

MODE 2 AND MODE 0 (OUTPUT)



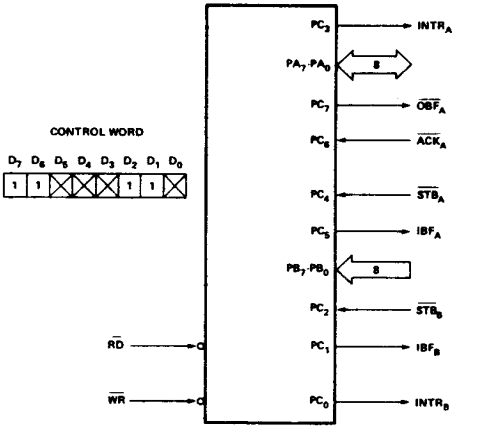
LS001661

MODE 2 AND MODE 1 (OUTPUT)



LS001681

MODE 2 AND MODE 1 (INPUT)



LS001691

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Refer to page 7-1 for Essential Information on Military Devices

Mode Definition Summary

	MODE 0	
	IN	OUT
PA_0	IN	OUT
PA_1	IN	OUT
PA_2	IN	OUT
PA_3	IN	OUT
PA_4	IN	OUT
PA_5	IN	OUT
PA_6	IN	OUT
PA_7	IN	OUT
PB_0	IN	OUT
PB_1	IN	OUT
PB_2	IN	OUT
PB_3	IN	OUT
PB_4	IN	OUT
PB_5	IN	OUT
PB_6	IN	OUT
PB_7	IN	OUT
PC_0	IN	OUT
PC_1	IN	OUT
PC_2	IN	OUT
PC_3	IN	OUT
PC_4	IN	OUT
PC_5	IN	OUT
PC_6	IN	OUT
PC_7	IN	OUT

MODE 1	
IN	OUT
IN	OUT
IN	OUT
IN	OUT
IN	OUT
IN	OUT
IN	OUT
IN	OUT
IN	OUT
IN	OUT
IN	OUT
IN	OUT
IN	OUT
IN	OUT
IN	OUT
$INTR_B$	$INTR_B$
IBF_B	$\overline{OBF}_B$
$\overline{STB}_B$	$\overline{ACK}_B$
$INTR_A$	$INTR_A$
$\overline{STB}_A$	I/O
IBF_A	I/O
I/O	$\overline{ACK}_A$
I/O	$\overline{OBF}_A$

MODE 2
GROUP A ONLY
⟷
⟷
⟷
⟷
⟷
⟷
⟷
⟷
—
—
—
—
—
—
—
—
I/O
I/O
I/O
$INTR_A$
$\overline{STB}_A$
IBF_A
$\overline{ACK}_A$
$\overline{OBF}_A$

MODE 0 OR MODE 1 ONLY

Special Mode Combination Considerations

There are several combinations of modes possible. For any combination, some or all of the Port C lines are used for control or status. The remaining bits are either inputs or outputs as defined by a "Set Mode" command.

During a read of Port C, the state of all the Port C lines, except the $\overline{ACK}$ and $\overline{STB}$ lines, will be placed on the data bus. In place of the $\overline{ACK}$ and $\overline{STB}$ line states, flag status will appear on the data bus in the PC2, PC4, and PC6 bit positions as illustrated by Figure 18.

Through a "Write Port C" command, only the Port C pins programmed as outputs in a Mode 0 group can be written. No other pins can be affected by a "Write Port C" command, nor can the interrupt enable flags be accessed. To write to any Port C output programmed as an output in a Mode 1 group or to change an interrupt enable flag, the "Set/Reset Port C Bit" command must be used.

With a "Set/Reset Port C Bit" command, any Port C line programmed as an output (including INTR, IBF and $\overline{OBF}$) can be written, or an interrupt enable flag can be either set or reset. Port C lines programmed as inputs, including $\overline{ACK}$ and $\overline{STB}$ lines, associated with Port C are not affected by a "Set/Reset Port C Bit" command. Writing to the corresponding Port C bit positions of the $\overline{ACK}$ and $\overline{STB}$ lines with the "Set/Reset Port C Bit" command will affect the Group A and Group B interrupt enable flag, as illustrated in Figure 18.

Reading Port C Status

In Mode 0, Port C transfers data to or from the peripheral device. When the 82C55A is programmed to function in Modes 1 or 2, Port C generates or accepts "handshaking" signals with the peripheral device. Reading the contents of Port C allows the programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

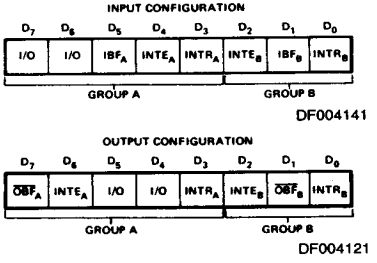


Figure 17. MODE 1 Status Word Format

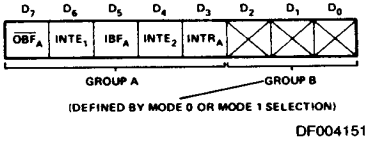


Figure 17a. MODE 2 Status Word Format

Interrupt Enable Flag	Position	Alternate Port C Pin Signal (Mode)
INTE B	PC2	$\overline{ACK}_B$ (Output Mode 1) or $\overline{STB}_B$ (Input Mode 1)
INTE A2	PC4	$\overline{STB}_A$ (Input Mode 1 or Mode 2)
INTE A1	PC6	$\overline{ACK}_A$ (Output Mode 1 or Mode 2)

Figure 18. Interrupt Enable Flags in Modes 1 and 2

APPLICATIONS INFORMATION

The 82C55A is a very powerful tool for interfacing peripheral equipment to the microcomputer system. It represents the optimum use of available pins and is flexible enough to interface almost any I/O device without the need for additional external logic.

Each peripheral device in a microcomputer system usually has a "service routine" associated with it. The routine manages the software interface between the device and the CPU. The functional definition of the 82C55A is programmed by the I/O service routine and becomes an extension of the system software. By examining the I/O devices interface characteristics for both data transfer and timing and matching this information to the examples and tables in the detailed operational description, a control word can easily be developed to initialize the 82C55A to exactly "fit" the application. Figures 19 through 25 present a few examples of typical applications of the 82C55A.

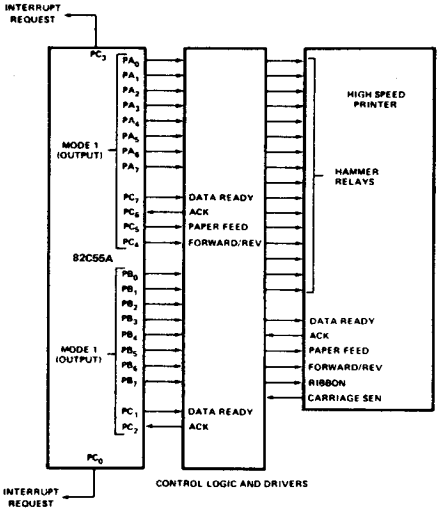
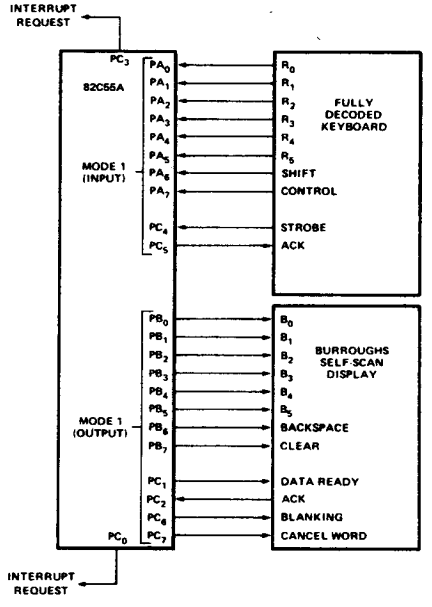
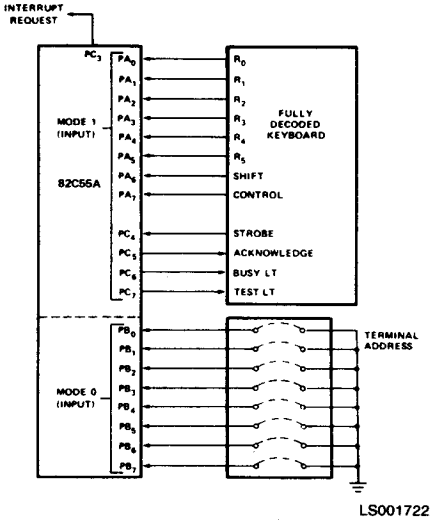


Figure 19. Printer Interface LS001712



LS001702

Figure 20. Keyboard and Display Interface



LS001722

Figure 21. Keyboard and Terminal Address Interface

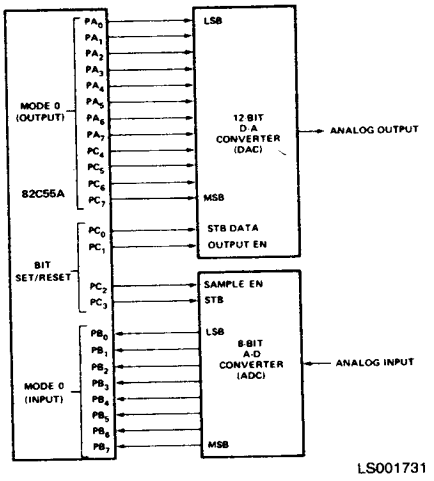


Figure 22. Digital to Analog, Analog to Digital

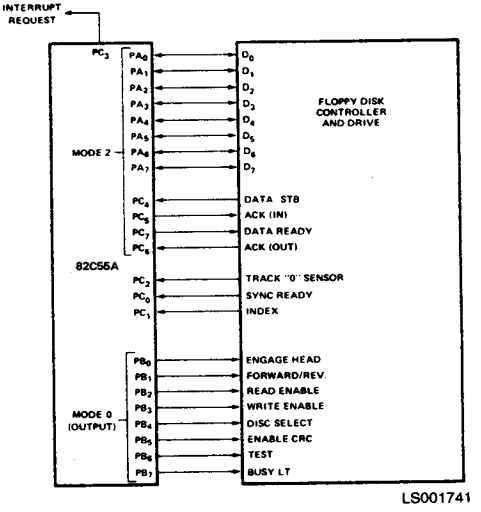


Figure 23. Basic CRT Controller Interface

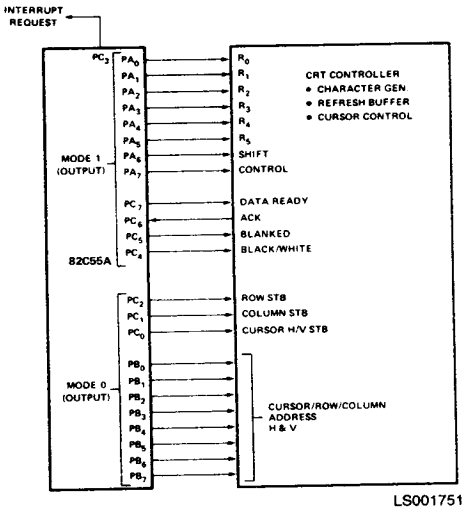


Figure 24. Basic Floppy Disc Interface

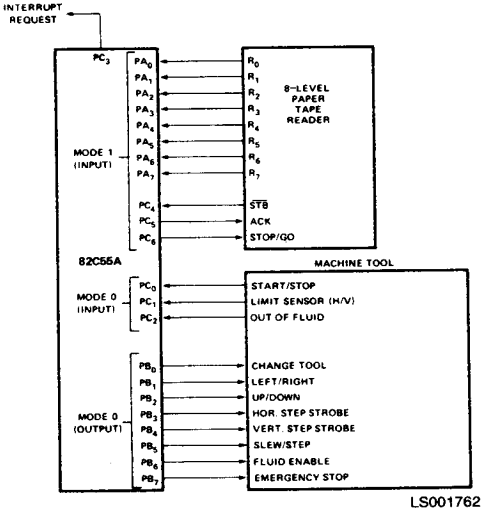


Figure 25. Machine Tool Controller Interface

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
V_{CC} with Respect to V_{SS} ..... −0.5 to +7.0V
All Signal Voltages with
Respect to V_{SS} ..... −0.5 to +7.0V
Power Dissipation 1.0W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Part Number	T_A	V_{CC}
82C55A-2, 82C55A	0°C to 70°C	5V ±10%

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

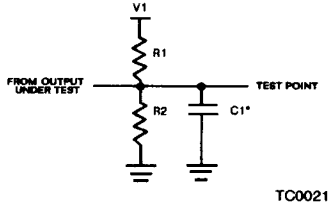
Parameters	Description	Test Conditions	Min	Max	Units
VIH	Logical One Input Voltage		2.0	V_{CC}	V
VIL	Logical Zero Input Voltage		−.5	0.8	V
VOH	Logical One Output Voltage	IOH = −2.5mA IOH = −100μA	3.0 VCC − 0.4		V V
VOL	Logical Zero Output Voltage	IOL = +2.5mA		0.4	V
IIL	Input Leakage Current	OV ≤ VIN ≤ VCC	−1.0	±10	μA
IO	I/O Pin Leakage Current	OV ≤ VO ≤ VCC	−10.0	10.0	μA
IBHH	Bus Hold High Leakage Current	VO = 3.0V Ports A, B, C	−50	−300	μA
IBHL	Bus Hold Low Leakage Current	VO = 1.0V Port A Only	+50	+300	μA
IDAR	Darlington Drive Current	Ports A, B, C Test Condition 3	−2.0		mA
ICC	Power Supply Current	VCC = 5.5V VIN = VCC or GND Outputs Open		10	μA

CAPACITANCE T_A = 25°C; VCC = GND = 0V; VIN = +5V or GND

Parameters	Description	Test Conditions	Min	Max	Units
CIN*	Input Capacitance	FREQ = 1 MHz Unmeasured pins returned to GND		10	pf
CI/O*	I/O Pin Capacitance			20	pf

* Guaranteed and sampled, but not 100% tested

SWITCHING TEST CIRCUIT

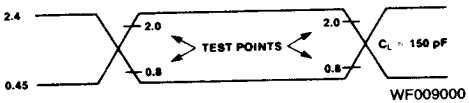


TC002170

TEST CONDITION DEFINITION TABLE

TEST CONDITION	V1	R1	R2	C1
1	1.7V	523Ω	OPEN	150 pf
2	5.0V	2KΩ	1.7KΩ	50 pf
3	1.5V	750Ω	OPEN	OPEN

SWITCHING TEST INPUT WAVEFORM



WF009000

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

Bus Parameters

READ

Parameters	Description	Test Conditions	Min	Max	Units
tAR	Address Stable Before READ		0		ns
tRA	Address Stable After READ		0		ns
tRR	READ Pulse Width		150		ns
tRD	Data Valid From READ	1		100	ns
tDF	Data Float After READ	2	10	75	ns
tRV	Time Between READs and/or WRITE		300		ns

WRITE

Parameters	Description	Test Conditions	Min	Max	Units
tAW	Address Stable Before WRITE		0		ns
tWA	Address Stable After WRITE	82C55A-2: Ports A, B, C	20		ns
		82C55A: Ports A, B	20		ns
		82C55A: Port C	60		ns
tWW	WRITE Pulse Width		100		ns
tDW	Data Valid to WRITE High		100		ns
tWD	Data Valid After WRITE High	82C55A-2: Ports A, B, C	30		ns
		82C55A: Ports A, B	30		ns
		82C55A: Port C	60		ns

OTHER TIMINGS

Parameters	Description	Test Conditions	Min	Max	Units
tWB	WR = 1 to Output	1		350	ns
tIR	Peripheral Data Before RD		0		ns
tHR	Peripheral Data After RD		0		ns
tAK	ACK Pulse Width		100		ns
tST	STB Pulse Width		100		ns
tPS	Per. Data Before STB High		20		ns
tPH	Per. Data After STB High		50		ns
tAD	ACK = 0 to Output	1		175	ns
tKD	ACK = 1 to Output Float	2	20	250	ns
tWOB	WR = 1 to OBF = 0	1		150	ns
tAOB	ACK = 0 to OBF = 1	1		150	ns
tSIB	STB = 0 to IBF = 1	1		150	ns
tRIB	RD = 1 to IBF = 0	1		150	ns
tRIT	RD = 0 to INTR = 0	1		200	ns
tSIT	STB = 1 to INTR = 1	1		150	ns
tAIT	ACK = 1 to INTR = 1	1		150	ns
tWIT	WR = 0 to INTR = 0	1		200	ns
tRES	Reset Pulse Width	see Note 1	500		ns

Note 1: Period of initial Reset pulse after power-on at least 50usec. Subsequent Reset pulses may be 500ns minimum.

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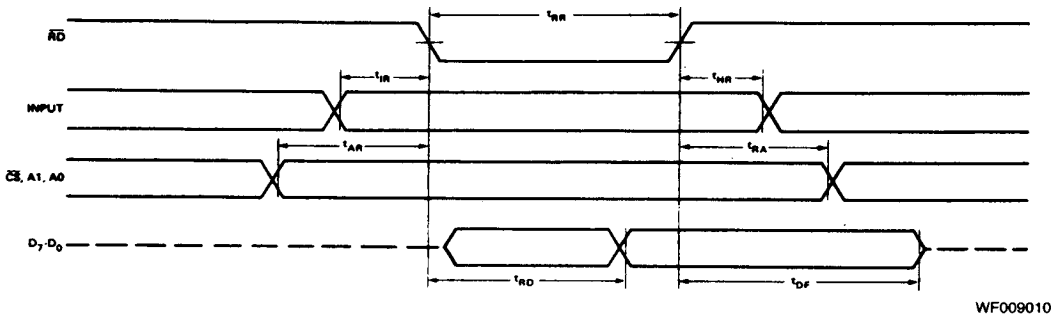
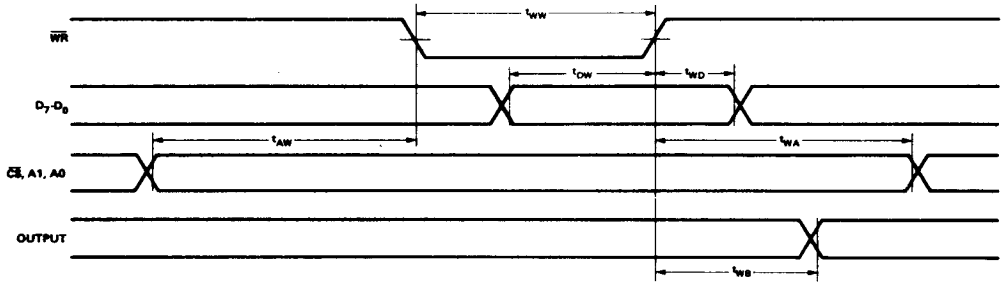
Refer to page 7-1 for Essential Information on Military Devices

SWITCHING WAVEFORMS



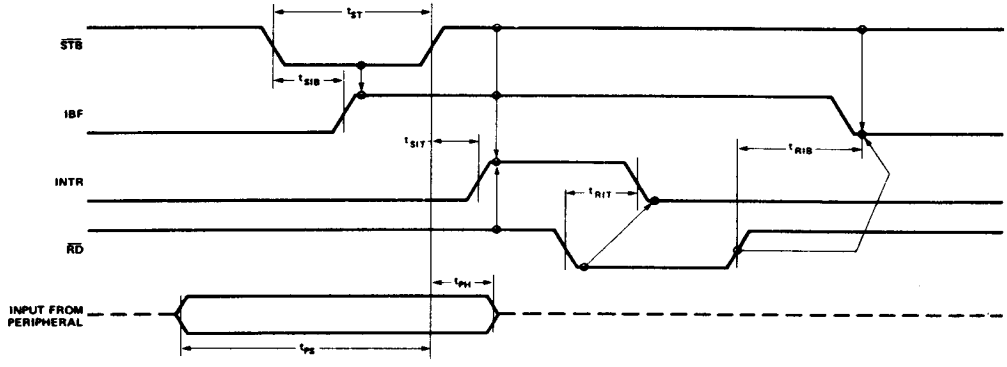
WF009010

Mode 0 (Basic Input)



WF009020

Mode 0 (Basic Output)



WF009030

Mode 1 (Strobed Input)

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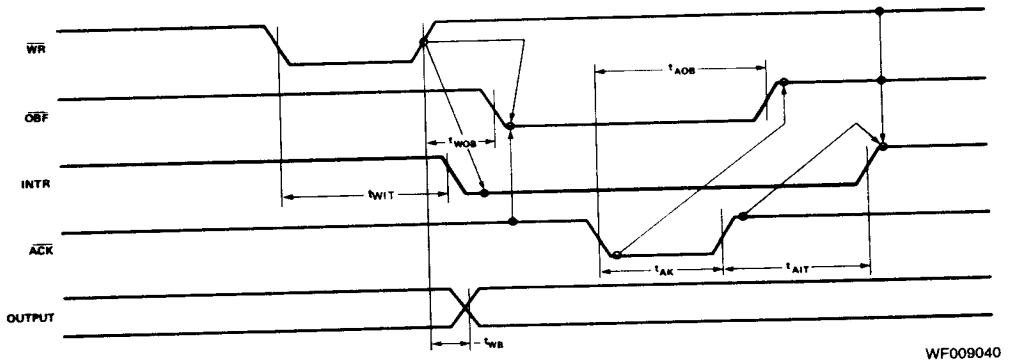
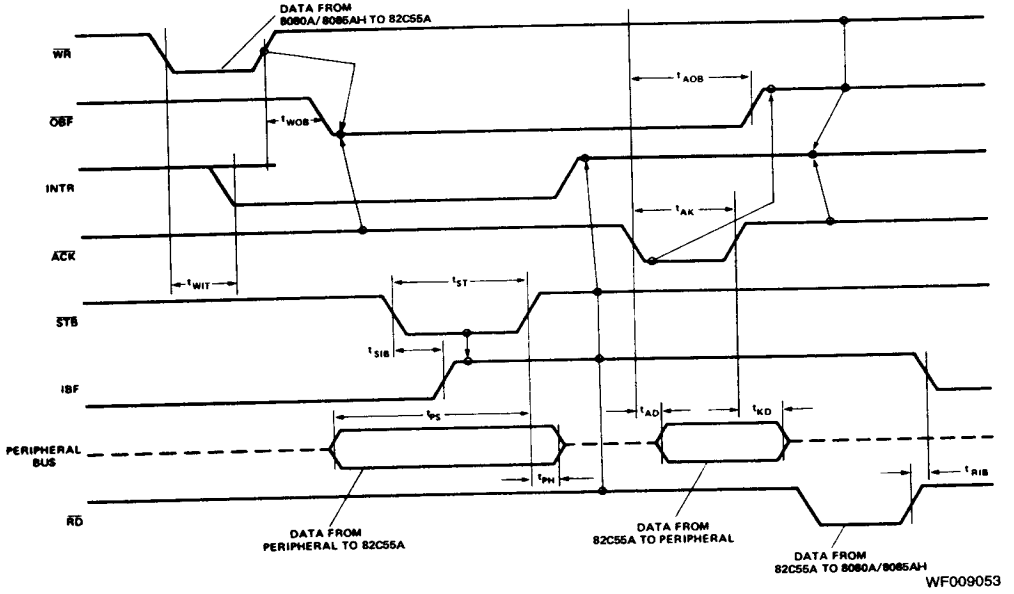
Refer to page 7-1 for Essential Information on Military Devices

SWITCHING WAVEFORMS (Cont.)



WF009040

Mode 1 (Strobed Output)



WF009053

Note: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible (INTR = IBF · $\overline{MASK}$ · $\overline{STB}$ · $\overline{RD}$ + $\overline{OBF}$ · $\overline{MASK}$ · $\overline{ACK}$ · $\overline{WR}$).

Mode 2 (Bidirectional)

06101A

Refer to page 7-1 for Essential Information on Military Devices