Intel® Wireless Flash Memory (W30)

28F640W30, 28F320W30, 28F128W30

Datasheet

Product Features

- **High Performance Read-While-Write/Erase**
  - Burst Frequency at 40 MHz
  - 70 ns Initial Access Speed
  - 25 ns Page-Mode Read Speed
  - 20 ns Burst-Mode Read Speed
  - Burst-Mode and Page-Mode in All Blocks and across All Partition Boundaries
  - Burst Suspend Feature
  - Enhanced Factory Programming: 3.5 µs per Word Program Time
  - Programmable WAIT Signal Polarity
- **Flash Power**
  - V_{CC} = 1.70 V – 1.90 V
  - V_{CCQ} = 2.20 V – 3.30 V
  - Standby Current (130 nm) = 8 µA (typ.)
  - Read Current = 7 mA (4 word burst, typical)
- **Flash Software**
  - 5 µs/9 µs (typ.) Program/Erase Suspend Latency Time
  - Intel® Flash Data Integrator (FDI) and Common Flash Interface (CFI) Compatible
- **Quality and Reliability**
  - Operating Temperature: –40 °C to +85 °C
  - 100K Minimum Erase Cycles
  - 130 nm ETOX™ VIII Process
  - 180 nm ETOX™ VII Process
- **Flash Architecture**
  - Multiple 4-Mbit Partitions
  - Dual Operation: RWW or RWE
  - Parameter Block Size = 4-Kword
  - Main block size = 32-Kword
  - Top or Bottom Parameter Blocks
- **Flash Security**
  - 128-bit Protection Register: 64 Unique Device Identifier Bits; 64 User OTP Protection Register Bits
  - Absolute Write Protection with V_{PP} at Ground
  - Program and Erase Lockout during Power Transitions
  - Individual and Instantaneous Block Locking/Unlocking with Lock-Down
- **Density and Packaging**
  - 130 nm: 32Mb, 64Mb, and 128Mb in VF BGA Package; 64Mb, 128Mb in QUAD+ Package
  - 180 nm: 32Mb and 128Mb Densities in VF BGA Package; 64Mb Density in µBGA* Package
  - 56 Active Ball Matrix, 0.75 mm Ball-Pitch
  - 16-bit Data Bus

The Intel® Wireless Flash Memory (W30) device combines state-of-the-art Intel® Flash technology to provide a versatile memory solution for high performance, low power, board constraint memory applications. The W30 flash memory device offers a multi-partition, dual-operation flash architecture that enables the flash device to read from one partition while programming or erasing in another partition. This Read-While-Write or Read-While-Erase capability makes it possible to achieve higher data throughput rates compared to single partition devices. Two processors can interleave code execution, because program and erase operations can now occur as background processes.

The W30 flash memory device incorporates an Enhanced Factory Programming (EFP) mode to improve 12 V factory programming performance. This feature helps eliminate manufacturing bottlenecks associated with programming high-density flash memory devices. The EFP program time is 3.5 µs per word, compared to the standard factory program time of 8.0 µs per word, so EFP mode saves significant factory programming time for improved factory efficiency.

The W30 flash memory device also includes block lock-down and programmable WAIT signal polarity, and is supported by an array of software tools.

Notice: This document contains information on new products in production. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

Order Number: 290702, Revision: 011
June 2005

Contents

Revision History

Date of Revision	Version	Description
09/19/00	-001	Initial release
03/14/01	-002	28F3208W30 product references removed (product was discontinued) 28F640W30 product added Revised Table 2, *Signal Descriptions (*$DQ_{15–0}$, ADV#, WAIT, S-UB#, S-LB#, V_{CCQ}) Revised Section 3.1, *Bus Operations* Revised Table 5, *Command Bus Definitions*, Notes 1 and 2 Revised Section 4.2.2, *First Latency Count (*$LC_{2–0}$*);* revised Figure 6, *Data Output with LC Setting at Code 3*; added Figure 7, *First Access Latency Configuration* Revised Section 4.2.3, *WAIT Signal Polarity (WT)* Added Section 4.2.4, *WAIT Signal Function* Revised Section 4.2.5, *Data Output Configuration (DOC)* Added Figure 8, *Data Output Configuration with WAIT Signal Delay* Revised Table 13, *Status Register DWS and PWS Description* Revised entire Section 5.0, *Program and Erase Voltages* Revised entire Section 5.3, *Enhanced Factory Programming (EFP)* Revised entire Section 8.0, *Flash Security Modes* Revised entire Section 9.0, *Flash Protection Register*; added Table 15, *Simultaneous Operations Allowed with the Protection Register* Revised Section 10.1, *Power-Up/Down Characteristics* Revised Section 11.3, *DC Characteristics. C*hanged I_{CCS},I_{CCWS}, I_{CCES} Specs from 18 µA to 21µA; changed I_{CCR} Spec from 12 mA to 15 mA (burst length = 4) Added Figure 20, *WAIT Signal in Synchronous Non-Read Array Operation Waveform* Added Figure 21, *WAIT Signal in Asynchronous Page-Mode Read Operation Waveform* Added Figure 22, *WAIT Signal in Asynchronous Single-Word Read Operation Waveform* Revised Figure 23, *Write Waveform* Revised Section 12.4, *Reset Operations* Clarified Section 13.2, *SRAM Write Operation*, Note 2 Revised Section 14.0, *Ordering Information* Minor text edits
04/05/02	-003	Deleted SRAM Section Added 128M DC and AC Specifications Added Burst Suspend Added Read While Write Transition Waveforms Various text edits
04/24/02	-004	Revised Device ID Revised Write Speed Bin Various text edits
10/20/02	-005	Added Latency Count Tables Updated Packing Ball-Out and Dimension Various text edits Minor text clarifications

Date of Revision	Version	Description
01/14/03	-006	Revised Table 20, DC Current Characteristics, I_{CCS} Revised Table 20, DC Current Characteristics, I_{CCAPS} Removed Intel Burst order Minor text edits Updated Package Drawing and Dimensions
03/22/03	-007	Revised Table 22, Read Operations, t_{APA} Added note to table 15, Configuration Register Descriptions Added note to section 3.1.1, Read
11/17/03	-008	Updated Block Lock Operations (Sect. 7.1 and Fig. 11) Updated improved AC timings Added QUAD+ package option, and Appendix D Minor text edits including new product-naming conventions
05/06/04	-009	Corrected Absolute Maximum Rating for V_{CCQ} (Sect. 10.1, Table 18) Minor text edits
05/17/04	-010	Restructured the datasheet according to new layout.
06/2005	-011	Timing Diagram Nomenclature Synergy with other product families Added Ordering information Minor Text Edits

1.0 Introduction

1.1 Document Purpose

This datasheet contains information about the Intel® Wireless Flash Memory (W30) device family. Throughout this document, this device family is referred to as the W30 flash memory device.

- This chapter provides a flash memory overview.
- Chapter 2.0 through Chapter 8.0 describe the memory functionality.
- Chapter 6.0 describes the electrical specifications for extended temperature product offerings.
- Appendix A describes the Write State Machine (WSM),
- Appendix B describes the Intel® Common Flash Interface (CFI) as it applies to the W30 flash memory device.
- Appendix C provides ordering information for the Intel® Wireless Flash Memory (W30) device family.

1.2 Nomenclature

Acronyms that describe product features or usage are defined here:

- **APS** - Automatic Power Savings
- **BBA** - Block Base Address
- **CFI** - Common Flash Interface
- **CUI** - Command User Interface
- **DU** - Do not Use
- **EFP** - Enhanced Factory Programming
- **FDI** - Flash Data Integrator
- **NC** - No Connect
- **OTP** - One-Time Programmable
- **PBA** - Partition Base Address
- **RCR** - Read Configuration Register
- **RWE** - Read-While-Erase
- **RWW** - Read-While-Write
- **SCSP** - Stacked Chip Scale Package
- **SRD** - Status Register Data
- **VF BGA** - Very-thin, Fine-pitch, Ball Grid Array
- **WSM** - Write State Machine

1.3 Conventions

The following abbreviated terms and phrases are used throughout this document:

- **1.8 V** refers to the V_{CC} operating voltage range of 1.7 V – 1.9 V (except where noted).
- **3.0 V** refers to the V_{CCQ} operating voltage range of 2.2 V - 3.3 V.
- **V_{PP} = 12 V** refers to 12 V ± 5%.
- When referring to registers, the term **set** means the bit is a logical 1, and **cleared** means the bit is a logical 0.
- The terms **pin** and **signal** are often used interchangeably to refer to the external signal connections on the package. (*Ball* is the term used for BGA).
- A **word** is 2 bytes, or 16 bits.
- **Signal** names are in all CAPS (for example, WAIT).
- **Voltage** applied to the signal is subscripted (for example, V_{PP}).

Throughout this document, references are made to top, bottom, parameter, and partition. To clarify these references, the following conventions have been adopted:

- A **block** is a group of bits (or words) that erase simultaneously with one block erase instruction.
- A **main block** contains 32 Kwords.
- A **parameter block** contains 4 Kwords.
- The **Block Base Address** (BBA) is the first address of a block.
- A **partition** is a group of blocks that share erase and program circuitry and a common status register.
- The **Partition Base Address** (PBA) is the first address of a partition. For example, on a 32-Mbit top-parameter flash device, partition number 5 has a PBA of 0x140000.
- The **top partition** is located at the highest physical flash device address. This partition can be a main partition or a parameter partition.
- The **bottom partition** is located at the lowest physical flash device address. This partition can be a main partition or a parameter partition.
- A **main partition** contains only main blocks.
- A **parameter partition** contains a mixture of main blocks and parameter blocks.
- A **top parameter device** (**TPD**) has the parameter partition at the top of the memory map with the parameter blocks at the top of that partition. This flash device type was formerly referred to as a top-boot flash device.
- A **bottom parameter device** (**BPD**) has the parameter partition at the bottom of the memory map with the parameter blocks at the bottom of that partition. This flash device type was formerly referred to as a bottom-boot block flash device.

2.0 Functional Overview

This section provides an overview of the W30 flash memory device features and architecture.

2.1 Overview

The W30 flash memory device provides Read-While-Write (RWW) and Read-White-Erase (RWE) capability. This capability provides high-performance synchronous and asynchronous reads in package-compatible densities using a 16-bit data bus. Individually-erasable memory blocks are optimally sized for code and data storage. Eight 4-Kword parameter blocks are located in the parameter partition at either the top or bottom of the memory map. The rest of the memory array is grouped into 32-Kword main blocks.

The memory architecture for the W30 flash memory device consists of multiple 4-Mbit partitions, the exact number depending on the flash device density. By dividing the memory array into partitions, program or erase operations can take place simultaneously during read operations. Burst reads can traverse partition boundaries, but user application code is responsible for ensuring that burst reads do not extend into a partition that is actively programming or erasing. Although each partition has burst-read, write, and erase capabilities, simultaneous operation is limited to write or erase in one partition while other partitions are in a read mode.

Augmented erase-suspend functionality further enhances the RWW capabilities of the W30 flash memory device. An erase can be suspended to perform a program or read operation within any block, except a block that is erase-suspended. A program operation nested within a suspended erase can subsequently be suspended to read yet another memory location.

After power-up or reset, the W30 flash memory device defaults to asynchronous read configuration. Writing to the flash memory device Read Configuration Register (RCR) enables synchronous burst-mode read operation. In synchronous mode, the CLK input increments an internal burst address generator. CLK also synchronizes the flash memory device with the host CPU and outputs data on every, or on every other, valid CLK cycle after an initial latency. A programmable WAIT output signals to the CPU when data from the flash memory device is ready.

In addition to its improved architecture and interface, the W30 flash memory device incorporates Enhanced Factory Programming (EFP), a feature that enables fast programming and low-power designs. The EFP feature provides fast program performance, which can increase the manufacturing throughput of a factory.

The W30 flash memory device supports read operations at 1.8 V and erase and program operations at 1.8 V or 12 V. With the 1.8-V option, VCC and VPP can be tied together for an ultra-low-power design. In addition to voltage flexibility, the dedicated VPP input provides extensive data protection when $V_{PP} \leq V_{PPLK}$.

A 128-bit protection register can implement new security techniques and data protection schemes:

- A combination of factory-programmed and user-OTP data cells provide unique flash device identification, help implement fraud or cloning prevention schemes, or help protect content.
- Zero-latency locking/unlocking on any memory block provides instant and complete protection for critical system code and data.
- An additional block lock-down capability provides hardware protection where software commands alone cannot change the block protection status.

The flash device Command User Interface (CUI) links the system processor to the internal flash memory operation. A valid command sequence written to the CUI initiates the flash device Write State Machine (WSM) operation, which automatically executes the algorithms, timings, and verifications necessary to manage flash memory program and erase. An internal status register provides ready/busy indication results of the operation (success, fail, and so on).

Three power-saving features– Automatic Power Savings (APS), standby, and RST#– can significantly reduce power consumption.

- The flash device automatically enters APS mode following read cycle completion.
- Standby mode begins when the system deselects the flash memory by de-asserting CE#.
- Driving RST# low produces power savings similar to standby mode. It also resets the part to read-array mode (important for system-level reset), clears internal status registers, and provides an additional level of flash device write protection.

2.2 Memory Map and Partitioning

The W30 flash memory device is divided into 4-Mbit physical partitions. This partitioning allows simultaneous RWW or RWE operations, and enables users to segment code and data areas on 4-Mbit boundaries. The flash memory array is asymmetrically blocked, which enables system code and data integration within a single flash device. Each block can be erased independently in block erase mode. Simultaneous program and erase operations are not allowed; only one partition at a time can be actively programming or erasing. See Table 1, “Bottom Parameter Memory Map” on page 12 and Table 2, “Top Parameter Memory Map” on page 13.

- The 32-Mbit flash device has eight partitions.
- The 64-Mbit flash device has 16 partitions.
- The 128-Mbit flash device has 32 partitions.

Each flash device density contains one parameter partition and several main partitions. The 4-Mbit parameter partition contains eight 4-Kword parameter blocks and seven 32-Kword main blocks. Each 4-Mbit main partition contains eight 32-Kword blocks.

The bulk of the flash memory array is divided into main blocks that can store code or data, and parameter blocks that allow storage of frequently updated small parameters that are normally stored in EEPROM. By using software techniques, the word-rewrite functionality of EEPROMs can be emulated.

Table 1. Bottom Parameter Memory Map

		Size (KW)	Blk #	32 Mbit	Blk #	64 Mbit	Blk #	128 Mbit
Main Partitions	Sixteen Partitions	32					262	7F8000-7FFFFF
		: .					: .	: .
		32					135	400000-407FFF
	Eight Partitions	32			134	3F8000-3FFFFF	134	3F8000-3FFFFF
		: .			: .	: .	: .	: .
		32			71	200000-207FFF	71	200000-207FFF
	Four Partitions	32	70	1F8000-1FFFFF	70	1F8000-1FFFFF	70	1F8000-1FFFFF
		: .	: .	: .	: .	: .	: .	: .
		32	39	100000-107FFF	39	100000-107FFF	39	100000-107FFF
	One Partition	32	38	0F8000-0FFFFF	38	0F8000-0FFFFF	38	0F8000-0FFFFF
		: .	: .	: .	: .	: .	: .	: .
		32	31	0C0000-0C7FFF	31	0C0000-0C7FFF	31	0C0000-0C7FFF
	One Partition	32	30	0B8000-0BFFFF	30	0B8000-0BFFFF	30	0B8000-0BFFFF
		: .	: .	: .	: .	: .	: .	: .
		32	23	080000-087FFF	23	080000-087FFF	23	080000-087FFF
	One Partition	32	22	078000-07FFFF	22	078000-07FFFF	22	078000-07FFFF
		: .	: .	: .	: .	: .	: .	: .
		32	15	040000-047FFF	15	040000-047FFF	15	040000-047FFF
Parameter Partition	One Partition	32	14	038000-03FFFF	14	038000-03FFFF	14	038000-03FFFF
		: .	: .	: .	: .	: .	: .	: .
		32	8	008000-00FFFF	8	008000-00FFFF	8	008000-00FFFF
		4	7	007000-007FFF	7	007000-007FFF	7	007000-007FFF
		: .	: .	: .	: .	: .	: .	: .
		4	0	000000-000FFF	0	000000-000FFF	0	000000-000FFF

Table 2. Top Parameter Memory Map

		Size (KW)	Blk #	32 Mbit	Blk #	64 Mbit	Blk #	128 Mbit
Parameter Partition	One Partition	4	70	1FF000-1FFFFF	134	3FF000-3FFFFF	262	7FF000-7FFFFF
		: ·	: ·	: ·	: ·	: ·	: ·	: ·
		4	63	1F8000-1F8FFF	127	3F8000-3F8FFF	255	7F8000-7F8FFF
		32	62	1F0000-1F7FFF	126	3F0000-3F7FFF	254	7F0000-7F7FFF
		: ·	: ·	: ·	: ·	: ·	: ·	: ·
		32	56	1C0000-1C7FFF	120	3C0000-3C7FFF	248	7C0000-7C7FFF
Main Partitions	One Partition	32	55	1B8000-1BFFFF	119	3B8000-3BFFFF	247	7B8000-7BFFFF
		: ·	: ·	: ·	: ·	: ·	: ·	: ·
		32	48	18000-187FFF	112	380000-387FFF	240	780000-787FFF
	One Partition	32	47	178000-17FFFF	111	378000-37FFFF	239	778000-77FFFF
		: ·	: ·	: ·	: ·	: ·	: ·	: ·
		32	40	140000-147FFF	104	340000-347FFF	232	740000-747FFF
	One Partition	32	39	138000-13FFFF	103	338000-33FFFF	231	738000-73FFFF
		: ·	: ·	: ·	: ·	: ·	: ·	: ·
		32	32	100000-107FFF	96	300000-307FFF	224	700000-707FFF
	Four Partitions	32	31	0F8000-0FFFFF	95	2F8000-2FFFFF	223	6F8000-6FFFFF
		: ·	: ·	: ·	: ·	: ·	: ·	: ·
		32	0	000000-007FFF	64	200000-207FFF	192	600000-607FFF
	Eight Partitions	32			63	1F8000-1FFFFF	191	5F8000-5FFFFF
		: ·			: ·	: ·	: ·	: ·
		32			0	000000-007FFF	128	400000-407FFF
	Sixteen Partitions	32					127	3F8000-3FFFFF
		: ·					: ·	: ·
		32					0	000000-007FFF

3.0 Package Information

3.1 W30 Flash Memory Device – 130 nm Lithography

Figure 1. 32 Mb, 64 Mb, and 128 Mb VF BGA Package Drawing

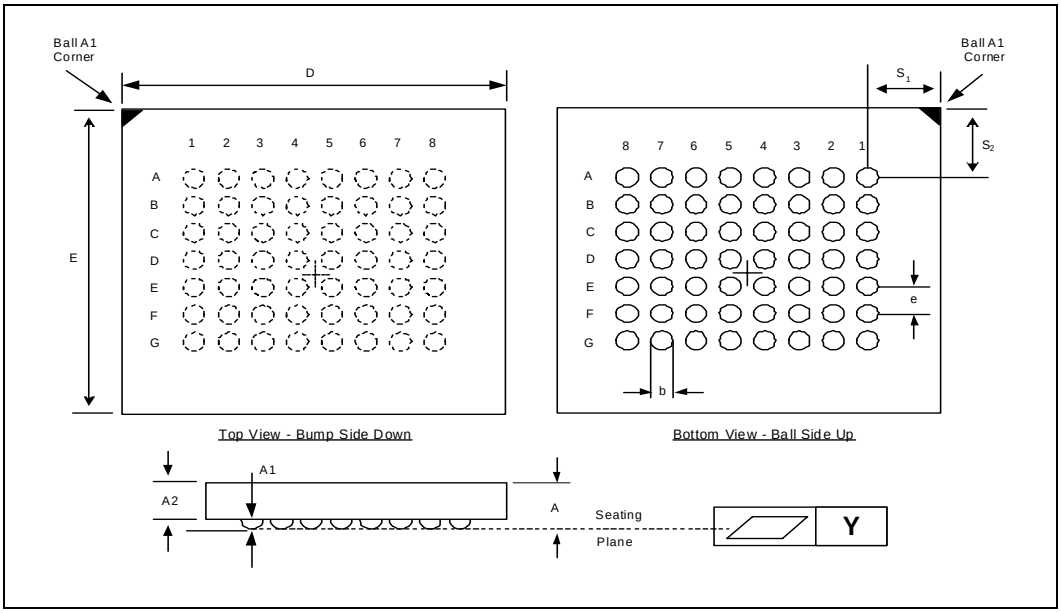
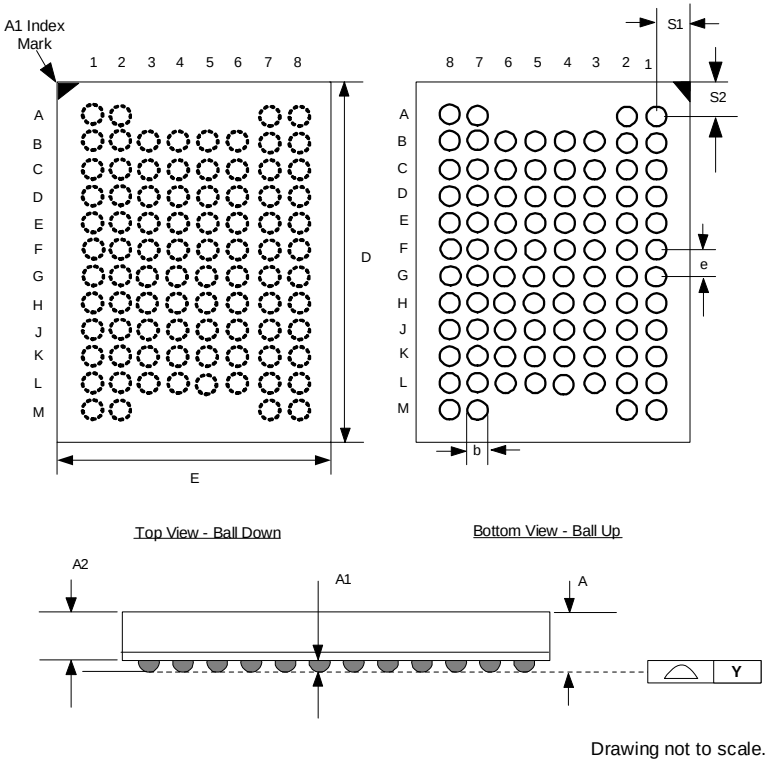


Table 3. 2 Mb, 64 Mb, and 128 Mb VF BGA Package Specifications

Dimension	Symbol	Millimeters			Inches		
		Min	Nom	Max	Min	Nom	Max
Package Height	A	-	-	1.000	-	-	0.0394
Ball Height	A_1	0.150	-	-	0.0059	-	-
Package Body Thickness	A_2	-	0.665	-	-	0.0262	-
Ball (Lead) Width	b	0.325	0.375	0.425	0.0128	0.0148	0.0167
Package Body Width (32 Mb, 64 Mb)	D	7.600	7.700	7.800	0.2992	0.3031	0.3071
Package Body Width (128 Mb)	D	10.900	11.000	11.100	0.4291	0.4331	0.4370
Package Body Length (32 Mb, 64 Mb, 128 Mb)	E	8.900	9.000	9.100	0.3504	0.3543	0.3583
Pitch	[e]	-	0.750	-	-	0.0295	-
Ball (Lead) Count	N	-	56	-	-	56	-
Seating Plane Coplanarity	Y	-	-	0.100	-	-	0.0039
Corner to Ball A1 Distance Along D (32 Mb, 64 Mb)	S_1	1.125	1.225	1.325	0.0443	0.0482	0.0522
Corner to Ball A1 Distance Along D (128 Mb)	S_1	2.775	2.2875	2.975	0.1093	0.1132	0.1171
Corner to Ball A1 Distance Along E (32 Mb, 64 Mb,128 Mb)	S_2	2.150	2.250	2.350	0.0846	0.0886	0.0925

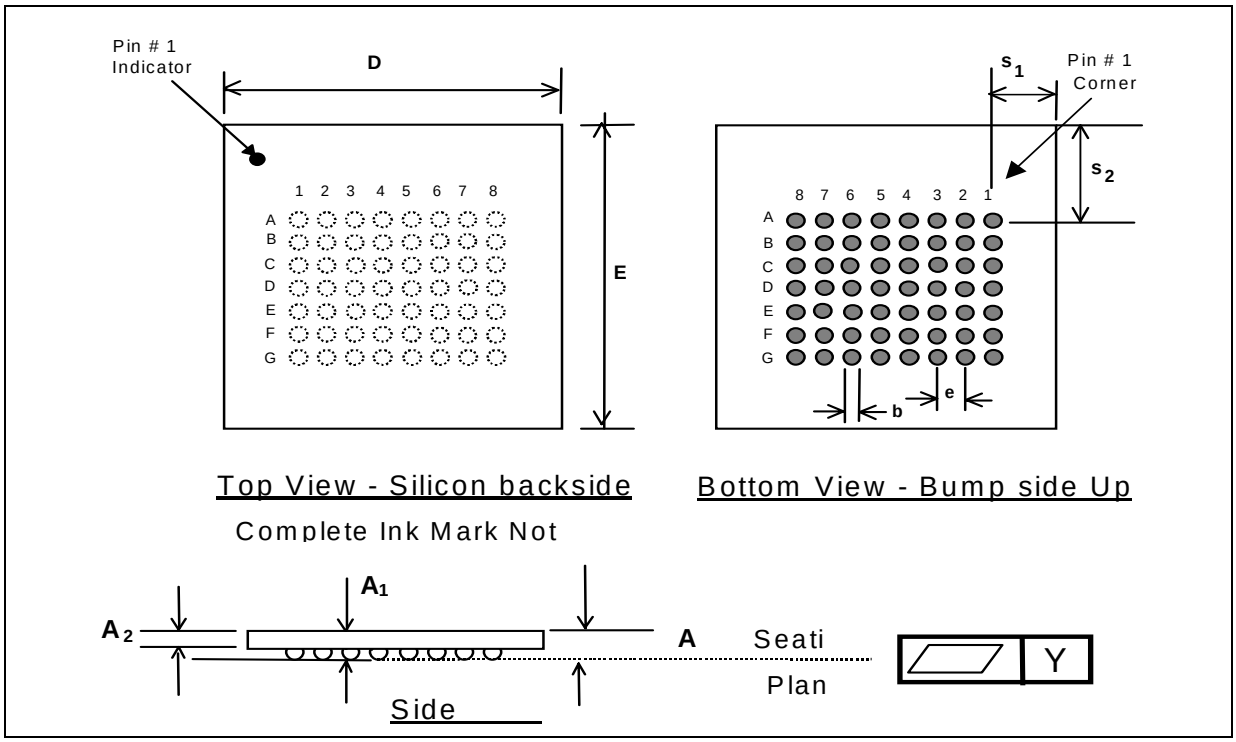
Figure 2. 32Mb, 64Mb and 128Mb QUAD+ Package Drawing



		Millimeters				Inches		
Dimensions	**Symbol**	**Min**	**Nom**	**Max**	**Notes**	**Min**	**Nom**	**Max**
Package Height	A			1.200				0.0472
Ball Height	A1	0.200				0.0079		
Package Body Thickness	A2		0.860				0.0339	
Ball (Lead) Width	b	0.325	0.375	0.425		0.0128	0.0148	0.0167
Package Body Length	D	9.900	10.000	10.100		0.3898	0.3937	0.3976
Package Body Width	E	7.900	8.000	8.100		0.3110	0.3150	0.3189
Pitch	e		0.800				0.0315	
Ball (Lead) Count	N		88				88	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball A1 Distance Along E	S1	1.100	1.200	1.300		0.0433	0.0472	0.0512
Corner to Ball A1 Distance Along D	S2	0.500	0.600	0.700		0.0197	0.0236	0.0276

3.2 W30 Flash Memory Device – 180 nm Lithography

Figure 3. 64Mb µBGA* CSP Package Drawing and Dimensions



	Symbol	Millimeters				Inches		
		Min	Nom	Max	Notes	Min	Nom	Max
Package Height	A	0.850		1.000		0.0335		0.0394
Ball Height	A1	0.150				0.0059		
Package Body Thickness	A2	0.612	0.712	0.812		0.0241	0.0280	0.0320
Ball (Lead) Width	b	0.300	0.350	0.400		0.0118	0.0138	0.0157
Package Body Width	D	7.600	7.700	7.800		0.2992	0.3031	0.3071
Package Body Length	E	8.900	9.000	9.100		0.3503	0.3543	0.3583
Pitch	[e]		0.750				0.0295	
Ball (Lead) Count	N		56				56	
Seating Plane Coplanarity	Y			0.100				0.0039
Corner to Ball A1 Distance Along D	S1	1.125	1.225	1.325		0.0443	0.0482	0.0522
Corner to Ball A1 Distance Along E	S2	2.150	2.250	2.350		0.0846	0.0886	0.0925

Figure 4. 32Mb VF BGA Package Drawing

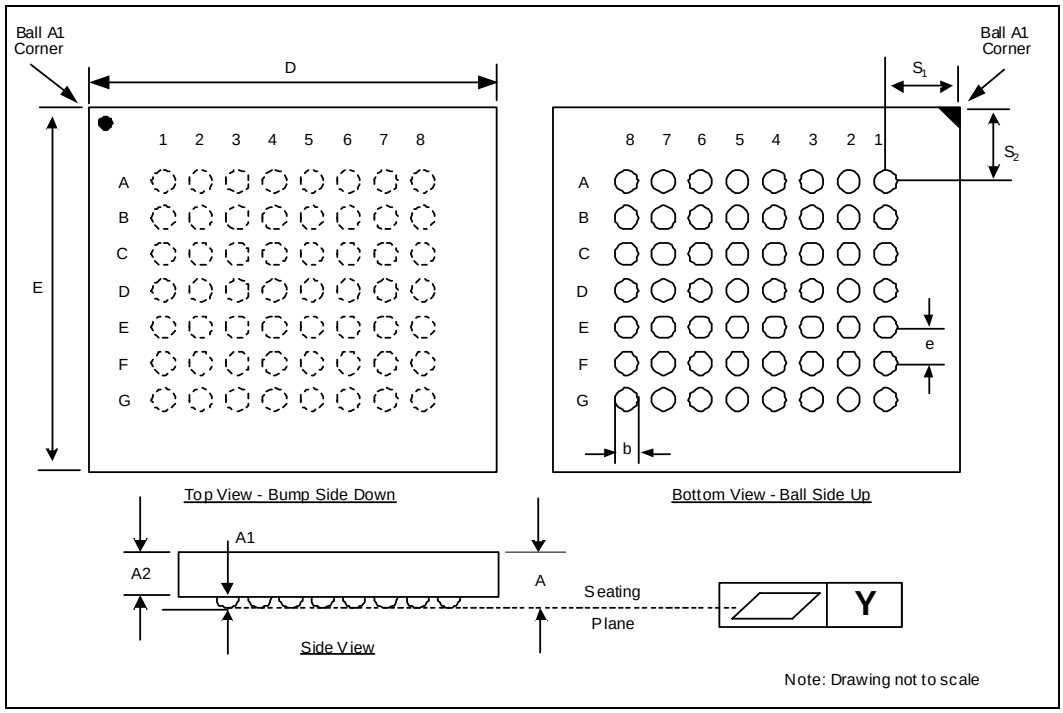


Figure 5. 128Mb VF BGA Package Drawing

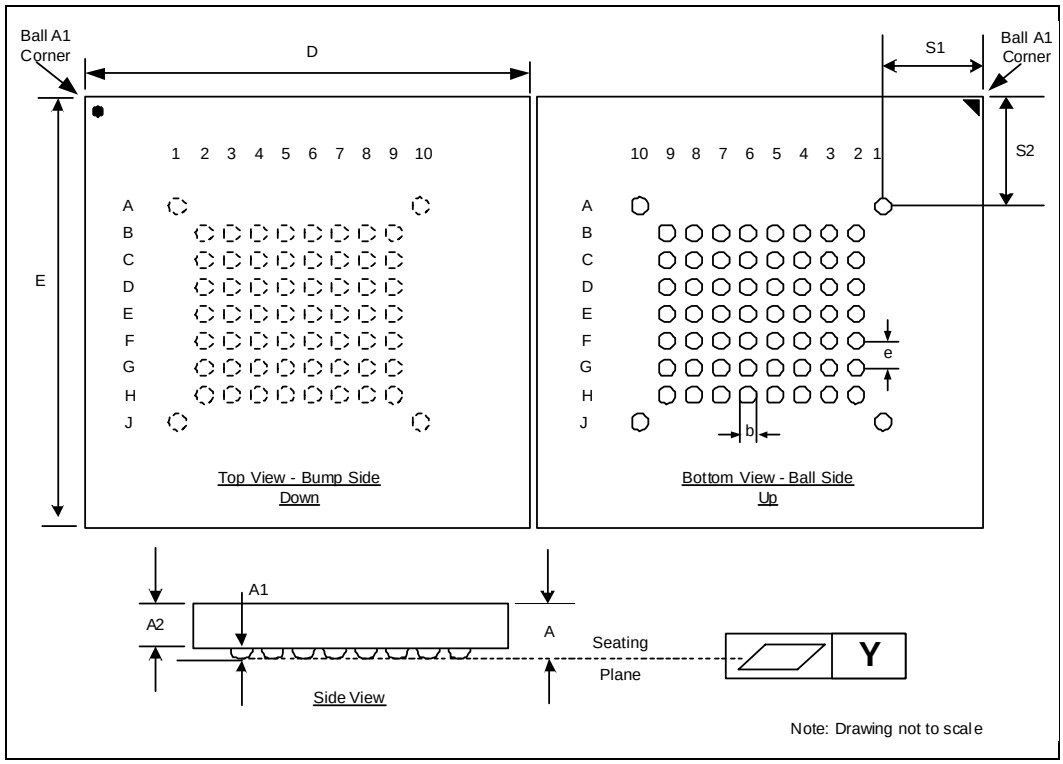


Table 4. 32Mb and 128Mb VF BGA Package Dimensions

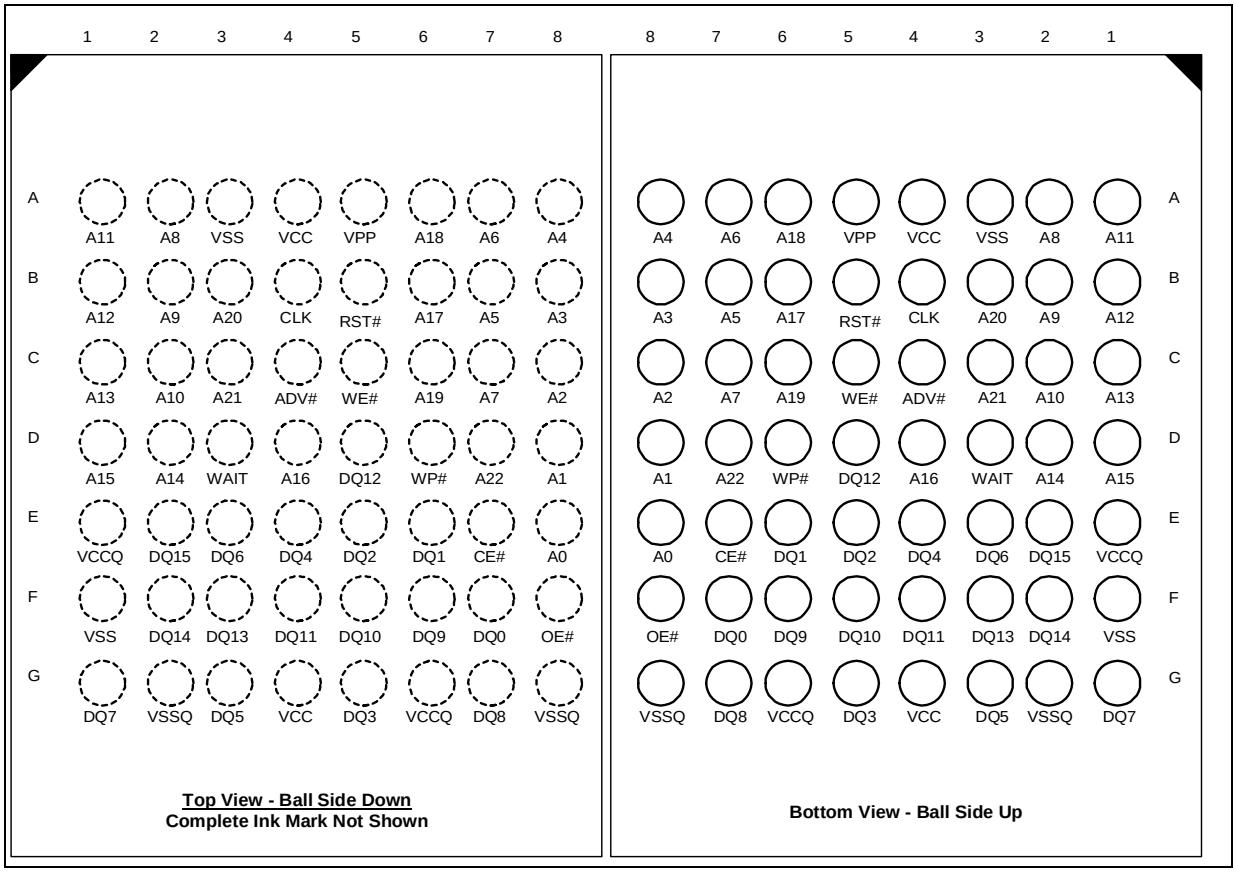
Dimension	Symbol	Millimeters			Inches		
		Min	Nom	Max	Min	Nom	Max
Package Height	A	0.850	-	1.000	0.0335	-	0.0394
Ball Height	A_1	0.150	-	-	0.0059	-	-
Package Body Thickness	A_2	0.615	0.665	0.715	0.0242	0.0262	0.0281
Ball (Lead) Width	b	0.325	0.375	0.425	0.0128	0.0148	0.0167
Package Body Width 32Mb	D	7.600	7.700	7.800	0.2992	0.3031	0.3071
Package Body Length32Mb	E	8.900	9.000	9.100	0.3503	0.3543	0.3583
Package Body Width 128Mb	D	12.400	12.500	12.600	0.4882	0.4921	0.4961
Package Body Length 128Mb	E	11.900	12.000	12.100	0.4685	0.4724	0.4764
Pitch	[e]	-	0.750	-	-	0.0295	-
Ball (Lead) Count 32Mb	N	-	56	-	-	56	-
Ball (Lead) Count 128Mb	N	-	60	-	-	60	-
Seating Plane Coplanarity	Y	-	-	0.100	-	-	0.0039
Corner to Ball A1 Distance Along D 32Mb	S_1	1.125	1.225	1.325	0.0443	0.0482	0.0522
Corner to Ball A1 Distance Along E 32Mb	S_2	2.150	2.250	2.350	0.0846	0.0886	0.0925
Corner to Ball A1 Distance Along D 128Mb	S_1	2.775	2.875	2.975	0.1093	0.1132	0.1171
Corner to Ball A1 Distance Along E 128Mb	S_2	2.900	3.000	3.1000	0.1142	0.1181	0.1220

4.0 Ballout and Signal Descriptions

4.1 Signal Ballout

The W30 flash memory device is available in the 56-ball VF BGA and µBGA Chip Scale Package with 0.75 mm ball pitch, or the QUAD+ SCSP package. Figure 6 shows the VF BGA and µBGA package ballout. Figure 7 shows the QUAD+ package ballout.

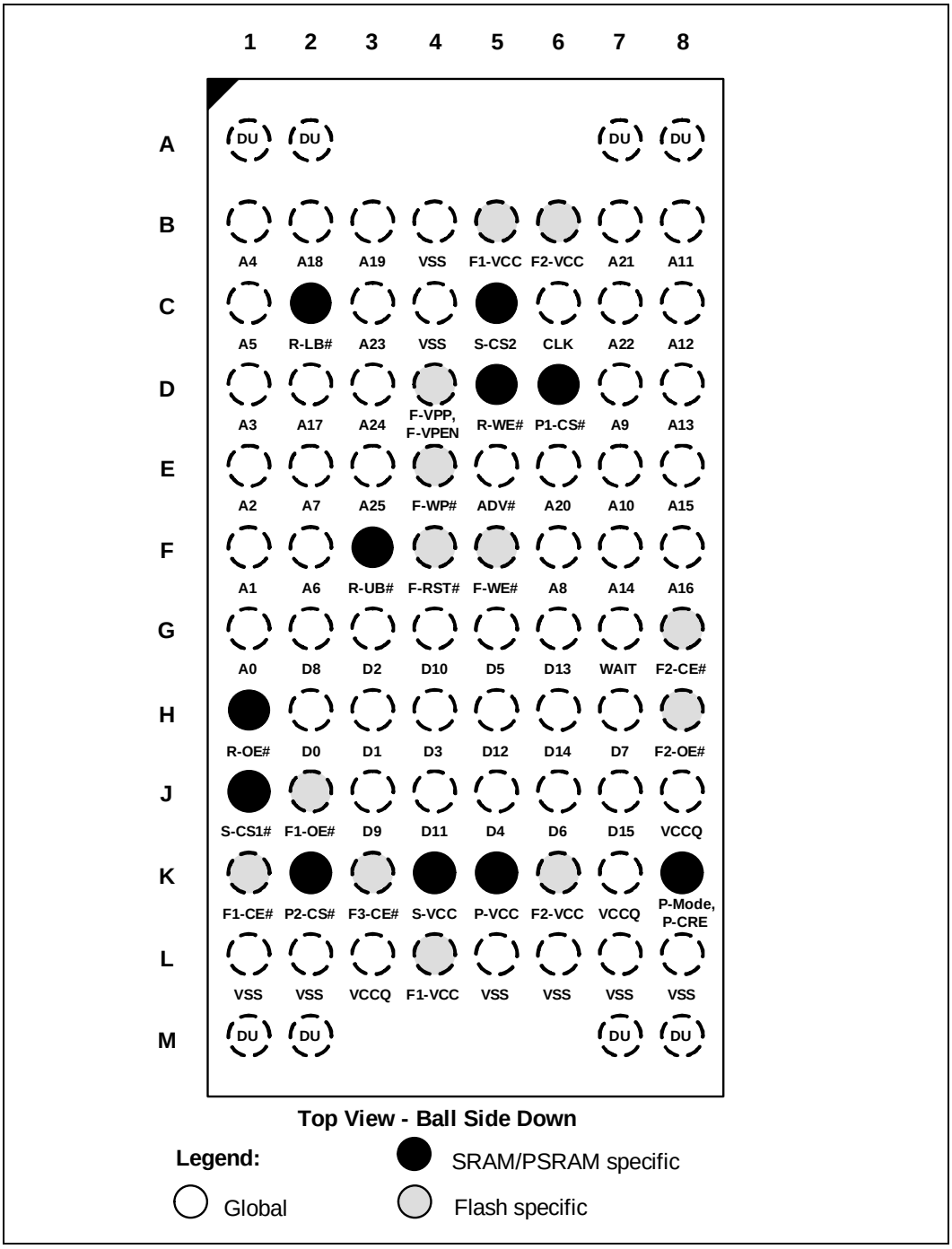
Figure 6. 56-Ball VF BGA/ µBGA Ballout



Notes:

1. On lower density flash memory devices, the upper address balls can be treated as NC. (that is, on 32-Mbit density, A22 and A21 are NC).
2. See Appendix C, "Ordering Information" on page 103 for mechanical specifications for the package.

Figure 7. 88-Ball (80 Active Balls) QUAD+ Ballout



Notes:

1. On lower density flash memory devices, the upper address balls can be treated as NC (that is, on 64-Mb density, A[25:23]are NC)
2. See Appendix C, "Ordering Information" on page 103 for mechanical specifications for the package.

4.2 Signal Descriptions

- Table 5 describes the signals for the 56-ball VF BGA and µBGA Chip Scale Package.
- Table 6 describes the signals for the QUAD+ package ballout.

Table 5. Signal Descriptions - µBGA Package & VF BGA Package (Sheet 1 of 2)

Symbol	Type	Name and Function
A[22:0]	Input	**ADDRESS INPUTS:** For memory addresses. 32 Mbit: A[20:0]; 64 Mbit: A[21:0]; 128 Mbit: A[22:0]
D[15:0]	Input/ Output	**DATA INPUTS/OUTPUTS:** • Inputs data and commands during write cycles. • Outputs data during reads. Data pins are High-Z when the flash device or its outputs are deselected. Data is internally latched during writes.
ADV#	Input	**ADDRESS VALID:** ADV# indicates valid address presence on address inputs. During synchronous read operations, all addresses are latched on the rising edge of ADV#, or the next valid CLK edge with ADV# low, whichever occurs first.
CE#	Input	**CHIP ENABLE:** • Asserting CE# activates internal control logic, I/O buffers, decoders, and sense amps. • De-asserting CE# deselects the flash device, places it in standby mode, and tri-states all outputs.
CLK	Input	**CLOCK:** CLK synchronizes the flash device to the system bus frequency during synchronous reads and increments an internal address generator. During synchronous read operations, addresses are latched on ADV#'s rising edge or CLK's rising (or falling) edge, whichever occurs first.
OE#	Input	**OUTPUT ENABLE:** • When asserted, OE# enables the flash device output data buffers during a read cycle. • When OE# is deasserted, data outputs are placed in a high-impedance state.
RST#	Input	**RESET:** When low, RST# resets internal automation and inhibits write operations. This reset provides data protection during power transitions. De-asserting RST# enables normal operation and places the flash device in asynchronous read-array mode.
WAIT	Output	**WAIT:** The WAIT signal indicates valid data during synchronous read modes. It can be configured to be asserted-high or asserted-low, based on bit 10 of the Read Configuration Register. WAIT is tri-stated if CE# is deasserted. WAIT is not gated by OE#.
WE#	Input	**WRITE ENABLE:** WE# controls writes to the CUI and array. Addresses and data are latched on the rising edge of WE#.
WP#	Input	**WRITE PROTECT:** Disables/enables the lock-down function. When WP# is asserted, the lock-down mechanism is enabled and blocks marked lock-down cannot be unlocked through software. See Section 13.1, "Block Lock Operations" on page 73 for details on block locking.
VPP	Power/ Input	**ERASE AND PROGRAM POWER:** A valid voltage on this pin allows erasing or programming. Flash memory contents cannot be altered when $V_{PP} \le V_{PPLK}$. Do not attempt block erase and program operations at invalid V_{PP} voltages. Set $V_{PP} = V_{CC}$ for in-system program and erase operations. To accommodate resistor or diode drops from the system supply, the V_{IH} level of V_{PP} can be as low as V_{PPL} min. V_{PP} must remain above V_{PPL} min to perform in-system flash device modification. VPP can be 0 V during read operations. V_{PPH} can be applied to main blocks for 1000 cycles maximum and to parameter blocks for 2500 cycles. VPP can be connected to 12 V for a cumulative total not to exceed 80 hours. Extended use of this pin at 12 V might reduce block cycling capability.
VCC	Power	**FLASH DEVICE POWER SUPPLY:** Writes are inhibited at $V_{CC} \le V_{LKO}$. Do not attempt flash device operations at invalid V_{CC} voltages.
VCCQ	Power	**OUTPUT POWER SUPPLY:** Enables all outputs to be driven at V_{CCQ}.
VSS	Power	**GROUND:** Pins for all internal flash device circuitry must be connected to system ground.

Table 5. Signal Descriptions - µBGA Package & VF BGA Package (Sheet 2 of 2)

Symbol	Type	Name and Function
VSSQ	Power	**OUTPUT GROUND**: Provides ground to all outputs which are driven by VCCQ. This signal can be tied directly to VSS.
DU	—	**DO NOT USE:** Do not use this pin. Do not connect this pin to any power supplies, signals, or other pins; this pin must be floated.
NC	—	**NO CONNECT:** No internal connection; can be driven or floated.

Table 6. Signal Descriptions - QUAD+ Package (Sheet 1 of 3)

Symbol	Type	Description
A[MAX:MIN]	Input	**ADDRESS INPUTS:** Inputs for all die addresses during read and write operations. • 128-Mbit Die : AMAX = A22 • 64-Mbit Die : AMAX = A21 • 32-Mbit Die : AMAX = A20 A0 is the lowest-order 16-bit wide address. A[25:24] denote high-order addresses reserved for future flash device densities.
DQ[15:0]	Input/ Output	**DATA INPUTS/OUTPUTS:** • Inputs data and commands during write cycles. • Outputs data during read cycles. Data signals float when the flash device or its outputs are deselected. Data are internally latched during writes on the flash device.
F[3:1]-CE#	Input	**FLASH CHIP ENABLE:** Low-true input. F[3:1]-CE# low selects the associated flash memory die. • When asserted, flash memory internal control logic, input buffers, decoders, and sense amplifiers are active. • When deasserted, the associated flash die is deselected, power is reduced to standby levels, and data and WAIT outputs are placed in high-Z state. • F1-CE# selects or deselects flash die #1. • F2-CE# selects or deselects flash die #2 and is RFU on combinations with only one flash die. • F3-CE# selects or deselects flash die #3 and is RFU on stacked combinations with only one or two flash dies.
S-CS1# S-CS2	Input	**SRAM CHIP SELECT:** Low-true / High-true input (S-CS1# / S-CS2 respectively). • When either/both SRAM Chip Select signals are asserted, SRAM internal control logic, input buffers, decoders, and sense amplifiers are active. • When either/both SRAM Chip Select signals are deasserted, the SRAM is deselected and its power is reduced to standby levels. S-CS1# and S-CS2 are available on stacked combinations with SRAM die and are RFU on stacked combinations without SRAM die.
P[2:1]-CS#	Input	**PSRAM CHIP SELECT:** Low-true input. • When asserted, PSRAM internal control logic, input buffers, decoders, and sense amplifiers are active. • When deasserted, the PSRAM is deselected and its power is reduced to standby levels. • P1-CS# selects PSRAM die #1 and is available only on stacked combinations with PSRAM die. This ball is an RFU on stacked combinations without PSRAM. • P2-CS# selects PSRAM die #2 and is available only on stacked combinations with two PSRAM dies. This ball is an RFU on stacked combinations without PSRAM or with a single PSRAM.

Table 6. Signal Descriptions - QUAD+ Package (Sheet 2 of 3)

Symbol	Type	Description
F[2:1]-OE#	Input	**FLASH OUTPUT ENABLE:** Low-true input. • Fx-OE# low enables the output buffers on the selected flash memory device. • F[2:1]-OE# high disables the output buffers on the selected flash memory device, placing them in High-Z. • F1-OE# controls the outputs of flash die #1. • F2-OE# controls the outputs of flash die #2 and flash die #3. F2-OE# is available on stacked combinations with two or three flash die, and is RFU on stacked combinations with only one flash die.
R-OE#	Input	**RAM OUTPUT ENABLE:** Low-true input. • R-OE# low enables the output buffers on the selected RAM. • R-OE# high disables the RAM output buffers, and places the selected RAM outputs in High-Z. R-OE# is available on stacked combinations with PSRAM or SRAM die, and is an RFU on flash-only stacked combinations.
F-WE#	Input	**FLASH WRITE ENABLE:** Low-true input. F-WE# controls writes to the selected flash die. Address and data are latched on the rising edge of F-WE#.
R-WE#	Input	**RAM WRITE ENABLE:** Low-true input. R-WE# controls writes to the selected RAM die. R-WE# is available on stacked combinations with PSRAM or SRAM die, and is an RFU on flash-only stacked combinations.
CLK	Input	**CLOCK:** Synchronizes the flash die with the system bus clock in synchronous read mode and increments the internal address generator. • During synchronous read operations, addresses are latched on the rising edge of ADV#, or on the next valid CLK edge with ADV# low, whichever occurs first. • During asynchronous mode read operations, addresses are latched on the rising edge ADV#, or are continuously flow-through when ADV# is kept asserted.
WAIT	Output	**WAIT:** Output signal. Indicates invalid data during synchronous array or non-array flash memory reads. Read Configuration Register bit 10 (RCR[10]) determines WAIT-asserted polarity (high or low). WAIT is High-Z if F-CE# is deasserted; WAIT is not gated by F-OE#. • In synchronous array or non-array flash memory read modes, WAIT indicates invalid data when asserted and valid data when deasserted. • In asynchronous flash memory page read, and all flash memory write modes, WAIT is asserted.
F-WP#	Input	**FLASH WRITE PROTECT:** Low-true input. F-WP# enables/disables the lock-down protection mechanism of the selected flash die. • F-WP# low enables the lock-down mechanism where locked down blocks cannot be unlocked using software commands. • F-WP# high disables the lock-down mechanism, allowing locked down blocks to be unlocked using software commands.
ADV#	Input	**ADDRESS VALID:** Low-true input. • During synchronous flash memory read operations, addresses are latched on the rising edge of ADV#, or on the next valid CLK edge with ADV# low, whichever occurs first. • During asynchronous flash memory read operations, addresses are latched on the rising edge of ADV#, or are continuously flow-through when ADV# is kept asserted.

Table 6. Signal Descriptions - QUAD+ Package (Sheet 3 of 3)

Symbol	Type	Description
R-UB# R-LB#	Input	**RAM UPPER / LOWER BYTE ENABLES:** Low-true input. During RAM read and write cycles: • R-UB# low enables the RAM high order bytes on D[15:8]. • R-LB# low enables the RAM low-order bytes on D[7:0]. R-UB# and R-LB# are available on stacked combinations with PSRAM or SRAM die, and are RFU on flash-only stacked combinations.
F-RST#	Input	**FLASH RESET:** Low-true input. • F-RST# low initializes flash device internal circuitry and disables flash device operations. • F-RST# high enables flash device operation. Exit from reset places the flash device in asynchronous read array mode.
P-Mode, P-CRE	Input	**P-Mode (PSRAM Mode):** Low-true input. P-Mode programs the Configuration Register, and enters/exits the Low Power Mode of the PSRAM die. P-Mode is available on stacked combinations with asynchronous-only PSRAM die. • **P-CRE (PSRAM Configuration Register Enable):** High-true input. • P-CRE is high, write operations load the Refresh Control Register or Bus Control Register. • P-CRE applies only on combinations with synchronous PSRAM die. P-Mode, P-CRE is an RFU on stacked combinations without PSRAM die.
F-VPP, F-VPEN	Power	**FLASH PROGRAM AND ERASE POWER:** Valid F-V_{PP} voltage on this ball enables flash memory device program/erase operations. Flash memory array contents cannot be altered when F-V_{PP}(F-V_{PEN}) ≤ V_{PPLK} (V_{PENLK}). Do not attempt erase / program operations at invalid F-V_{PP} (F-V_{PEN}) voltages. F-VPEN (Erase/Program/Block Lock Enables) is not available for L18/L30 SCSP products.
F[2:1]-VCC	Power	**FLASH LOGIC POWER:** • F1-VCC supplies power to the core logic of flash die #1. • F2-VCC supplies power to the core logic of flash die #2 and flash die #3. Write operations are inhibited when F-V_{CC} ≤ V_{LKO}. Do not attempt flash device operations at invalid F-V_{CC} voltages. F2-VCC is available on stacked combinations with two or three flash dies, and is an RFU on stacked combinations with only one flash die.
S-VCC	Power	**SRAM POWER SUPPLY:** Supplies power for SRAM operations. S-VCC is available on stacked combinations with SRAM die, and is RFU on stacked combinations without SRAM die.
P-VCC	Power	**PSRAM POWER SUPPLY:** Supplies power for PSRAM operations. P-VCC is available on stacked combinations with PSRAM die, and is RFU on stacked combinations without PSRAM die.
VCCQ	Power	**FLASH DEVICE I/O POWER:** Supply power for the flash device input and output buffers.
VSS	Power	**FLASH DEVICE GROUND:** Connect to system ground. Do not float any VSS connection.
RFU	—	**RESERVED for FUTURE USE:** Reserved for future flash device functionality/ enhancements. Contact Intel regarding the use of balls designated RFU.
DU	—	**DO NOT USE:** Do not connect to any other signal, or power supply; must be left floating.

5.0 Maximum Ratings and Operating Conditions

5.1 Absolute Maximum Ratings

Warning: Stressing the flash device beyond the Absolute Maximum Ratings in Table 7 might cause permanent damage. These are stress ratings only.

Notice: This datasheet contains information on products in the design phase of development. The information here is subject to change without notice. Do not finalize a design with this information.

Table 7. Absolute Maximum Ratings

Parameter	Maximum Rating	Note
Temperature under Bias	–40 °C to +85 °C	
Storage Temperature	–65 °C to +125 °C	
Voltage on Any Pin (except V_{CC}, V_{CCQ}, V_{PP})	–0.5 V to +3.8 V	
V_{PP} Voltage	–0.2 V to +14 V	1,2,3
V_{CC} Voltage	–0.2 V to +2.45 V	1
V_{CCQ} Voltage	–0.2 V to +3.8 V	1
Output Short Circuit Current	100 mA	4

Notes:

1. All specified voltages are relative to V_{SS}. Minimum DC voltage is –0.5 V on input/output pins and –0.2 V on V_{CC} and V_{PP} pins. During transitions, this level might undershoot to –2.0 V for periods < 20 ns. Maximum DC voltage on input/output pins is V_{CC} +0.5 V which, during transitions, might overshoot to V_{CC} +2.0 V for periods < 20 ns.
2. Maximum DC voltage on V_{PP} might overshoot to +14.0 V for periods < 20 ns.
3. V_{PP} program voltage is normally V_{PPL}. V_{PP} can be 12 V ± 0.6 V for 1000 cycles on the main blocks and 2500 cycles on the parameter blocks during program/erase.
4. Output shorted for no more than one second. No more than one output shorted at a time.

5.2 Operating Conditions

Do not operate the W30 flash memory device beyond the Operating Conditions in Table 8. Extended exposure beyond these Operating Conditions might affect flash device reliability.

Table 8. Extended Temperature Operation

Symbol	Parameter[1]		Min	Nom	Max	Unit	Notes
T_A	Operating Temperature		–40	25	85	°C	-
V_{CC}	V_{CC} Supply Voltage		1.7	1.8	1.90	V	3
V_{CCQ}	I/O Supply Voltage		2.2	3.0	3.3		3
V_{PPL}	V_{PP} Voltage Supply (Logic Level)		0.90	1.80	1.95		2
V_{PPH}	Factory Programming V_{PP}		11.4	12.0	12.6		2
t_{PPH}	Maximum V_{PP} Hours	V_{PP} = 12 V	-	-	80	Hours	2
Block Erase Cycles	Main and Parameter Blocks	$V_{PP} \leq V_{CC}$	100,000	-	-	Cycles	2
	Main Blocks	V_{PP} = 12 V	-	-	1000		2
	Parameter Blocks	V_{PP} = 12 V	-	-	2500		2

Notes:

1. See Section 6.1, “DC Current Characteristics” on page 27 and Section 6.2, “DC Voltage Characteristics” on page 28 for specific voltage-range specifications.
2. VPP is normally V_{PPL}. VPP can be connected to 11.4 V–12.6 V for 1000 cycles on main blocks for extended temperatures and 2500 cycles on parameter blocks at extended temperature.
3. Contact your Intel field representative for V_{CC}/V_{CCQ} operations down to 1.65 V.
4. See the tables in Section 6.0, “Electrical Specifications” on page 27 and in Section 7.0, “AC Characteristics” on page 29 for operating characteristics

6.0 Electrical Specifications

6.1 DC Current Characteristics

Table 9. DC Current Characteristics (Sheet 1 of 2)

Sym	Parameter [1]		Note	V_{CCQ}= 3.0 V				Unit	Test Conditions	
				32/64 Mbit		128 Mbit				
				Typ	Max	Typ	Max			
I_{LI}	Input Load		9	-	±2	-	±2	µA	$V_{CC} = V_{CC}$Max $V_{CCQ} = V_{CCQ}$Max $V_{IN} = V_{CCQ}$ or GND	
I_{LO}	Output Leakage	DQ[15:0]		-	±10	-	±10	µA	$V_{CC} = V_{CC}$Max $V_{CCQ} = V_{CCQ}$Max $V_{IN} = V_{CCQ}$ or GND	
180 nm I_{CCS}	V_{CC} Standby		10	6	21	6	30	µA	$V_{CC} = V_{CC}$Max $V_{CCQ} = V_{CCQ}$Max CE# = V_{CCQ} RST# =V_{CCQ}	
130 nm I_{CCS}				8	50	8	70			
180 nm I_{CCAPS}	APS		11	6	21	6	30	µA	$V_{CC} = V_{CC}$Max $V_{CCQ} = V_{CCQ}$Max CE# = V_{SSQ} RST# =V_{CCQ} All other inputs =V_{CCQ} or V_{SSQ}	
130 nm I_{CCAPS}				8	50	8	70			
I_{CCR}	Average V_{CC} Read	Asynchronous Page Mode f=13 MHz	2	4	7	4	10	mA	4 Word Read	$V_{CC} = V_{CC}$Max CE# = V_{IL} OE# = V_{IH} Inputs = V_{IH} or V_{IL}
		Synchronous CLK = 40 MHz	2	7	15	7	15	mA	Burst length = 4	
				9	16	9	16	mA	Burst length = 8	
				11	19	11	19	mA	Burst length =16	
				12	22	12	22	mA	Burst length = Continuous	
I_{CCW}	V_{CC} Program		3,4,5	18	40	18	40	mA	$V_{PP} = V_{PPL,}$ Program in Progress	
				8	15	8	15	mA	$V_{PP} = V_{PPH,}$ Program in Progress	
I_{CCE}	V_{CC} Block Erase		3,4,5	18	40	18	40	mA	$V_{PP} = V_{PPL,}$ Block Erase in Progress	
				8	15	8	15	mA	$V_{PP} = V_{PPH,}$ Block Erase in Progress	
I_{CCWS}	V_{CC} Program Suspend		6	6	21	6	30	µA	CE# = $V_{CC,}$ Program Suspended	
I_{CCES}	V_{CC} Erase Suspend		6	6	21	6	30	µA	CE# = $V_{CC,}$ Erase Suspended	
I_{PPS} ($I_{PPWS,}$ I_{PPES})	V_{PP} Standby V_{PP} Program Suspend V_{PP} Erase Suspend		3	0.2	5	0.2	5	µA	$V_{PP} \leq V_{CC}$	
I_{PPR}	V_{PP} Read		-	2	15	2	15	µA	$V_{PP} \leq V_{CC}$	

Table 9. DC Current Characteristics (Sheet 2 of 2)

Sym	Parameter (1)	Note	V_{CCQ}= 3.0 V				Unit	Test Conditions
			32/64 Mbit		128 Mbit			
			Typ	Max	Typ	Max		
I_{PPW}	V_{PP} Program	4	0.05	0.10	0.05	0.10	mA	$V_{PP} = V_{PPL,}$ Program in Progress
			8	22	16	37		$V_{PP} = V_{PPH,}$ Program in Progress
I_{PPE}	V_{PP} Erase	4	0.05	0.10	0.05	0.10	mA	$V_{PP} = V_{PPL,}$ Erase in Progress
			8	22	8	22		$V_{PP} = V_{PPH,}$ Erase in Progress

Notes:
1. All currents are RMS unless noted. Typical values at typical V_{CC}, T_A = +25°C.
2. Automatic Power Savings (APS) reduces I_{CCR} to approximately standby levels in static operation. See I_{CCRQ} specification for details.
3. Sampled, not 100% tested.
4. V_{CC} read + program current is the sum of V_{CC} read and V_{CC} program currents.
5. V_{CC} read + erase current is the sum of V_{CC} read and V_{CC} erase currents.
6. I_{CCES} is specified with the flash device deselected. If the flash device is read while in erase suspend, the current is I_{CCES} plus I_{CCR}.
7. $V_{PP} \leq V_{PPLK}$ inhibits erase and program operations. Do not use V_{PPL} and V_{PPH} outside their valid ranges.
8. V_{IL} can undershoot to –0.4V and V_{IH} can overshoot to V_{CCQ}+0.4V for durations of 20 ns or less.
9. If $V_{IN}>V_{CC}$ the input load current increases to 10 µA max.
10. I_{CCS} is the average current measured over any 5ms time interval 5 µs after a CE# de-assertion.
11. Refer to section Section 8.2, “Automatic Power Savings (APS)” on page 45 for I_{CCAPS} measurement details.

6.2 DC Voltage Characteristics

Table 10. DC Voltage Characteristics

Sym	Parameter (1)	Note	V_{CCQ}= 3.0 V				Unit	Test Conditions
			32/64 Mbit		128 Mbit			
			Min	Max	Min	Max		
V_{IL}	Input Low	8	0	0.4	0	0.4	V	
V_{IH}	Input High	-	V_{CCQ} – 0.4	V_{CCQ}	V_{CCQ} – 0.4	V_{CCQ}	V	
V_{OL}	Output Low	-	-	0.1	-	0.1	V	$V_{CC} = V_{CC}$Min $V_{CCQ} = V_{CCQ}$Min I_{OL} = 100 µA
V_{OH}	Output High	-	V_{CCQ} – 0.1	-	V_{CCQ} – 0.1	-	V	$V_{CC} = V_{CC}$Min $V_{CCQ} = V_{CCQ}$Min I_{OH} = –100 µA
V_{PPLK}	V_{PP} Lock-Out	7	-	0.4	-	0.4	V	
V_{LKO}	V_{CC} Lock	-	1.0	-	1.0	-	V	
V_{ILKOQ}	V_{CCQ} Lock	-	0.9	-	0.9	-	V	

Note: For all numbered note references in this table, refer to the notes in Table 9, “DC Current Characteristics” on page 27.

7.0 AC Characteristics

7.1 Read Operations - 130 nm Lithography

Table 11. Read Operations - 130 nm Lithography (Sheet 1 of 2)

#	Sym	Parameter [1]	32-Mbit 64-Mbit				128-Mbit		Units	Notes
			-70		-85		-70			
			Min	Max	Min	Max	Min	Max		
Asynchronous Specifications										
R1	t_{AVAV}	Read Cycle Time	70	-	85	-	70	-	ns	6
R2	t_{AVQV}	Address to Output Valid	-	70	-	85	-	70	ns	6
R3	t_{ELQV}	CE# Low to Output Valid	-	70	-	85	-	70	ns	6
R4	t_{GLQV}	OE# Low to Output Valid	-	30	-	30	-	30	ns	3
R5	t_{PHQV}	RST# High to Output Valid	-	150	-	150	-	150	ns	-
R6	t_{ELQX}	CE# Low to Output Low-Z	0	-	0	-	0	-	ns	4
R7	t_{GLQX}	OE# Low to Output Low-Z	0	-	0	-	0	-	ns	3,4
R8	t_{EHQZ}	CE# High to Output High-Z	-	20	-	20	-	20	ns	4
R9	t_{GHQZ}	OE# High to Output High-Z	-	14	-	14	-	14	ns	3,4
R10	t_{OH}	CE# (OE#) High to Output Low-Z	0	-	0	-	0	-	ns	3,4
R11	t_{EHEL}	CE# Pulse Width High	20	-	20	-	20	-	ns	5
R12	t_{ELTV}	CE# Low to WAIT Valid	-	20	-	22	-	22	ns	5
R13	t_{EHTZ}	CE# High to WAIT High-Z	-	25	-	25	-	25	ns	4,5
Latching Specifications										
R101	t_{AVVH}	Address Setup to ADV# High	10	-	10	-	12	-	ns	-
R102	t_{ELVH}	CE# Low to ADV# High	10	-	10	-	12	-	ns	-
R103	t_{VLQV}	ADV# Low to Output Valid	-	70		85	-	70	ns	6
R104	t_{VLVH}	ADV# Pulse Width Low	10	-	10	-	12	-	ns	-
R105	t_{VHVL}	ADV# Pulse Width High	10	-	10	-	12	-	ns	-
R106	t_{VHAX}	Address Hold from ADV# High	9	-	9	-	9	-	ns	2
R108	t_{APA}	Page Address Access Time	-	25	-	25	-	25	ns	-
Clock Specifications										
R200	f_{CLK}	CLK Frequency	-	40	-	33	-	40	MHz	-
R201	t_{CLK}	CLK Period	25	-	30	-	25	-	ns	-
R202	$t_{CH/L}$	CLK High or Low Time	9.5	-	9.5	-	9.5	-	ns	-
R203	t_{CHCL}	CLK Fall or Rise Time	-	3	-	5	-	5	ns	-

Table 11. Read Operations - 130 nm Lithography (Sheet 2 of 2)

#	Sym	Parameter [1]	32-Mbit 64-Mbit				128-Mbit		Units	Notes
			-70		-85		-70			
			Min	Max	Min	Max	Min	Max		
Synchronous Specifications										
R301	t_{AVCH}	Address Valid Setup to CLK	9	-	9	-	10	-	ns	-
R302	t_{VLCH}	ADV# Low Setup to CLK	10	-	10	-	10	-	ns	-
R303	t_{ELCH}	CE# Low Setup to CLK	9	-	9	-	9	-	ns	-
R304	t_{CHQV}	CLK to Output Valid	-	20	-	22	-	20	ns	-
R305	t_{CHQX}	Output Hold from CLK	5	-	5	-	5	-	ns	-
R306	t_{CHAX}	Address Hold from CLK	10	-	10	-	10	-	ns	2
R307	t_{CHTV}	CLK to WAIT Valid	-	20	-	22	-	22	ns	-

Notes:

1. See Figure 22, "AC Input/Output Reference Waveform" on page 48 for timing measurements and maximum allowable input slew rate.
2. Address hold in synchronous-burst mode is defined as t_{CHAX} or t_{VHAX}, whichever timing specification is satisfied first.
3. OE# can be delayed by up to $t_{ELQV} - t_{GLQV}$ after the falling edge of CE# without impact to t_{ELQV}.
4. Sampled, not 100% tested.
5. Applies only to subsequent synchronous reads.
6. During the initial access of a synchronous burst read, data from the first word might begin to be driven onto the data bus as early as the first clock edge after t_{AVQV}.

7.2 Read Operations - 180 nm Lithography

Table 12. Read Operations - 180 nm Lithography (Sheet 1 of 2)

#	Sym	Parameter [1]	32-Mbit 64-Mbit				128-Mbit		Units	Notes
			-70		-85		-90			
			Min	Max	Min	Max	Min	Max		
Asynchronous Specifications										
R1	t_{AVAV}	Read Cycle Time	70	-	85	-	90	-	ns	6
R2	t_{AVQV}	Address to Output Valid	-	70	-	85	-	90	ns	6
R3	t_{ELQV}	CE# Low to Output Valid	-	70	-	85	-	90	ns	6
R4	t_{GLQV}	OE# Low to Output Valid	-	30	-	30	-	30	ns	3
R5	t_{PHQV}	RST# High to Output Valid	-	150	-	150	-	150	ns	-
R6	t_{ELQX}	CE# Low to Output Low-Z	0	-	0	-	0	-	ns	4
R7	t_{GLQX}	OE# Low to Output Low-Z	0	-	0	-	0	-	ns	3,4
R8	t_{EHQZ}	CE# High to Output High-Z	-	20	-	20	-	20	ns	4
R9	t_{GHQZ}	OE# High to Output High-Z	-	14	-	14		14	ns	3,4

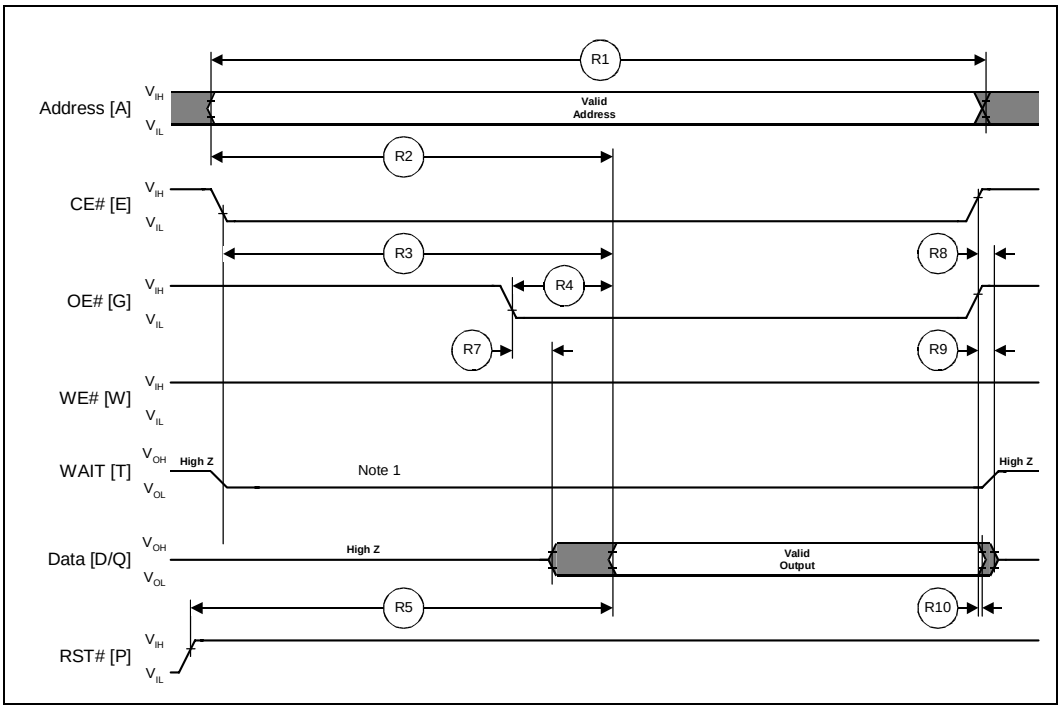
Table 12. Read Operations - 180 nm Lithography (Sheet 2 of 2)

#	Sym	Parameter [1]	32-Mbit 64-Mbit				128-Mbit		Units	Notes
			-70		-85		-90			
			Min	Max	Min	Max	Min	Max		
R10	t_{OH}	CE# (OE#) High to Output Low-Z	0	-	0	-	0	-	ns	3,4
R11	t_{EHEL}	CE# Pulse Width High	20	-	20	-	20	-	ns	5
R12	t_{ELTV}	CE# Low to WAIT Valid	-	20	-	22	-	22	ns	5
R13	t_{EHTZ}	CE# High to WAIT High-Z	-	25	-	25	-	25	ns	4,5
Latching Specifications										
R101	t_{AVVH}	Address Setup to ADV# High	10	-	10	-	12	-	ns	-
R102	t_{ELVH}	CE# Low to ADV# High	10	-	10	-	12	-	ns	-
R103	t_{VLQV}	ADV# Low to Output Valid	-	70	-	85	-	90	ns	6
R104	t_{VLVH}	ADV# Pulse Width Low	10	-	10	-	12	-	ns	-
R105	t_{VHVL}	ADV# Pulse Width High	10	-	10	-	12	-	ns	-
R106	t_{VHAX}	Address Hold from ADV# High	9	-	9	-	9	-	ns	2
R108	t_{APA}	Page Address Access Time	-	25	-	25	-	30	ns	-
Clock Specifications										
R200	f_{CLK}	CLK Frequency	-	40	-	33	-	33	MHz	-
R201	t_{CLK}	CLK Period	25	-	30	-	30	-	ns	-
R202	$t_{CH/L}$	CLK High or Low Time	9.5	-	9.5	-	9.5	-	ns	-
R203	t_{CHCL}	CLK Fall or Rise Time	-	3		5	-	5	ns	-
Synchronous Specifications										
R301	t_{AVCH}	Address Valid Setup to CLK	9	-	9	-	10	-	ns	-
R302	t_{VLCH}	ADV# Low Setup to CLK	10	-	10	-	10	-	ns	-
R303	t_{ELCH}	CE# Low Setup to CLK	9	-	9	-	9	-	ns	-
R304	t_{CHQV}	CLK to Output Valid	-	20	-	22	-	22	ns	-
R305	t_{CHQX}	Output Hold from CLK	5	-	5		5	-	ns	-
R306	t_{CHAX}	Address Hold from CLK	10	-	10	-	10	-	ns	2
R307	t_{CHTV}	CLK to WAIT Valid	-	20	-	22	-	22	ns	-

Notes:

1. See Figure 22, “AC Input/Output Reference Waveform” on page 48 for timing measurements and maximum allowable input slew rate.
2. Address hold in synchronous-burst mode is defined as t_{CHAX} or t_{VHAX}, whichever timing specification is satisfied first.
3. OE# can be delayed by up to $t_{ELQV} - t_{GLQV}$ after the falling edge of CE# without impact to t_{ELQV}.
4. Sampled, not 100% tested.
5. Applies only to subsequent synchronous reads.
6. During the initial access of a synchronous burst read, data from the first word might begin to be driven onto the data bus as early as the first clock edge after t_{AVQV}.

Figure 8. Asynchronous Read Operation Waveform



Notes: .

1. WAIT shown asserted (RCR[10]=0)
2. ADV# assumed to be driven to VIL in this waveform

Figure 9. Latched Asynchronous Read Operation Waveform

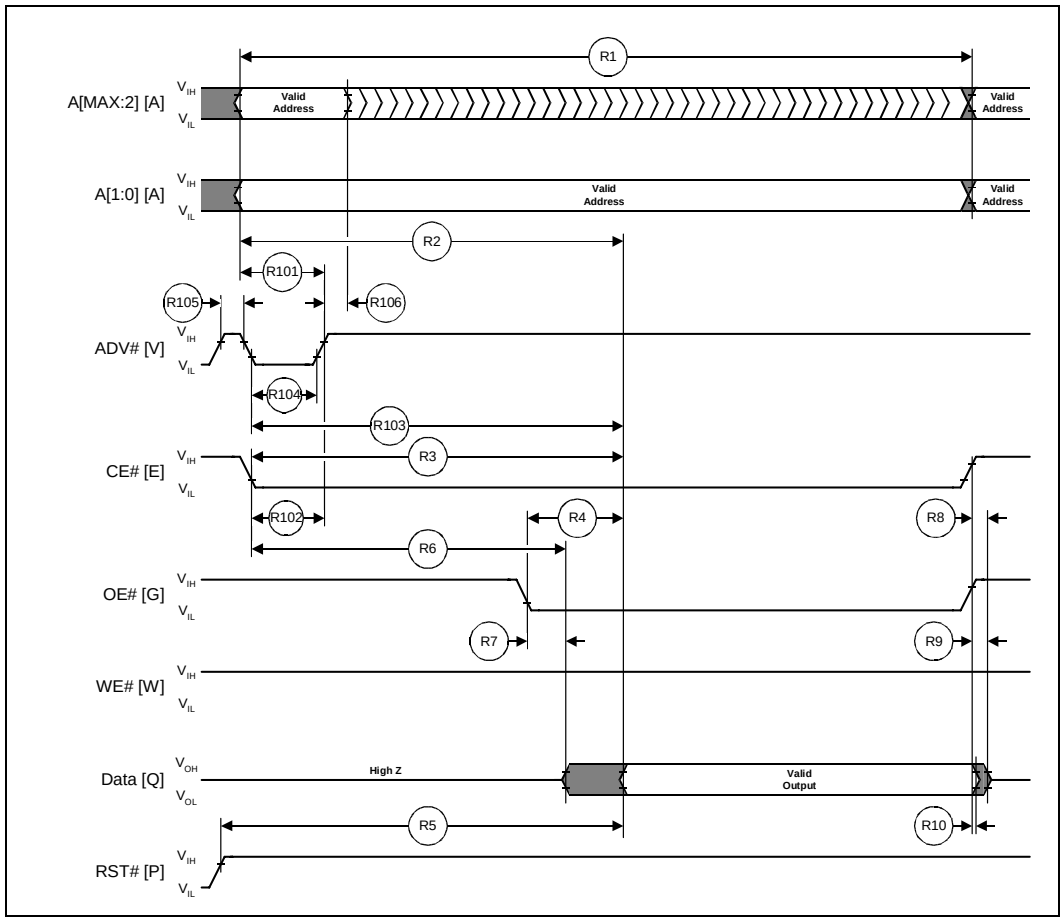
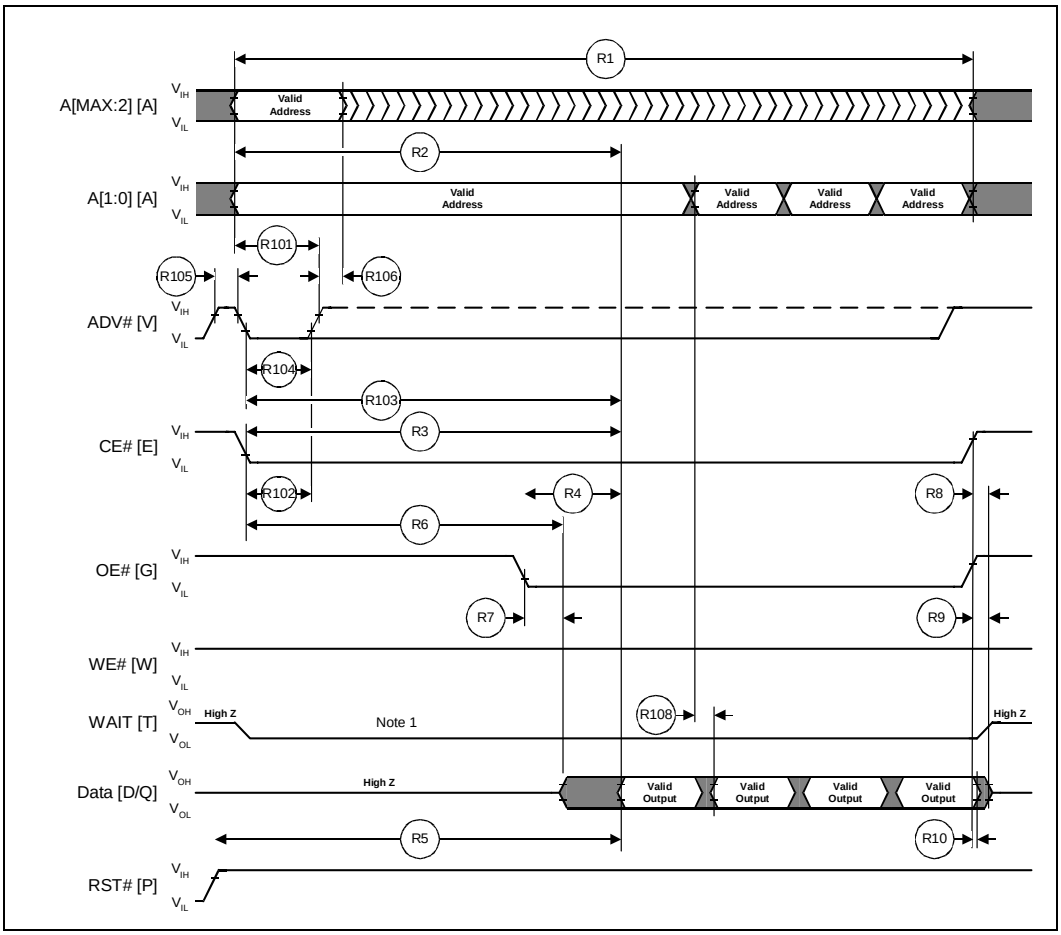


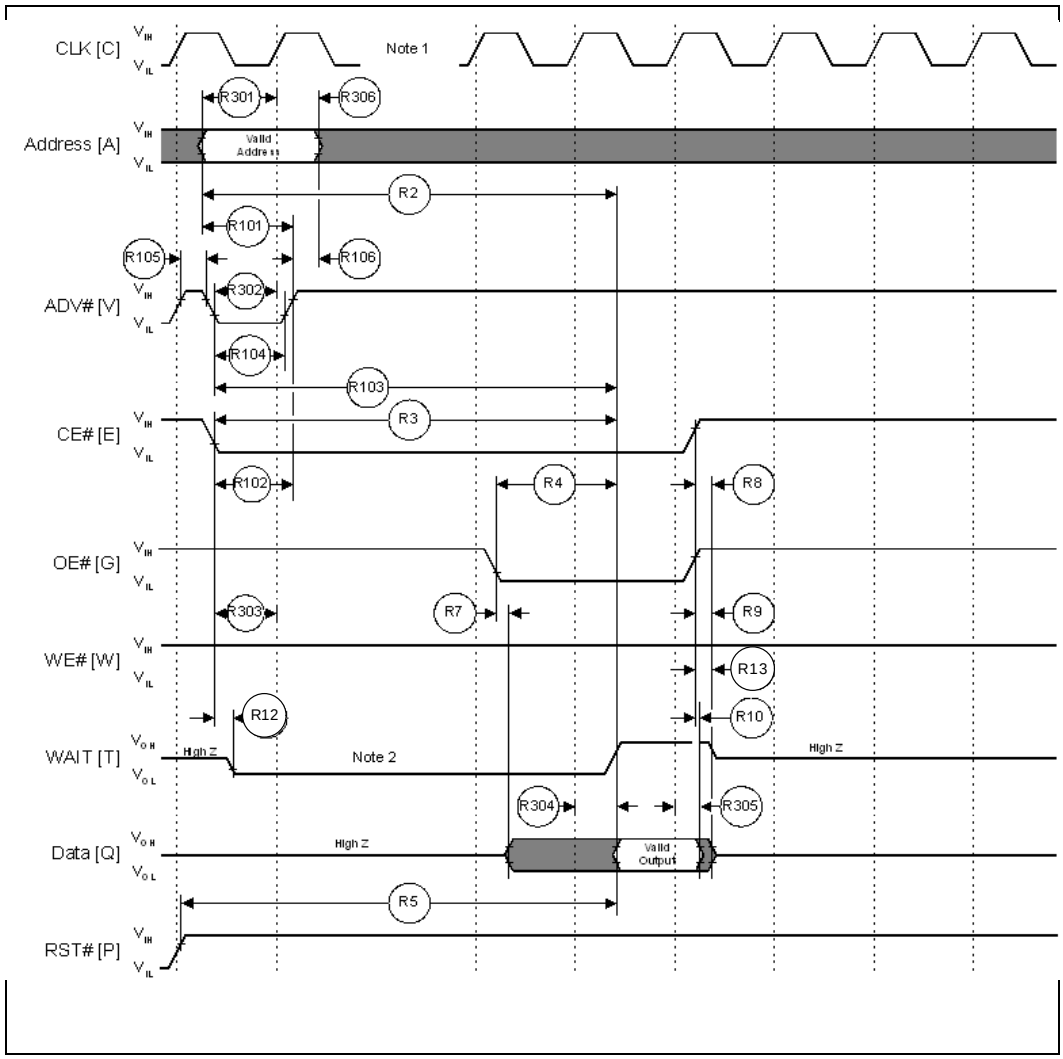
Figure 10. Page-Mode Read Operation Waveform



Note:

1. WAIT shown asserted (RCR[10] = 0).

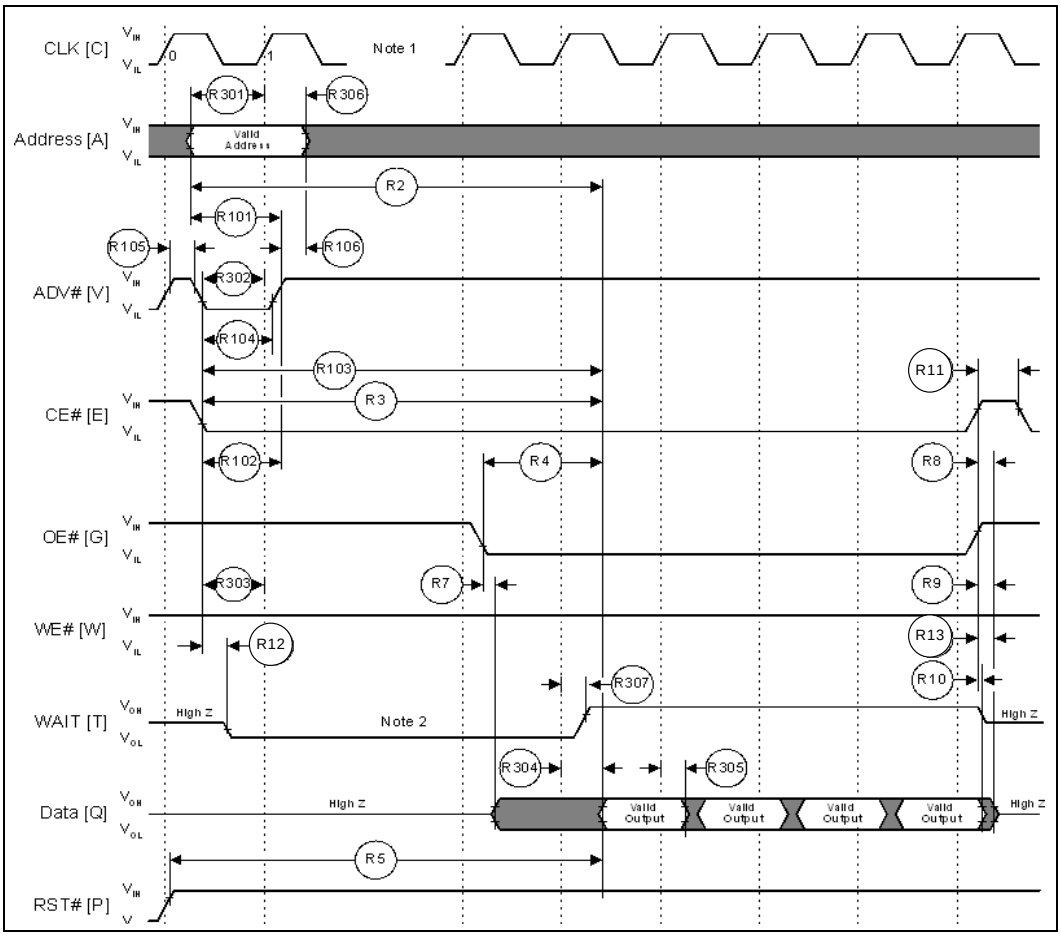
Figure 11. Single Synchronous Read-Array Operation Waveform



Notes:

1. Section 14.2, “First Access Latency Count (RCR[13:11])” on page 83 describes how to insert clock cycles during the initial access.
2. WAIT (shown asserted; RCR[10]=0) can be configured to assert either during, or one data cycle before, valid data.
3. In this waveform, an x-word burst is initiated to the main array and it is terminated by a CE# de-assertion after the first word in the burst. If this access had been done to Status, ID, or Query reads, the asserted (low) WAIT signal would have remained asserted (low) as long as CE# is asserted (low).

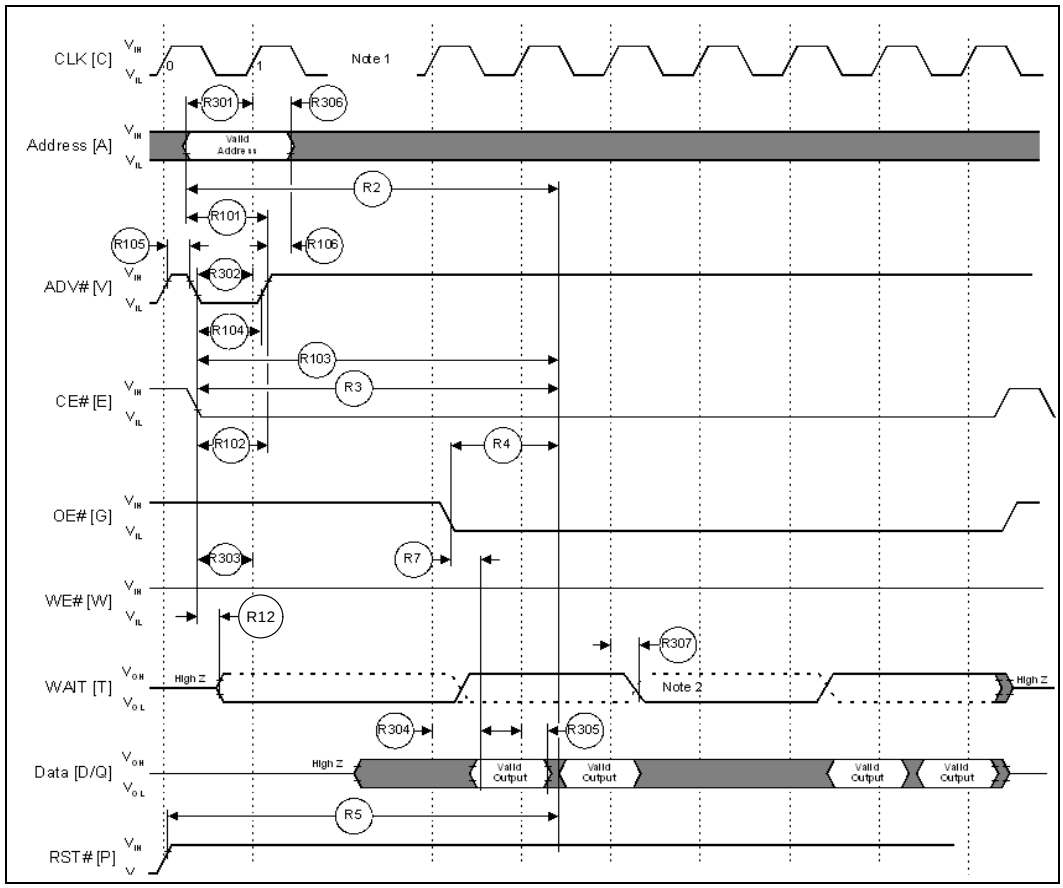
Figure 12. Synchronous 4-Word Burst Read Operation Waveform



Notes:

1. Section 14.2, “First Access Latency Count (RCR[13:11])” on page 83 describes how to insert clock cycles during the initial access.
2. WAIT (shown asserted; RCR[10] = 0) can be configured to assert either during, or one data cycle before, valid data.

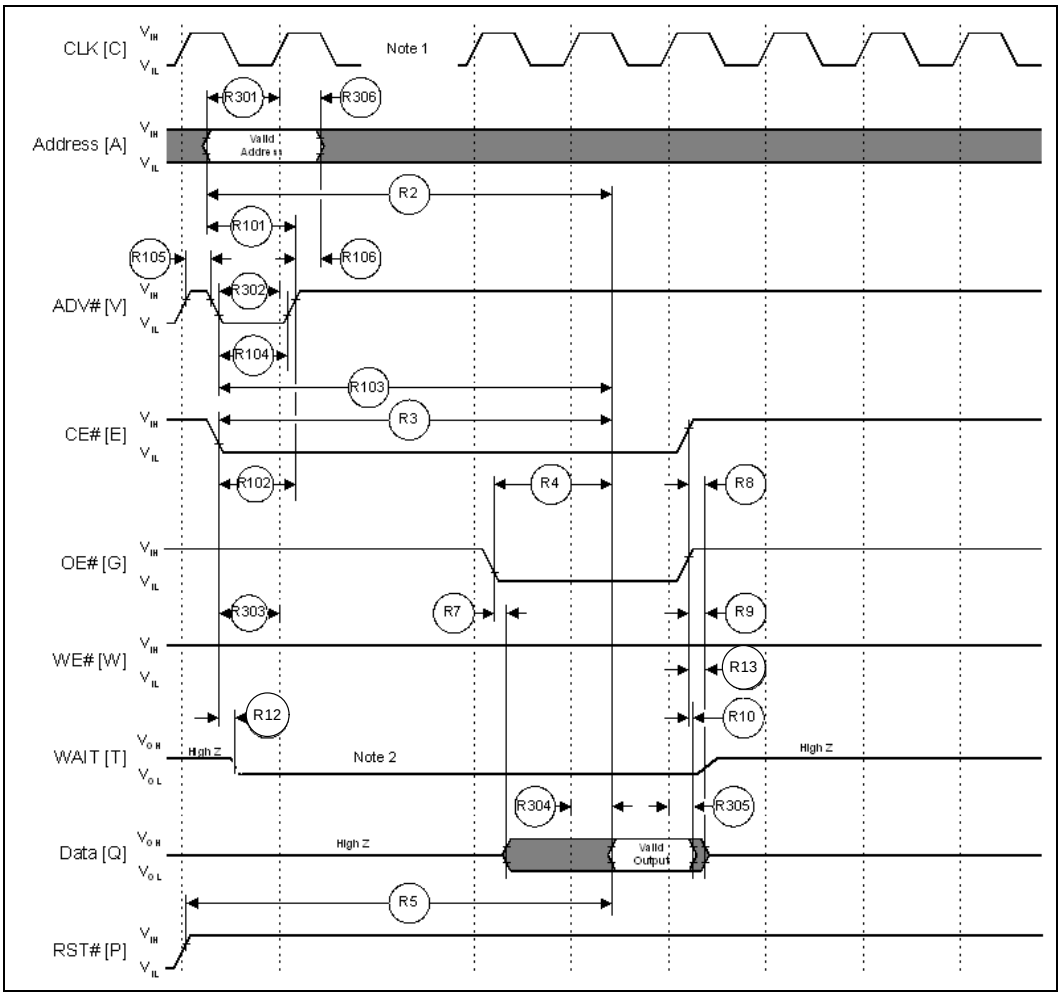
Figure 13. WAIT Functionality for EOWL (End-of-Word Line) Condition Waveform



Notes:

1. Section 14.2, "First Access Latency Count (RCR[13:11])" on page 83 describes how to insert clock cycles during the initial access.
2. WAIT (shown asserted; RCR[10]=0) can be configured to assert either during, or one data cycle before, valid data. (This example assumes a wait delay of two clocks.)

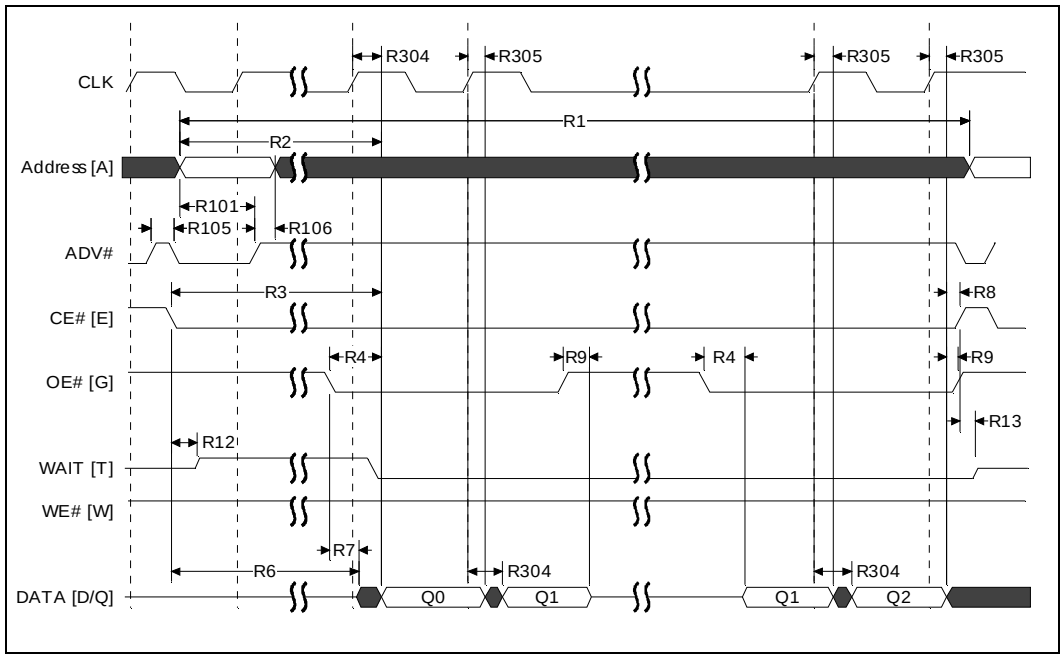
Figure 14. WAIT Signal in Synchronous Non-Read Array Operation Waveform



Notes:

1. Section 14.2, "First Access Latency Count (RCR[13:11])" on page 83 describes how to insert clock cycles during the initial access.
2. WAIT shown asserted (RCR[10]=0).

Figure 15. Burst Suspend



Note:

1. During Burst Suspend, the Clock signal can be held high or low.

7.3 AC Write Characteristics

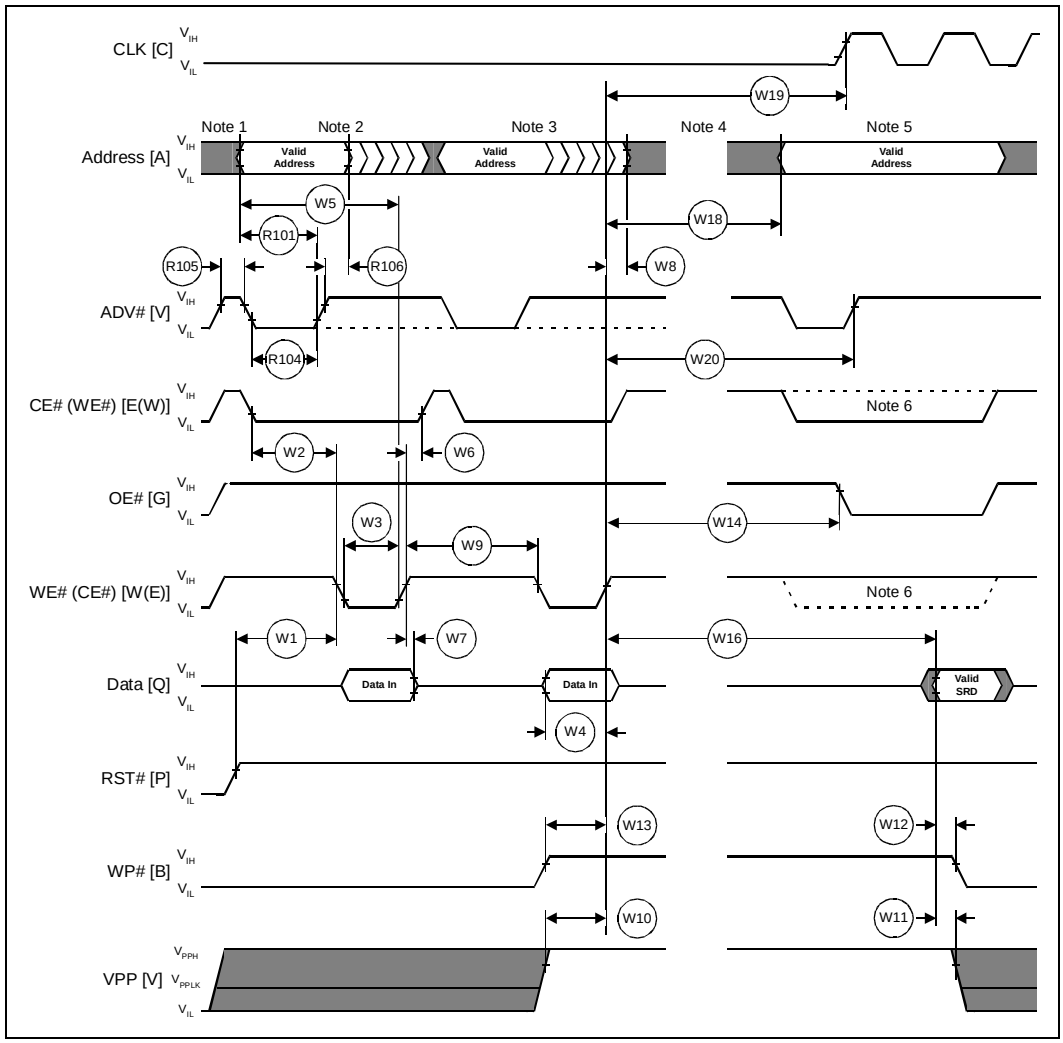
Table 13. AC Write Characteristics

#	Sym	Parameter [1,2]	Notes	32-Mbit 64-Mbit 128-Mbit				Unit
				-70		-85 / -90		
				Min	Max	Min	Max	
W1	t_{PHWL} (t_{PHEL})	RST# High Recovery to WE# (CE#) Low	3	150	-	150	-	ns
W2	t_{ELWL} (t_{WLEL})	CE# (WE#) Setup to WE# (CE#) Low		0	-	0	-	ns
W3	t_{WLWH} (t_{ELEH})	WE# (CE#) Write Pulse Width Low	4	45	-	60	-	ns
W4	t_{DVWH} (t_{DVEH})	Data Setup to WE# (CE#) High		45	-	60	-	ns
W5	t_{AVWH} (t_{AVEH})	Address Setup to WE# (CE#) High		45	-	60	-	ns
W6	t_{WHEH} (t_{EHWH})	CE# (WE#) Hold from WE# (CE#) High		0	-	0	-	ns
W7	t_{WHDX} (t_{EHDX})	Data Hold from WE# (CE#) High		0	-	0	-	ns
W8	t_{WHAX} (t_{EHAX})	Address Hold from WE# (CE#) High		0	-	0	-	ns
W9	t_{WHWL} (t_{EHEL})	WE# (CE#) Pulse Width High	5,6,7	25	-	25	-	ns
W10	t_{VPWH} (t_{VPEH})	VPP Setup to WE# (CE#) High	3	200	-	200	-	ns
W11	t_{QVVL}	VPP Hold from Valid SRD	3,8	0	-	0	-	ns
W12	t_{QVBL}	WP# Hold from Valid SRD	3,8	0	-	0	-	ns
W13	t_{BHWH} (t_{BHEH})	WP# Setup to WE# (CE#) High	3	200	-	200	-	ns
W14	t_{WHGL} (t_{EHGL})	Write Recovery before Read	-	0	-	0	-	ns
W16	t_{WHQV}	WE# High to Valid Data	3,6,10	t_{AVQV} + 40	-	t_{AVQV} + 50	-	ns
W18	t_{WHAV}	WE# High to Address Valid	3,9,10	0	-	0	-	ns
W19	t_{WHCV}	WE# High to CLK Valid	3,10	20	-	20	-	ns
W20	t_{WHVH}	WE# High to ADV# High	3,10	20	-	20	-	ns

Notes:

1. Write timing characteristics during erase suspend are the same as during write-only operations.
2. A write operation can be terminated with either CE# or WE#.
3. Sampled, not 100% tested.
4. Write pulse width low (t_{WLWH} or t_{ELEH}) is defined from CE# or WE# low (whichever occurs last) to CE# or WE# high (whichever occurs first). Hence, $t_{WLWH} = t_{ELEH} = t_{WLEH} = t_{ELWH}$.
5. Write pulse width high (t_{WHWL} or t_{EHEL}) is defined from CE# or WE# high (whichever is first) to CE# or WE# low (whichever is last). Hence, $t_{WHWL} = t_{EHEL} = t_{WHEL} = t_{EHWL}$.
6. System designers must take this into account, and can insert a software No-Op instruction to delay the first read after issuing a command.
7. For commands other than resume commands.
8. V_{PP} must be held at V_{PPL} or V_{PPH} until block erase or program success is determined.
9. Applicable during asynchronous reads following a write.
10. $t_{WHCH/L}$ OR t_{WHVH} must be met when transitioning from a write cycle to a synchronous burst read. $t_{WHCH/L}$ and t_{WHVH} both refer to the address latching event (either the rising/falling clock edge or the rising ADV# edge, whichever occurs first).

Figure 16. Write Operations Waveform



Notes:

1. V_{CC} power-up and standby.
2. Write Program or Erase Setup command.
3. Write valid address and data (for program) or Erase Confirm command.
4. Automated program/erase delay.
5. Read status register data (SRD) to determine program/erase operation completion.
6. OE# and CE# must be asserted and WE# must be deasserted for read operations.
7. CLK is ignored (but can be kept active/toggling).

Figure 17. Asynchronous Read to Write Operation Waveform

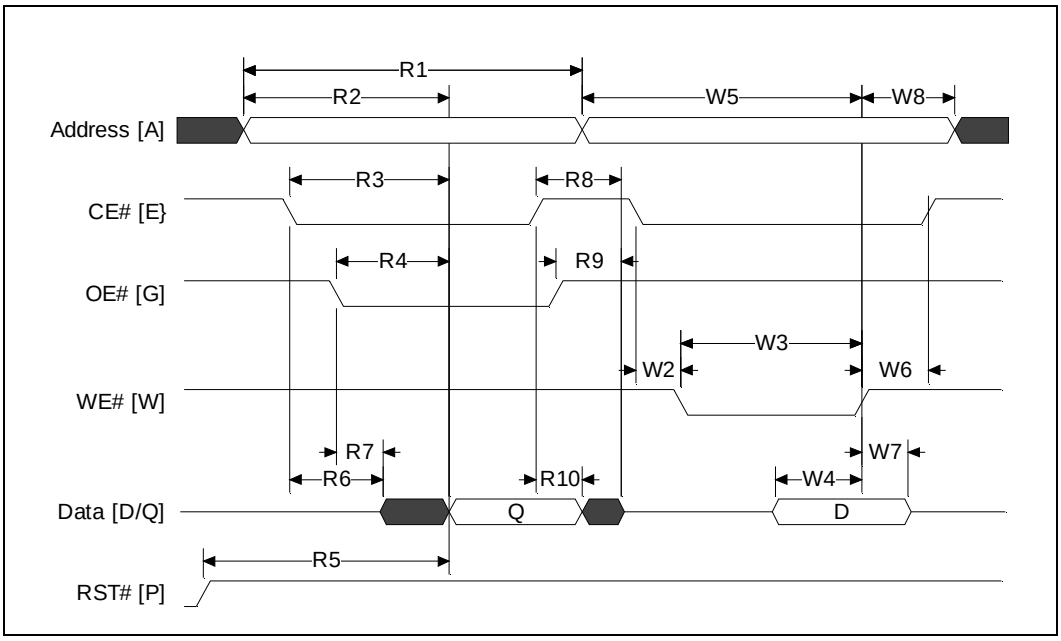


Figure 18. Asynchronous Write to Read Operation

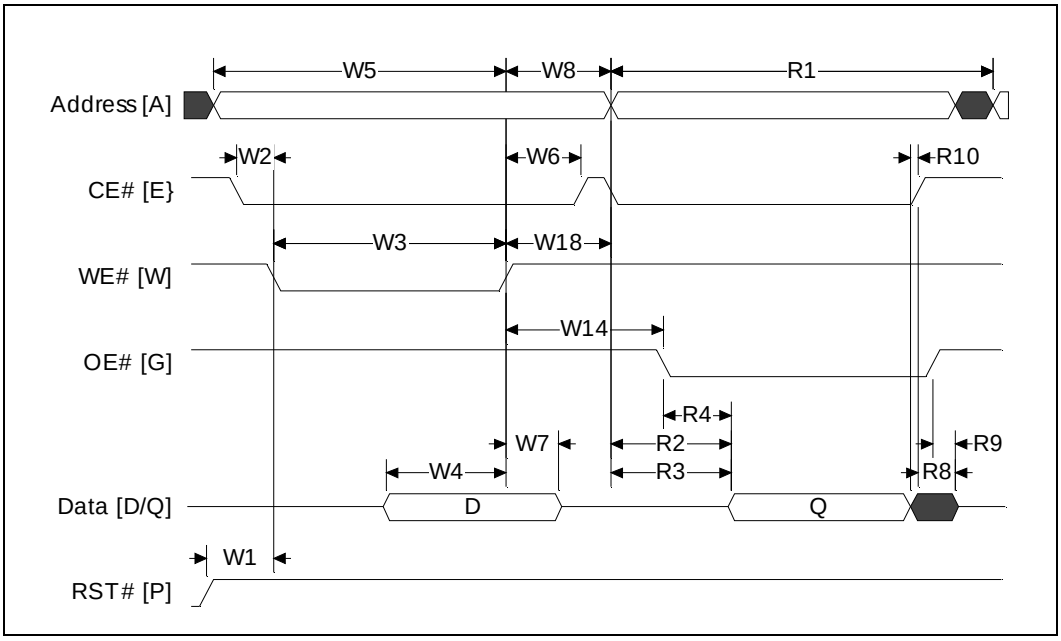


Figure 19. Synchronous Read to Write Operation

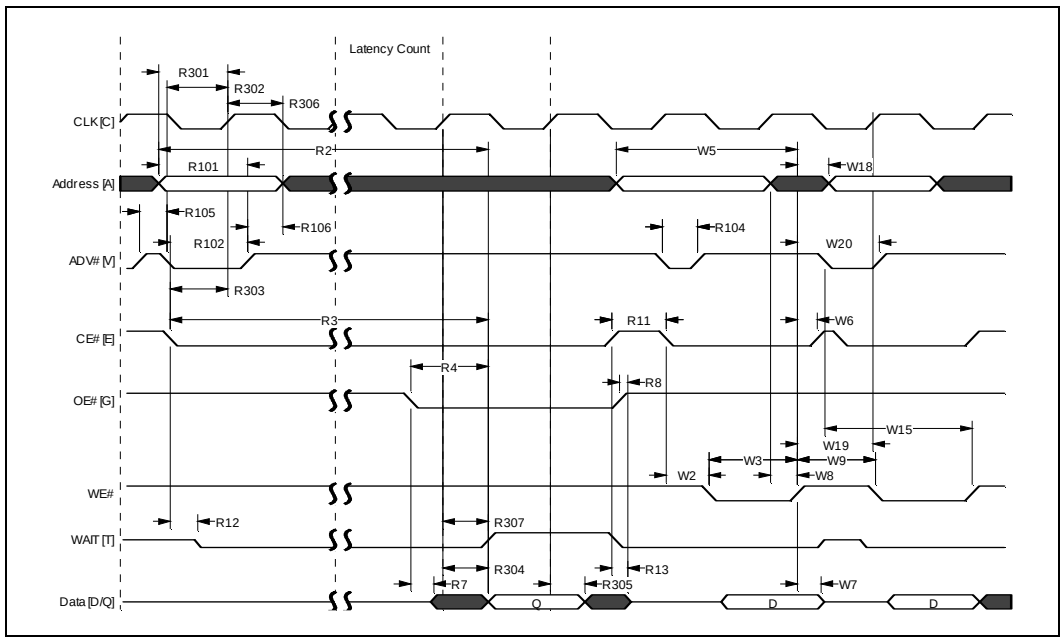
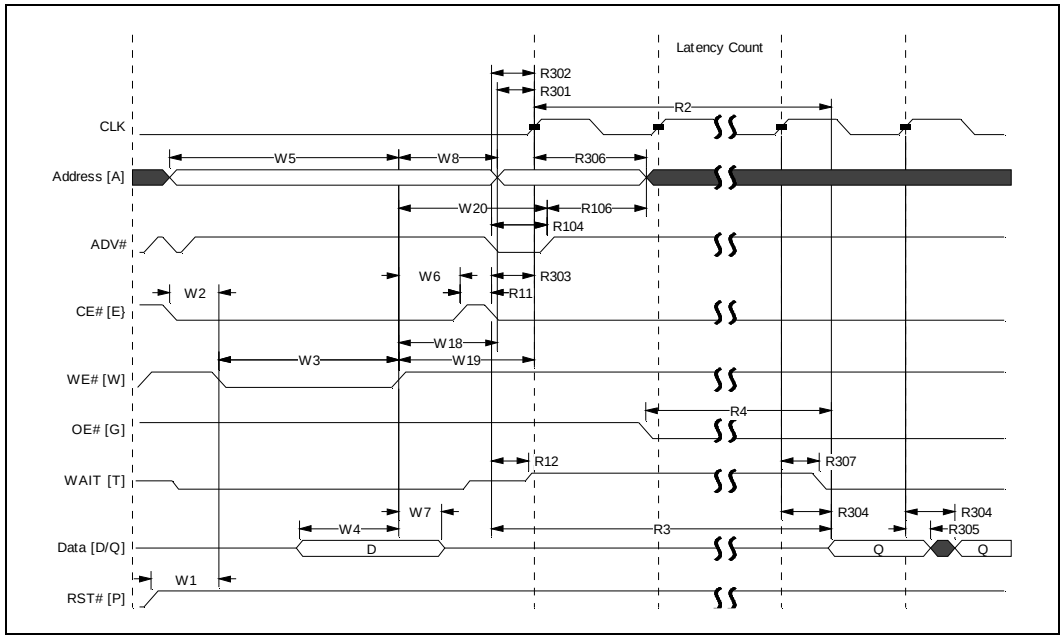


Figure 20. Synchronous Write To Read Operation



7.4 Erase and Program Times

Table 14. Erase and Program Times

Operation	Symbol	Parameter	Description[1]	Notes	V_{PPL}		V_{PPH}		Unit
					Typ	Max	Typ	Max	
Erasing and Suspending									
Erase Time	W500	tERS/PB	4-Kword Parameter Block	2,3	0.3	2.5	0.25	2.5	s
	W501	$t_{ERS/MB}$	32-Kword Main Block	2,3	0.7	4	0.4	4	s
Suspend Latency	W600	$t_{SUSP/P}$	Program Suspend	2	5	10	5	10	µs
	W601	$t_{SUSP/E}$	Erase Suspend	2	5	20	5	20	µs
Programming									
Program Time	W200	tPROG/W	Single Word	2	12	150	8	130	µs
	W201	tPROG/PB	4-Kword Parameter Block	2,3	0.05	.23	0.03	0.07	s
	W202	tPROG/MB	32-Kword Main Block	2,3	0.4	1.8	0.24	0.6	s
Enhanced Factory Programming[5]									
Program	W400	tEFP/W	Single Word	4	N/A	N/A	3.5	16	µs
	W401	tEFP/PB	4-Kword Parameter Block	2,3	N/A	N/A	15	-	ms
	W402	tEFP/MB	32-Kword Main Block	2,3	N/A	N/A	120	-	ms
Operation Latency	W403	$t_{EFP/SETUP}$	EFP Setup	-	N/A	N/A	-	5	µs
	W404	$t_{EFP/TRAN}$	Program to Verify Transition	-	N/A	N/A	2.7	5.6	µs
	W405	$t_{EFP/VERIFY}$	Verify	-	N/A	N/A	1.7	130	µs

Notes:

1. Unless noted otherwise, all parameters are measured at T_A = +25 °C and nominal voltages, and are sampled, not 100% tested.
2. Excludes external system-level overhead.
3. Exact results might vary based on system overhead.
4. W400-Typ is the calculated delay for a single programming pulse. W400-Max includes the delay when programming within a new word-line.
5. Some EFP performance degradation might occur if block cycling exceeds 10.

8.0 Power and Reset Specifications

Intel® Wireless Flash Memory (W30) devices have a layered approach to power savings that can significantly reduce overall system power consumption.

- The APS feature reduces power consumption when the flash device is selected but idle.
- If CE# is deasserted, the memory enters its standby mode, where current consumption is even lower.
- Asserting RST# provides current savings similar to standby mode.

The combination of these features can minimize memory power consumption, and therefore, overall system power consumption.

8.1 Active Power

With CE# at V_{IL} and RST# at V_{IH}, the flash device is in the active mode. Refer to Section 6.1, "DC Current Characteristics" on page 27, for I_{CC} values. When the flash device is in *active* state, it consumes the most power from the system. Minimizing flash device active current therefore reduces system power consumption, especially in battery-powered applications.

8.2 Automatic Power Savings (APS)

Automatic Power Saving (APS) provides low power operation during a read active state. I_{CCAPS} is the average current measured over any 5 ms time interval, 5 µs after CE# is deasserted. During APS, average current is measured over the same time interval 5 µs after the following events:

- There is no internal read, program or erase activity.
- CE# is asserted.
- The address lines are quiescent, and at V_{IL} or V_{IH}.

OE# can be driven during APS.

8.3 Standby Power

When CE# is deasserted, the flash device is deselected and placed in standby, substantially reducing power consumption. In standby, the data outputs are placed in High-Z, independent of the level placed on OE#. Standby current, I_{CCS}, is the average current measured over any 5 ms time interval, 5 µs after CE# is deasserted. During standby, average current is measured over the same time interval 5 µs after CE# is deasserted.

When the flash device is deselected (while CE# is deasserted) during a program or erase operation, it continues to consume active power until the program or erase operation completes.

8.4 Power-Up/Down Characteristics

The flash device is protected against accidental block erasure or programming during power transitions. Power supply sequencing is not required if V_{CC} and V_{PP} are connected together; so it does not matter whether V_{PP} or V_{CC} powers-up first. If V_{PP} is not connected to the system supply, then V_{CC} must attain V_{CCMIN} before applying V_{CCQ} and V_{PP}. Do not drive flash device inputs before supply voltage = V_{CCQMIN}. Power supply transitions can occur only when RST# is low.

8.4.1 System Reset and RST#

The use of RST# during system reset is important with automated program/erase flash devices, because the system expects to read from the flash memory when it comes out of reset. If a CPU reset occurs without a flash memory reset, the CPU is not properly initialized, because the flash memory might be providing status information instead of array data.

Note: To allow proper CPU/flash device initialization at system reset, connect RST# to the system CPU RESET# signal.

System designers must guard against spurious writes when VCC voltages are above V_{LKO}. Because both WE# and CE# must be low for a command write, driving either signal to V_{IH} inhibits writes to the flash device. The CUI architecture provides additional protection, because memory contents can be altered only *after* successful completion of the two-step command sequences.

The flash device is also disabled until RST# is brought to V_{IH}, regardless of its control input states.

By holding the flash device in reset (RST# connected to system PowerGood) during power-up/down, invalid bus conditions during power-up can be masked, providing yet another level of memory protection.

8.4.2 VCC, VPP, and RST# Transitions

The CUI latches commands issued by system software, and is not altered by VPP or CE# transitions or WSM actions. Read-array mode is the power-up default state after the flash device exits from reset mode or after VCC transitions above V_{LKO} (Lockout voltage).

After completing program or block erase operations (even after VPP transitions below V_{PPLK}), the Read Array command must reset the CUI to read-array mode if flash memory array access is desired.

8.5 Power Supply Decoupling

When the flash device is accessed, many internal conditions change. Circuits are enabled to charge pumps and switch voltages. This internal activity produces transient noise.

To minimize the effect of this transient noise, device decoupling capacitors are required. Transient current magnitudes depend on the flash device output capacitive and inductive loading. Two-line control and proper decoupling capacitor selection suppresses these transient voltage peaks.

Note: Each flash device must have a 0.1 µF ceramic capacitor connected between each power (VCC, VCCQ, VPP), and ground (VSS, VSSQ) signal. High-frequency, inherently low-inductance capacitors must be as close as possible to the package signals.

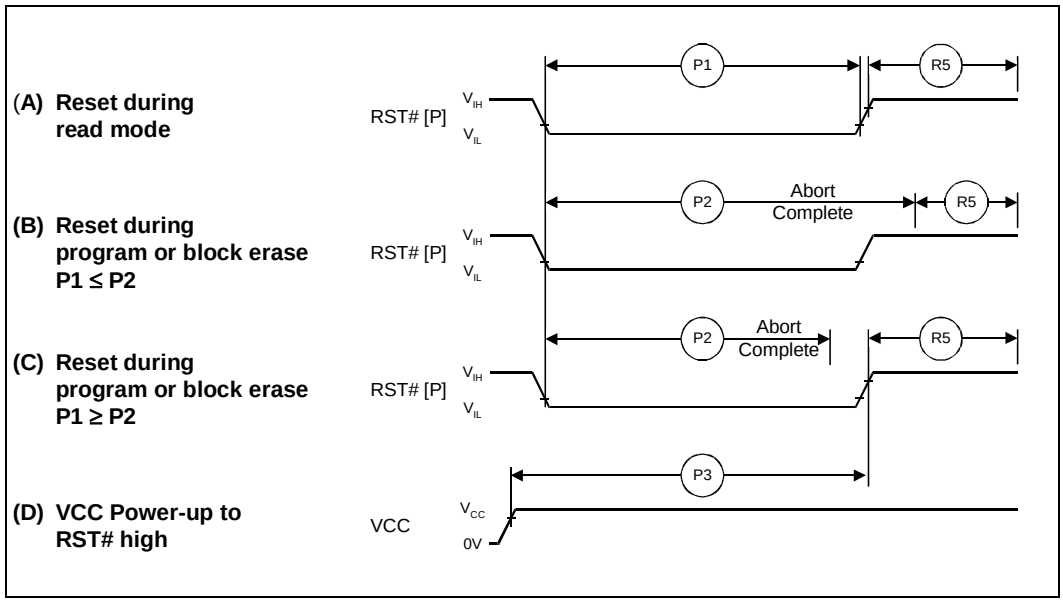
8.6 Reset Specifications

Table 15. Reset Specifications

#	Symbol	Parameter[1]	Notes	Min	Max	Unit
P1	t_{PLPH}	RST# Low to Reset during Read	1, 2, 3, 4	100	-	ns
P2	t_{PLRH}	RST# Low to Reset during Block Erase	1, 3, 4, 5	-	20	µs
		RST# Low to Reset during Program	1, 3, 4, 5	-	10	µs
P3	t_{VCCPH}	VCC Power Valid to Reset	1,3,4,5,6	60	-	µs

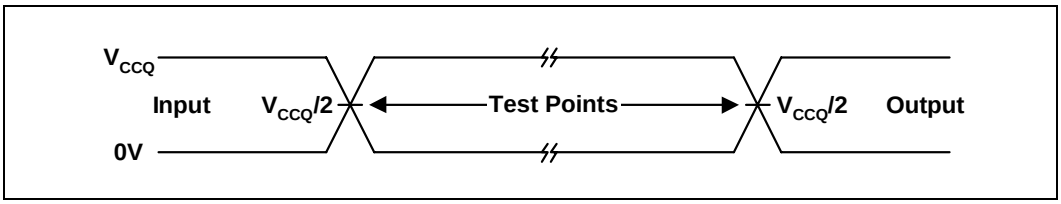
Notes:
1. These specifications are valid for all product versions (packages and speeds).
2. The flash device might reset if $t_{PLPH} < t_{PLPH}$Min, but this is not guaranteed.
3. Not applicable if RST# is tied to VCC.
4. Sampled, but not 100% tested.
5. If RST# is tied to VCC, the flash device is not ready until t_{VCCPH} occurs after when $V_{CC} \geq V_{CC}$Min.
6. If RST# is tied to any supply/signal with V_{CCQ} voltage levels, the RST# input voltage must not exceed V_{CC} until $V_{CC} \geq V_{CC}$Min.

Figure 21. Reset Operations Waveforms



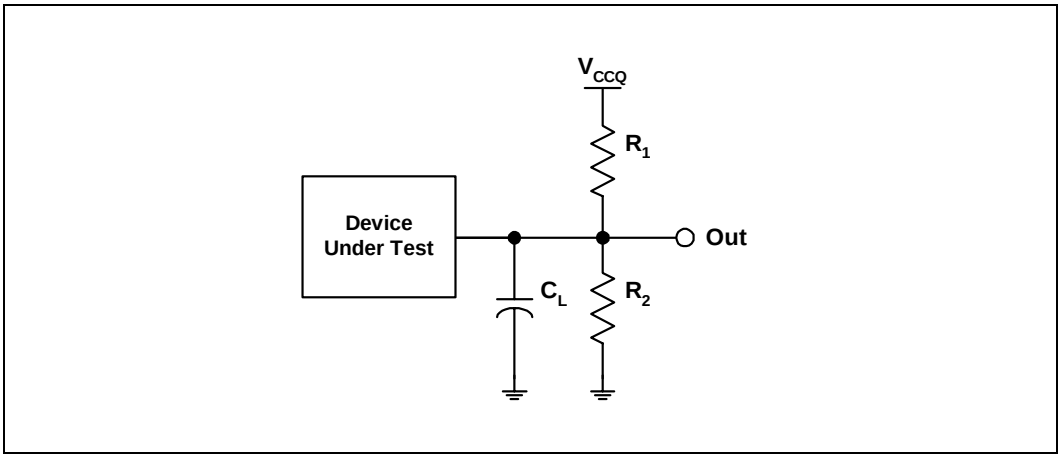
8.7 AC I/O Test Conditions

Figure 22. AC Input/Output Reference Waveform



Note: Input timing begins, and output timing ends, at $V_{CCQ}/2$. Input rise and fall times (10% to 90%) < 5 ns. Worst case speed conditions are when $V_{CC} = V_{CC}$Min.

Figure 23. Transient Equivalent Testing Load Circuit



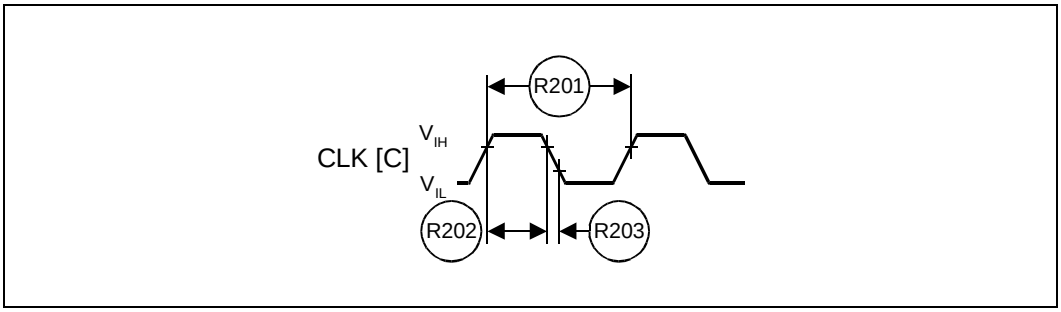
Note: See Table 16 for component values.

Table 16. Test Configuration Component Values for Worst Case Speed Conditions

Test Configuration	C_L (pF)	R_1 (kΩ)	R_1 (kΩ)
V_{CCQ}Min Standard Test	30	25	25

Note: C_L includes jig capacitance.

Figure 24. Clock Input AC Waveform



8.8 Flash Device Capacitance

T_A = +25 °C, f = 1 MHz

Symbol	Parameter[§]	Typ	Max	Unit	Condition
C_{IN}	Input Capacitance	6	8	pF	V_{IN} = 0.0 V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0.0 V
C_{CE}	CE# Input Capacitance	10	12	pF	V_{IN} = 0.0 V

[§]Sampled, not 100% tested.

9.0 Flash Device Operations

This chapter provides an overview of flash device operations. The W30 flash memory device family includes an on-chip Write State Machine (WSM) to manage block erase and program algorithms. The WSM Command User Interface (CUI) allows minimal processor overhead with RAM-like interface timings.

9.1 Bus Operations

Table 17. Bus Operations Summary

Bus Operation		RST#	CLK	ADV#	CE#	OE#	WE#	WAIT	DQ[15:0]	Notes
Read	Asynchronous	V_{IH}	X	L	L	L	H	Asserted	Output	-
	Synchronous	V_{IH}	Running	L	L	L	H	Driven	Output	1
	Burst Suspend	V_{IH}	Halted	X	L	H	H	Active	Output	-
Write		V_{IH}	X	L	L	H	L	Asserted	Input	2
Output Disable		V_{IH}	X	X	L	H	H	Asserted	High-Z	3
Standby		V_{IH}	X	X	H	X	X	High-Z	High-Z	3
Reset		V_{IL}	X	X	X	X	X	High-Z	High-Z	3,4

Notes:
1. WAIT is valid only during synchronous array-read operations.
2. Refer to the Table 19, “Bus Cycle Definitions” on page 55 for valid DQ[15:0] during a write operation.
3. X = Don’t Care (H or L).
4. RST# must be at V_{SS} ± 0.2 V to meet the maximum specified power-down current.

9.1.1 Read

The W30 flash memory device has several read configurations:

- Asynchronous page mode read.
- Synchronous burst mode read — outputs four, eight, sixteen, or continuous words, from main blocks and parameter blocks.

Several read modes are available in each partition:

- **Read-array mode:** read accesses return flash memory array data from the addressed locations.
- **Read identifier mode:** reads return manufacturer and device identifier data, block lock status, and protection register data. Identifier information can be accessed starting at a 4-Mbit partition base addresses; the flash memory array is not accessible in read identifier mode.
- **Read query mode:** reads return the flash device CFI data. CFI information can be accessed starting at a 4-Mbit partition base addresses; the flash memory array is not accessible in read query mode.
- **Read status register mode:** reads return status register data from the addressed partition. The array data for that partition is not accessible. A system processor can check the status register to determine the state of an addressed partition, or to monitor program and erase progress.

All partitions support the synchronous burst mode that internally sequences addresses with respect to the input CLK to select and supply data to the outputs.

Identifier codes, query data, and status register read operations execute as single-synchronous or asynchronous read cycles. WAIT is asserted during these reads.

Access to the modes listed above is independent of V_{PP}. An appropriate CUI command places the flash device in a read mode. At initial power-up or after reset, the flash device defaults to asynchronous read-array mode.

Asserting CE# enables flash device read operations. The flash device internally decodes upper address inputs to determine which partition is accessed.

- Asserting ADV# opens the internal address latches.
- Asserting OE# activates the outputs, and gates the selected data onto the I/O bus.
- In asynchronous mode, the address is latched when ADV# is deasserted (when the flash device is configured to use ADV#).
- In synchronous mode, the address is latched by either the rising edge of ADV# or the rising (or falling) CLK edge while ADV# remains asserted, whichever occurs first.

WE# and RST# must be deasserted during read operations.

Note: If only asynchronous reads are to be performed in your system, CLK must be tied to a valid V_{IH} level, the WAIT signal can be floated, and ADV# must be tied to ground.

9.1.2 Burst Suspend

The Burst Suspend feature allows the system to temporarily suspend a synchronous burst operation if the system needs to use the flash device address and data bus for other purposes. Burst accesses can be suspended during the initial latency (before data is received) or after the flash device has output data. When a burst access is suspended, internal array sensing continues and any previously latched internal data is retained.

Burst Suspend occurs when CE# is asserted, the current address has been latched (either ADV# rising edge or valid CLK edge), CLK is halted, and OE# is deasserted. CLK can be halted when it is at V_{IH} or V_{IL}. To resume the burst access, OE# is reasserted and CLK is restarted. Subsequent CLK edges resume the burst sequence where it left off.

Within the flash device, CE# gates the WAIT signal. Therefore, during Burst Suspend, WAIT remains asserted and does not revert to a high-impedance state when OE# is deasserted. This WAIT state can cause contention with another flash device attempting to control the system READY signal during a Burst Suspend. System using the Burst Suspend feature must not connect the flash device WAIT signal directly to the system READY signal.

Refer to Figure 15, “Burst Suspend” on page 39.

9.1.3 Standby

De-asserting CE# deselects the flash device and places it in standby mode, substantially reducing flash device power consumption. In standby mode, outputs are placed in a high-impedance state independent of OE#. If deselected during a program or erase algorithm, the flash device consumes active power until the program or erase operation completes.

9.1.4 Reset

The flash device enters a reset mode when RST# is asserted. In reset mode, internal circuitry is turned off and outputs are placed in a high-impedance state.

After returning from reset, a time t_{PHQV} is required until outputs are valid, and a delay (t_{PHWV}) is required before a write sequence can be initiated. After this wake-up interval, normal operation is restored. The flash device defaults to read-array mode, the status register is set to 80h, and the Read Configuration Register defaults to asynchronous page-mode reads.

If RST# is asserted during an erase or program operation, the operation aborts and the memory contents at the aborted block or address are invalid. See Figure 21, "Reset Operations Waveforms" on page 47 for detailed information regarding reset timings.

As on any automated device, RST# must be asserted during system reset. When the system comes out of reset, the processor expects to read from the flash memory array. Automated flash memory devices provide status information when read during program or erase operations. If a CPU reset occurs with no flash memory reset, the CPU might not be properly initialized, because the flash memory device might be providing status information instead of array data. 1.8 Volt Intel Flash memory devices allow proper CPU initialization following a system reset through the use of the RST# input. In this application, RST# is controlled by the same CPU reset signal, RESET#.

9.1.5 Write

A write occurs when CE# and WE# are asserted and OE# is deasserted. Flash memory control commands are written to the CUI using standard microprocessor write timings. Proper use of the ADV# input is needed for proper latching of the addresses. Refer to Section 7.3, "AC Write Characteristics" on page 40 for details. The address and data are latched on the rising edge of WE#. Write operations are asynchronous; CLK is ignored (but can be kept active/toggling).

The CUI does not occupy an addressable memory location within any partition. The system processor must access it at the correct address range, depending on the kind of command executed. Programming or erasing can occur in only one partition at a time. Other partitions must be in one of the read modes or erase suspend mode.

Table 18, "Command Codes and Descriptions" on page 53 shows the available commands. Appendix A, "Write State Machine" on page 90 provides information about moving between different operating modes using CUI commands.

9.2 Flash Device Commands

The flash device on-chip WSM manages erase and program algorithms. This local CPU (WSM) controls the flash device in-system read, program, and erase operations. Bus cycles to or from the flash memory device conform to standard microprocessor bus cycles. The RST#, CE#, OE#, WE#, and ADV# control signals dictate data flow into and out of the flash device. WAIT informs the CPU of valid data during burst reads. Table 17, "Bus Operations Summary" on page 50 summarizes bus operations.

To select flash device operations, write specific commands into the flash device CUI. Table 18, "Command Codes and Descriptions" on page 53 lists all possible command codes and descriptions. Table 19, "Bus Cycle Definitions" on page 55 lists command definitions. Because commands are partition-specific, you must issue write commands within the target address range.

Table 18. Command Codes and Descriptions (Sheet 1 of 2)

Operation	Code	Flash Device Command	Description
Read	FFh	Read Array	Places the selected partition in read-array mode.
	70h	Read Status Register	Places the selected partition in status register read mode. The partition enters this mode after a Program or Erase command is issued to it.
	90h	Read Identifier	Places the selected partition in read identifier mode. Flash device reads from partition addresses output the manufacturer/device codes, configuration register data, block lock status, or protection register data on D[15:0].
	98h	Read Query	Places the addressed partition in read query mode. Flash device reads from the partition addresses output the CFI information on D[7:0].
	50h	Clear Status Register	The WSM can set the block lock (SR[1]), V_{PP} (SR[3]), program (SR[4]), and erase (SR[5]) status bits of the status register, but WSM cannot clear these bits. SR[5:3,1] can be cleared only by a flash device reset or through the Clear Status Register command.
Program	40h	Word Program Setup	• The first cycle of this preferred program command prepares the CUI for a program operation. • The second cycle latches the address and data, and executes the WSM program algorithm at this location. Status register updates occur when CE# or OE# is toggled. After programming, use a Read Array command to read the array data.
	10h	Alternate Setup	Equivalent to a Program Setup command (40h).
	30h	EFP Setup	This program command activates EFP mode. • The first write cycle sets up the command. • If the second cycle is an EFP Confirm command (D0h), subsequent writes provide program data. All other commands are ignored after EFP mode begins.
	D0h	EFP Confirm	If the first command was EFP Setup (30h), the CUI latches the address and data, and prepares the flash device for EFP mode.
Erase	20h	Erase Setup	This command prepares the CUI for Block Erase. The flash device erases the block that the Erase Confirm command addresses. If the next command is not Erase Confirm, the CUI sets status register bits SR[5:4] to indicate a command sequence error, and places the partition in the read status register mode.
	D0h	Erase Confirm	If the first command was Erase Setup (20h), the CUI latches the address and data, and erases the block indicated by the erase confirm cycle address. During program or erase, the partition responds only to Read Status Register, Program Suspend, and Erase Suspend commands. CE# or OE# toggle updates the status register data.
Suspend	B0h	Program Suspend or Erase Suspend	This command, issued at any flash device address, suspends the currently executing program or erase operation. Status register data indicates that the operation was successfully suspended if SR[2] (program suspend) or SR[6] (erase suspend) and SR[7] are set. The WSM remains in the suspended state regardless of the control signal states (except RST#).
	D0h	Suspend Resume	This command, issued at any flash device address, resumes the suspended program or erase operation.

Table 18. Command Codes and Descriptions (Sheet 2 of 2)

Operation	Code	Flash Device Command	Description
Block Locking	60h	Lock Setup	This command prepares the CUI lock configuration. If the next command is not Lock Block, Unlock Block, or Lock-Down, the CUI sets SR[5:4] to indicate a command sequence error.
	01h	Lock Block	If the previous command was Lock Setup (60h), the CUI locks the addressed block.
	D0h	Unlock Block	If the previous command was Lock Setup (60h), the CUI latches the address and unlocks the addressed block. If previously locked-down, the operation has no effect.
	2Fh	Lock-Down	If the previous command was Lock Setup (60h), the CUI latches the address and locks-down the addressed block.
Protection	C0h	Protection Program Setup	This command prepares the CUI for a protection register program operation. The second cycle latches address and data, and starts the WSM protection register program or lock algorithm. Toggling CE# or OE# updates the flash device status register data. To read array data after programming, issue a Read Array command.
Configuration	60h	Configuration Setup	This command prepares the CUI for flash device configuration. If Set Configuration Register is not the next command, the CUI sets SR[5:4] to indicate a command sequence error.
	03h	Set Configuration Register	If the previous command was Configuration Setup (60h), the CUI latches the address and writes the data from A[15:0] into the configuration register. Subsequent read operations access the array data.

Note: Do not use unassigned commands. Intel reserves the right to redefine these codes for future functions.

Table 19. Bus Cycle Definitions

Operation	Command	Bus Cycles	First Bus Cycle			Second Bus Cycle		
			Oper	Addr[1]	Data[2,3]	Oper	Addr[1]	Data[2,3]
Read	Read Array/Reset	≥ 1	Write	PnA	FFh	Read	Read Address	Array Data
	Read Identifier	≥ 2	Write	PnA	90h	Read	PBA+IA	IC
	Read Query	≥ 2	Write	PnA	98h	Read	PBA+QA	QD
	Read Status Register	2	Write	PnA	70h	Read	PnA	SRD
	Clear Status Register	1	Write	XX	50h			
Program and Erase	Block Erase	2	Write	BA	20h	Write	BA	D0h
	Word Program	2	Write	WA	40h/10h	Write	WA	WD
	EFP	≥2	Write	WA	30h	Write	WA	D0h
	Program/Erase Suspend	1	Write	XX	B0h			
	Program/Erase Resume	1	Write	XX	D0h			
Lock	Lock Block	2	Write	BA	60h	Write	BA	01h
	Unlock Block	2	Write	BA	60h	Write	BA	D0h
	Lock-Down Block	2	Write	BA	60h	Write	BA	2Fh
Protection	Protection Program	2	Write	PA	C0h	Write	PA	PD
	Lock Protection Program	2	Write	LPA	C0h	Write	LPA	FFFDh
Configuration	Set Configuration Register	2	Write	CD	60h	Write	CD	03h

Notes:

1. First-cycle command addresses must be the same as the target address of the operation. Examples:
   —The first-cycle address for the Read Identifier command must be the same as the Identification code address (IA).
   —The first-cycle address for the Word Program command must be the same as the word address (WA) to be programmed.
   —The first-cycle address for the Erase/Program Suspend command must be the same as the address within the block to be suspended.
   XX = Any valid address within the flash device.
   IA = Identification code address.
   BA = Block Address. Any address within a specific block.
   LPA = The Lock Protection Address is obtained from the CFI (through the Read Query command). The W30 flash memory device family LPA is at 0080h.
   PA = User programmable 4-word protection address.
   PnA = Any address within a specific partition.
   PBA = Partition Base Address. The first address of a particular partition.
   QA = Query code address.
   WA = Word address of memory location to be written.
2. SRD = Status register data.
   WD = Data to be written at location WA.
   IC = Identifier code data.
   PD = User programmable 4-word protection data.
   QD = Query code data on D[7:0].
   CD = Configuration register code data presented on flash device addresses A[15:0]. A[MAX:16] address bits can select any partition. See Table 27, “Read Configuration Register Definitions” on page 81 for configuration register bits descriptions.
3. Do not use commands other than those shown above. Other commands are reserved by Intel for future flash device implementations.

9.3 Command Sequencing

When issuing a 2-cycle write sequence to the flash device, a read operation can occur *between* the two write cycles. The setup phase of a 2-cycle write sequence places the addressed partition into read-status mode, so if the same partition is read before the second *confirm* write cycle is issued, status register data is returned. Reads from other partitions, however, can return actual array data, if the addressed partition is already in read-array mode. Figure 25 and Figure 26 illustrate these two conditions.

Figure 25. Normal Write and Read Cycles

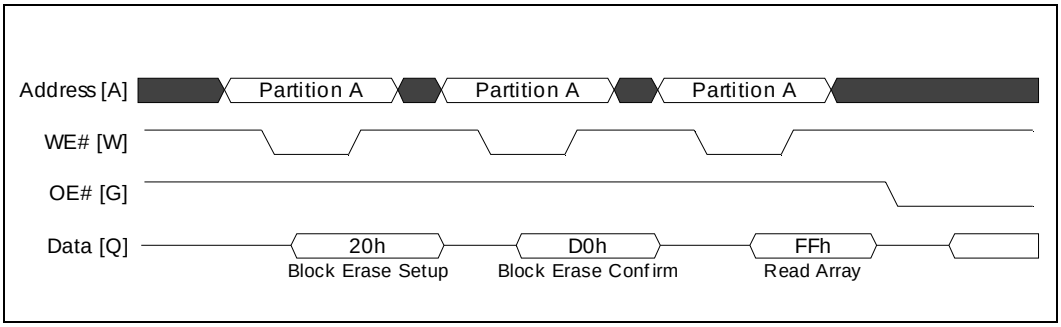
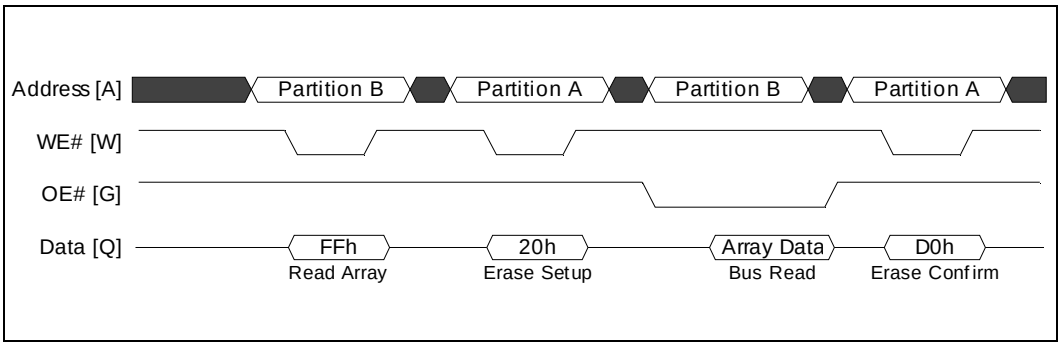
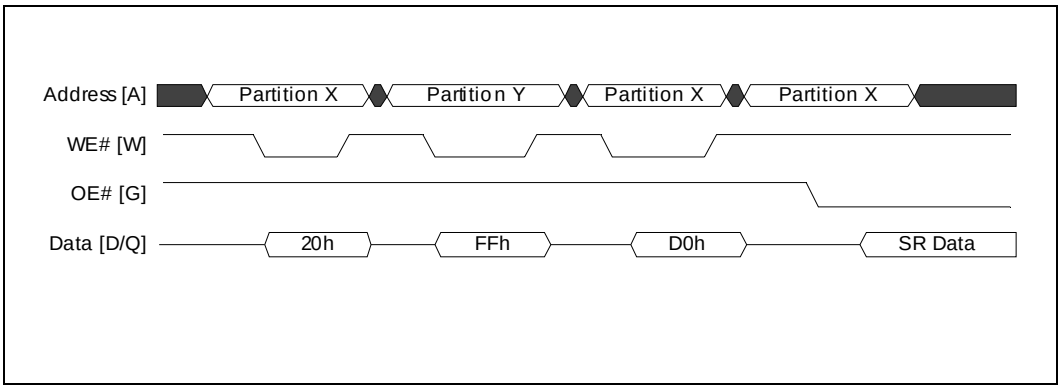


Figure 26. Interleaving a 2-Cycle Write Sequence with an Array Read



By contrast, a write bus cycle must not interrupt a 2-cycle write sequence. Such an interruption causes a command sequence error to appear in the status register. Figure 27 illustrates a command sequence error.

Figure 27. Improper Command Sequencing



10.0 Read Operations

10.1 Read Array

The Read Array command places (or resets) the partition in read-array mode and is used to read data from the flash memory array. Upon initial flash device power-up, or after reset (RST# transitions from V_{IL} to V_{IH}), all partitions default to asynchronous read-array mode.

To read array data from the flash device:

1. Write the Read Array command (FFh) to the CUI and specify the desired word address.
1. Read from that address.

Note: If a partition is already in read-array mode, you do not need to issue the Read Array command to read from that partition.

If the Read Array command is written to a partition that is erasing or programming, the flash device presents invalid data on the bus until the program or erase operation completes.

After the program or erase finishes in that partition, valid array data can then be read. If an Erase Suspend or Program Suspend command suspends the WSM, a subsequent Read Array command places the addressed partition in read-array mode.

The Read Array command functions independently of V_{PP}.

10.2 Read Device ID

The read identifier mode outputs the manufacturer/device identifier, block lock status, protection register codes, and configuration register data. The identifier information is contained within a separate memory space on the flash device, and can be accessed along the 4-Mbit partition address range supplied by the Read Identifier command (90h) address. Reads from addresses in Table 20 retrieve ID information. Issuing a Read Identifier command to a partition that is programming or erasing places the outputs of that partition in read ID mode while the partition continues to program or erase in the background.

Table 20. Flash Device Identification Codes (Sheet 1 of 2)

Item	Address[1]		Data	Description
	Base	Offset		
Manufacturer ID	Partition	00h	0089h	Intel
Device ID	Partition	01h	8852h	32-Mbit TPD
			8853h	32-Mbit BPD
			8854h	64-Mbit TPD
			8855h	64-Mbit BPD
			8856h	128-Mbit TPD
			8857h	128-Mbit BPD

Table 20. Flash Device Identification Codes (Sheet 2 of 2)

Item	Address[1]		Data	Description
	Base	Offset		
Block Lock Status[2]	Block	02h	D0 = 0	Block is unlocked
			D0 = 1	Block is locked
Block Lock-Down Status[2]	Block	02h	D1 = 0	Block is not locked-down
			D1 = 1	Block is locked down
Configuration Register	Partition	05h	Register Data	
Protection Register Lock Status	Partition	80h	Lock Data	
Protection Register	Partition	81h - 88h	Register Data	Multiple reads required to read the entire 128-bit Protection Register.

Notes:
1. The address is constructed from a base address plus an offset. For example, to read the Block Lock Status for block number 38 in a BPD, set the address to the BBA (0F8000h) plus the *offset* (02h), which in this example is 0F8002h. Then examine bit 0 of the data to determine whether the block is locked.
2. See Section 13.1.4, "Block Lock Status" on page 75 for valid lock status.

10.3 Read Query (CFI)

The W30 flash memory device contains a separate CFI query *database* that acts as an on-chip datasheet. To access the CFI information within the W30 flash memory device, issue the Read Query command and supply a specific address.

The address is constructed from the base address of a partition plus a particular offset corresponding to the desired CFI field.

Appendix B, "Common Flash Interface" on page 93 shows accessible CFI fields and their address offsets. Issuing the Read Query command to a partition that is programming or erasing puts that partition in read query mode while the partition continues to program or erase in the background.

10.4 Read Status Register

The flash device status register displays program and erase operation status. The status of a partition can be read after writing the Read Status Register command to any location within the address range of that partition. Read-status mode is the default read mode following a Program, Erase, or Lock Block command sequence. Subsequent single reads from that partition return the partition status until another valid command is written.

The read-status mode supports single synchronous and single asynchronous reads only; it does not support burst reads.

The first falling edge of OE# or CE# latches and updates Status Register data. The operation does not affect the modes of other partitions. Because the Status Register is 8 bits wide, only DQ [7:0] contain valid status register data; DQ [15:8] contain zeros. See Table 21, "Status Register Definitions" on page 59 and Table 22, "Status Register Descriptions" on page 59.

Each 4-Mbit partition contains its own status register. Bits SR[6:0] are unique to each partition, but SR[7], the Device WSM Status (DWS) bit, pertains to the entire flash memory device. SR[7] provides the program and erase status of the entire flash device. By contrast, the Partition WSM Status (PWS) bit, SR[0], provides program and erase status of the *addressed partition* only. Status register bits SR[6:1] present information about partition-specific program, erase, suspend, V_{PP}, and block-lock states. Table 23, "Status Register Device WSM and Partition Write Status Description" on page 60 describes the DWS (SR[7]) and PWS (SR[0]) combinations.

Table 21. Status Register Definitions

DWS	ESS	ES	PS	VPPS	PSS	DPS	PWS
7	6	5	4	3	2	1	0

Table 22. Status Register Descriptions

Bit	Name	State	Description
7	**DWS** Device WSM Status	0 = Device WSM is Busy 1 = Device WSM is Ready	• SR[7] indicates erase or program completion in the flash device. • SR[6:1] are invalid while SR[7] = 0. See Table 23 for valid SR[7] and SR[0] combinations.
6	**ESS** Erase Suspend Status	0 = Erase in progress/completed 1 = Erase suspended	After issuing an Erase Suspend command, the WSM halts and sets SR[7] and SR[6]. SR[6] remains set until the flash device receives an Erase Resume command.
5	**ES** Erase Status	0 = Erase successful 1 = Erase error	• SR[5] is set if an attempted erase failed. • A Command Sequence Error is indicated when SR[7,5:4] are set.
4	**PS** Program Status	0 = Program successful 1 = Program error	SR[4] is set if the WSM failed to program a word.
3	**VPPS** VPP Status	0 = V_{PP} OK 1 = V_{PP} low detect, operation aborted	The WSM indicates the V_{PP} level after program or erase completes. SR[3] does not provide continuous V_{PP} feedback and is not guaranteed when $V_{PP} \neq V_{PPL}/V_{PPH}$
2	**PSS** Program Suspend Status	0 = Program in progress/completed 1 = Program suspended	After receiving a Program Suspend command, the WSM halts execution and sets SR[7] and SR[2]. These bits remain set until a Resume command is received.
1	**DPS** Device Protect Status	0 = Unlocked 1 = Aborted erase/program attempt on a locked block	If an erase or program operation is attempted to a locked block (if WP# = V_{IL}), the WSM sets SR[1] and aborts the operation.
0	**PWS** Partition Write Status	0 = This partition is busy, but only if SR[7]=0 1 = Another partition is busy, but only if SR[7]=0	The addressed partition is erasing or programming. In EFP mode, SR[0] indicates that a data-stream word has finished programming or verifying, depending on the particular EFP phase. See Table 23 for valid SR[7] and SR[0] combinations.

Table 23. Status Register Device WSM and Partition Write Status Description

DWS (SR[7])	PWS (SR[0])	Description
0	0	The addressed partition is performing a program/erase operation. EFP: the flash device has finished programming or verifying data, or is ready for data.
0	1	A partition other than the one currently addressed is performing a program/erase operation. EFP: the flash device is either programming or verifying data.
1	0	No program/erase operation is in progress in any partition. Erase and Program suspend bits (SR[6,2]) indicate whether other partitions are suspended. EFP: the flash device has exited EFP mode.
1	1	Does not occur in standard program or erase modes. EFP: this combination does not occur.

10.5 Clear Status Register

The Clear Status Register command clears the status register and leaves all partition output states unchanged. The WSM can set all status register bits and clear bits SR[7:6,2,0]. Because bits SR[5,4,3,1] indicate various error conditions, they can be cleared only by the Clear Status Register command. By allowing system software to reset these bits, several operations (such as cumulatively programming several addresses or erasing multiple blocks in sequence) can be performed before reading the status register to determine whether an error occurred.

If an error is detected, the Status Register must be cleared before beginning another command or sequence. Flash device reset (RST# = V_{IL}) also clears the status register. This command functions independently of V_{PP}.

11.0 Program Operations

11.1 Word Program

When the Word Program command is issued, the WSM executes a sequence of internally timed events to program a word at the desired address, and to verify that the bits are sufficiently programmed. Programming the flash memory array changes specifically addressed bits to 0; 1 bits do not change the memory cell contents.

Programming can occur in only one partition at a time. All other partitions must be in either a read mode or erase suspend mode. Only one partition can be in erase suspend mode at a time.

To examine the status register can be examined for program progress, read any address within the partition that is busy programming. However, while most status register bits are partition-specific, the Device WSM Status bit, SR[7], is *device*-specific. That is, if the status register is read from any other partition, SR[7] indicates the program status of the entire flash memory device. This status bit permits the system CPU to monitor the program progress while reading the status of other partitions.

CE# or OE# toggle (during polling) updates the status register. Several commands can be issued to a partition that is programming: Read Status Register, Program Suspend, Read Identifier, and Read Query. The Read Array command can also be issued, but the read data is indeterminate.

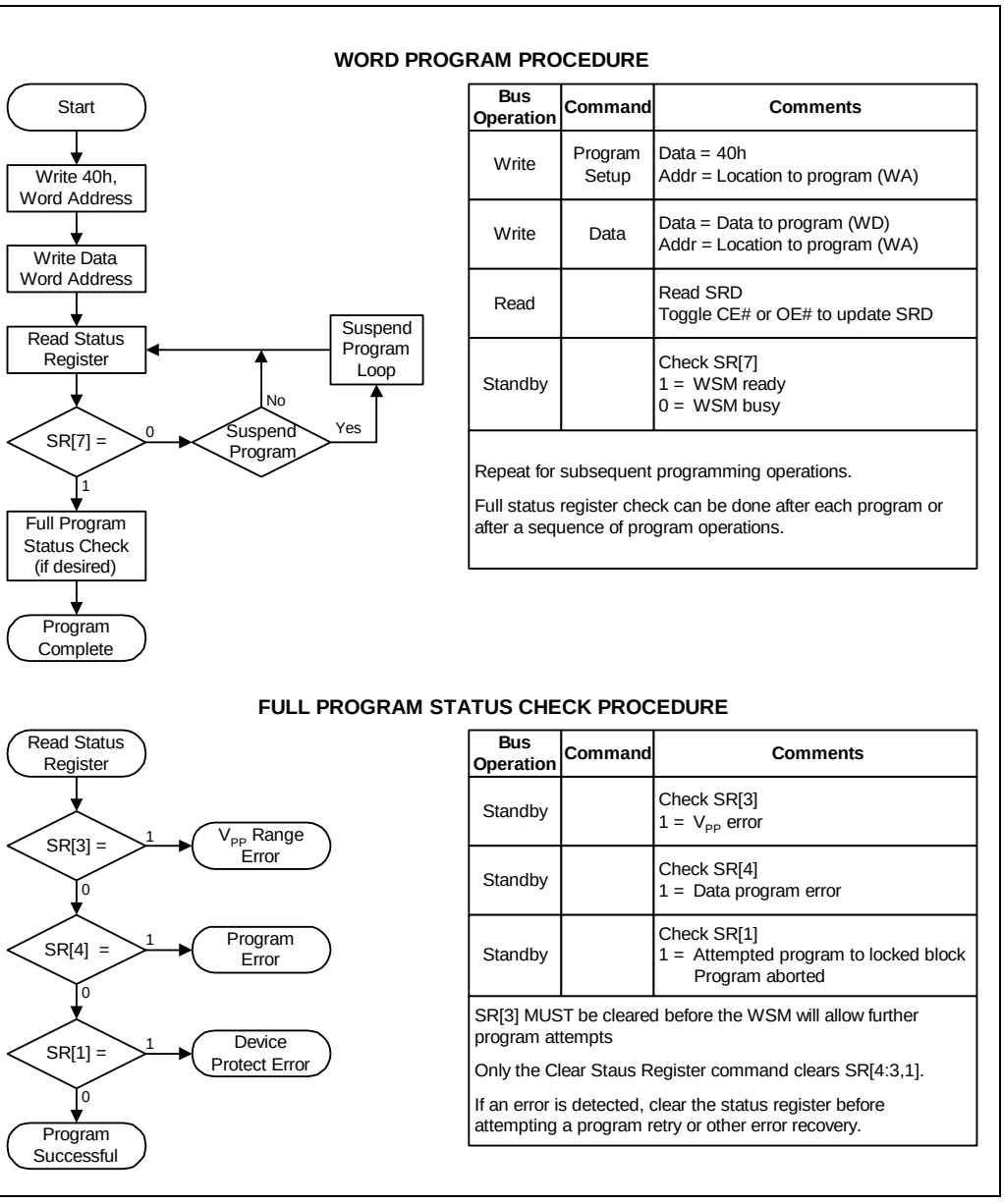
After programming completes, three status register bits can signify various possible error conditions:

- SR[4] indicates a program failure if set.
- If SR[3] is set, the WSM could not execute the Word Program command, because V_{PP} was outside the acceptable limits.
- If SR[1] is set, the program was aborted, because the WSM attempted to program a locked block.

After the status register data is examined, clear it using the Clear Status Register command before issuing a new command. The partition remains in status register mode until another command is written to that partition. Any command can be issued after the status register indicates program completion.

If CE# is deasserted while the flash device is programming, the flash devices do not enter standby mode until the program operation completes.

Figure 28. Word Program Flowchart



Bus Operation	Command	Comments
Write	Program Setup	Data = 40h Addr = Location to program (WA)
Write	Data	Data = Data to program (WD) Addr = Location to program (WA)
Read		Read SRD Toggle CE# or OE# to update SRD
Standby		Check SR[7] 1 = WSM ready 0 = WSM busy

Repeat for subsequent programming operations.

Full status register check can be done after each program or after a sequence of program operations.

Bus Operation	Command	Comments
Standby		Check SR[3] 1 = V_{PP} error
Standby		Check SR[4] 1 = Data program error
Standby		Check SR[1] 1 = Attempted program to locked block Program aborted

SR[3] MUST be cleared before the WSM will allow further program attempts

Only the Clear Staus Register command clears SR[4:3,1].

If an error is detected, clear the status register before attempting a program retry or other error recovery.

11.2 Factory Programming

The standard factory programming mode uses the same commands and algorithm as the Word Program mode (40h/10h). When V_{PP} is at V_{PPL}, program and erase currents are drawn through VCC. If VPP is driven by a logic signal, V_{PPL} must remain above the V_{PPL}Min value to perform in-system flash memory modifications. When VPP is connected to a 12 V power supply, the flash device draws program and erase current directly from VPP, which eliminates the need for an external switching transistor to control the V_{PP} voltage.

Figure 37, "Examples of VPP Power Supply Configurations" on page 80 shows examples of flash device power supply usage in various configurations.

The 12-V V_{PP} mode enhances programming performance during the short time period typically found in manufacturing processes. However, this mode is not intended for extended use.12 V can be applied to V_{PP} during program and erase operations as specified in Section 5.2, "Operating Conditions" on page 26. VPP can be connected to 12 V for a total of t_{PPH} hours maximum. Stressing the flash device beyond these limits might cause permanent damage.

11.3 Enhanced Factory Program (EFP)

EFP substantially improves flash device programming performance through a number of enhancements to the conventional 12-Volt word program algorithm. The more efficient WSM algorithm in EFP eliminates the traditional overhead delays of the conventional word program mode in both the host programming system and the flash device. Changes to the conventional word programming flowchart and internal WSM routine were developed because of today's beat-rate-sensitive manufacturing environments; a balance between programming speed and cycling performance was attained.

The host programmer writes data to the flash device and checks the Status Register to determine when the data has completed programming. This modification cuts write bus cycles approximately in half.

- Following each internal program pulse, the WSM increments the flash device address to the next physical location.
- Programming equipment can then sequentially stream program data throughout an entire block without having to setup and present each new address.

In combination, these enhancements reduce much of the host programmer overhead, enabling more of a data streaming approach to flash device programming.

EFP further speeds up programming by performing internal code verification. With this feature, PROM programmers can rely on the flash device to verify that it has been programmed properly. From the flash device side, EFP streamlines internal overhead by eliminating the delays previously associated with switching voltages between programming and verify levels at each memory-word location.

EFP consists of four phases: setup, program, verify, and exit. Refer to Figure 29, "Enhanced Factory Program Flowchart" on page 66 for a detailed graphical representation of how to implement EFP.

11.3.1 EFP Requirements and Considerations

Table 24. EFP Requirements and Considerations

EFP Requirements	EFP Considerations
Ambient temperature: T_A = 25 °C ±5 °C	Block cycling below 100 erase cycles [1]
V_{CC} within specified operating range	RWW not supported[2]
V_{PP} within specified V_{PPH} range	EFP programs one block at a time
Target block unlocked	EFP cannot be suspended

1. Recommended for optimum performance. Some degradation in performance might occur if this limit is exceeded, but the internal algorithm will continue to work properly.
2. Code or data cannot be read from another partition during EFP.

11.3.2 Setup

After receiving the EFP Setup (30h) and EFP Confirm (D0h) command sequence, SR[7] transitions from a 1 to a 0, indicating that the WSM is busy with EFP algorithm startup. A delay before checking SR[7] is required to allow the WSM time to perform all of its setups and checks (V_{PP} level and block lock status). If an error is detected, status register bits SR[4], SR[3], and/or SR[1] are set, and the EFP operation terminates.

Note: After the EFP Setup and Confirm command sequence, reads from the flash device automatically output status register data. Do not issue the Read Status Register command, because this command is interpreted as data to program at WA_0.

11.3.3 Program

After setup completion, the host programming system must check SR[0] to determine the *data-stream ready* status (SR[0]=0). Each subsequent write after this check is a program-data write to the flash memory array. Each cell within the memory word to be programmed to 0 receives one WSM pulse; additional pulses, if required, occur in the verify phase.

SR[0]=1 indicates that the WSM is busy applying the program pulse.

The host programmer must poll the flash device status register for the *program done* state after each data-stream write.

SR[0]=0 indicates that the appropriate cell(s) within the accessed memory location have received their single WSM program pulse, and that the flash device is ready for the next word.

Although the host can check full status for errors at any time, this check is necessary only on a block basis, after EFP exit.

Addresses must remain within the target block. Supplying an address outside of the target block immediately terminates the program phase; the WSM then enters the EFP verify phase.

The address can either remain constant or increment. The flash device compares the incoming address to the address stored from the setup phase (WA_0).

- If the addresses match, the WSM programs the new data word at the next sequential memory location.
- If the addresses differ, the WSM jumps to the new address location.

The program phase concludes when the host programming system writes to a different block address. The data supplied must be FFFFh. Upon program phase completion, the flash device enters the EFP verify phase.

11.3.4 Verify

A high percentage of the flash memory bits program on the first WSM pulse. However, EFP internal verification identifies cells that do not completely program on their first attempt, and applies additional pulses as required.

The verify phase is identical in flow to the program phase, except that instead of programming incoming data, the WSM compares the verify-stream data to the data that was previously programmed into the block.

- If the data compares correctly, the host programmer proceeds to the next word.
- If the data does not match, the host waits while the WSM applies one or more additional pulses.

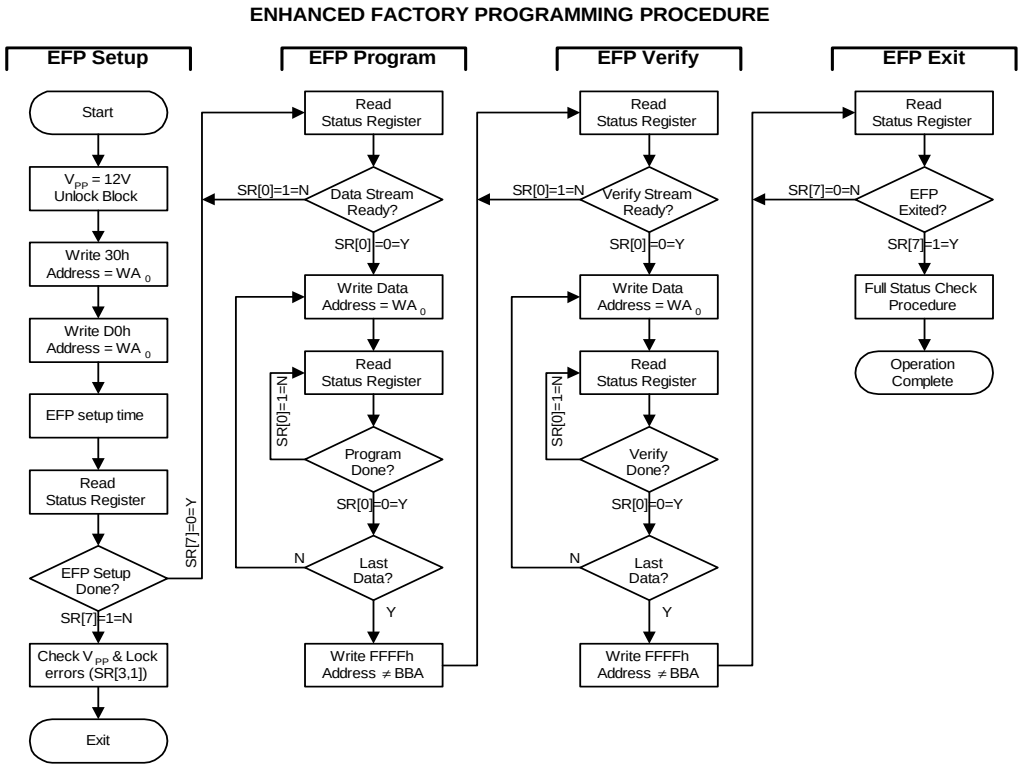
The host programmer must reset its initial verify-word address to the same starting location supplied during the program phase. It then reissues each data word in the same order as during the program phase. Like programming, the host can write each subsequent data word to WA_0 or it can increment through the block addresses.

The verification phase concludes when the interfacing programmer writes to a different block address. The data supplied must be FFFFh. Upon completion of the verify phase, the flash device enters the EFP exit phase.

11.3.5 Exit

SR[7]=1 indicates that the flash device has returned to normal operating conditions. Perform a full status check at this time, to verify that the entire block programmed successfully. After EFP exit, any valid CUI command can be issued.

Figure 29. Enhanced Factory Program Flowchart



EFP Setup		
Bus State		**Comments**
Write	Unlock Block	V_{PP} = 12V Unlock block
Write	EFP Setup	Data = 30h Address = WA_0
Write	EFP Confirm	Data = D0h Address = WA_0
Standby		EFP setup time
Read		Status Register
Standby	EFP Setup Done?	Check SR[7] 0 = EFP ready 1 = EFP not ready
Standby	Error Condition Check	If SR[7] = 1: Check SR[3,1] SR[3] = 1 = V_{PP} error SR[1] = 1 = locked block

EFP Program		
Bus State		**Comments**
Read		Status Register
Standby	Data Stream Ready?	Check SR[0] 0 = Ready for data 1 = Not ready for data
Write (note 1)		Data = Data to program Address = WA_0
Read		Status Register
Standby	Program Done?	Check SR[0] 0 = Program done 1 = Program not done
Standby	Last Data?	Device automatically increments address.
Write	Exit Program Phase	Data = FFFFh Address not within same BBA

EFP Verify		
Bus State		**Comments**
Read		Status Register
Standby	Verify Stream Ready?	Check SR[0] 0 = Ready for verify 1 = Not ready for verify
Write (note 2)		Data = Word to verify Address = WA_0
Read		Status Register
Standby (note 3)	Verify Done?	Check SR[0] 0 = Verify done 1 = Verify not done
Standby	Last Data?	Device automatically increments address.
Write	Exit Verify Phase	Data = FFFFh Address not within same BBA

EFP Exit		
Read		Status Register
Standby	EFP Exited?	Check SR[7] 0 = Exit not finished 1 = Exit completed

Repeat for subsequent operations.

After EFP exit, a Full Status Check can determine if any program error occurred.

See the Full Status Check procedure in the Word Program flowchart.

1. WA_0 = first Word Address to be programmed within the target block. The BBA (Block Base Address) must remain constant throughout the program phase data stream; WA can be held constant at the first address location, or it can be written to sequence up through the addresses within the block. Writing to a BBA not equal to that of the block currently being written to terminates the EFP program phase, and instructs the device to enter the EFP verify phase.
2. For proper verification to occur , the verify data stream must be presented to the device in the same sequence as that of the program phase data stream. Writing to a BBA not equal to WA terminates the EFP verify phase, and instructs the device to exit EFP .
3. Bits that did not fully program with the single WSM pulse of the EFP program phase receive additional program-pulse attempts during the EFP verify phase. The device will report any program failure by setting SR[4]=1; this check can be performed during the full status check after EFP has been exited for that block, and will indicate any error within the entire data stream.

12.0 Program and Erase Operations

12.1 Program/Erase Suspend and Resume

The Program Suspend and Erase Suspend commands halt an in-progress program or erase operation. The command can be issued at any flash device address. The partition corresponding to the address of the command remains in its previous state. A suspend command allows data to be accessed from memory locations other than the location being programmed or the block being erased.

- A program operation can be suspended only to perform a read operation.
- An erase operation can be suspended to perform either a program or a read operation within any block, except the block that is erase suspended.
- A program command nested within a suspended erase can subsequently be suspended to read yet another location.

Once a program or erase process starts, the Suspend command requests that the WSM suspends the program or erase sequence at predetermined points in the algorithm. The partition that is actually suspended continues to output status register data after the Suspend command is written. An operation is suspended when status bits SR[7] and SR[6] and/or SR[2] are set.

To read data from blocks within the partition (other than an erase-suspended block), write a Read Array command. Block erase cannot resume until the program operations initiated during erase suspend are complete.

- Read Array, Read Status Register, Read Identifier (ID), Read Query, and Program Resume are valid commands during Program or Erase Suspend.
- Additionally, Clear Status Register, Program, Program Suspend, Erase Resume, Lock Block, Unlock Block, and Lock-Down Block are valid commands during erase suspend.

To read data from a block in a partition that is not programming or erasing, the operation does not need to be suspended.

- If the other partition is already in read array, ID, or Query mode, issuing a valid address returns corresponding data.
- If the other partition is not in a read mode, one of the read commands must be issued to the partition before data can be read.

During a suspend, CE# = V_{IH} places the flash device in standby state, which reduces active current. V_{PP} must remain at its program level and WP# must remain unchanged while in suspend mode.

A resume command instructs the WSM to continue programming or erasing, and clears status register bits SR[2] (or SR[6]) and SR[7]. The Resume command can be written to any partition. When read at the partition that is programming or erasing, the flash device outputs data corresponding to the last mode for that partition. If the status register error bits are set, the status register can be cleared before issuing the next instruction. RST# must remain at V_{IH}. See Figure 30, “Program Suspend / Resume Flowchart” on page 68, and Figure 31, “Erase Suspend / Resume Flowchart” on page 69.

If a suspended partition was placed in Read Array, Read Status Register, Read Identifier (ID), or Read Query during the suspend, the flash device remains in that mode, and outputs data corresponding to that mode after the program or erase operation resumes.

After resuming a suspended operation, issue the read command appropriate to the read operation. To read status after resuming a suspended operation, issue a Read Status Register command (70h) to return the suspended partition to status mode.

Figure 30. Program Suspend / Resume Flowchart

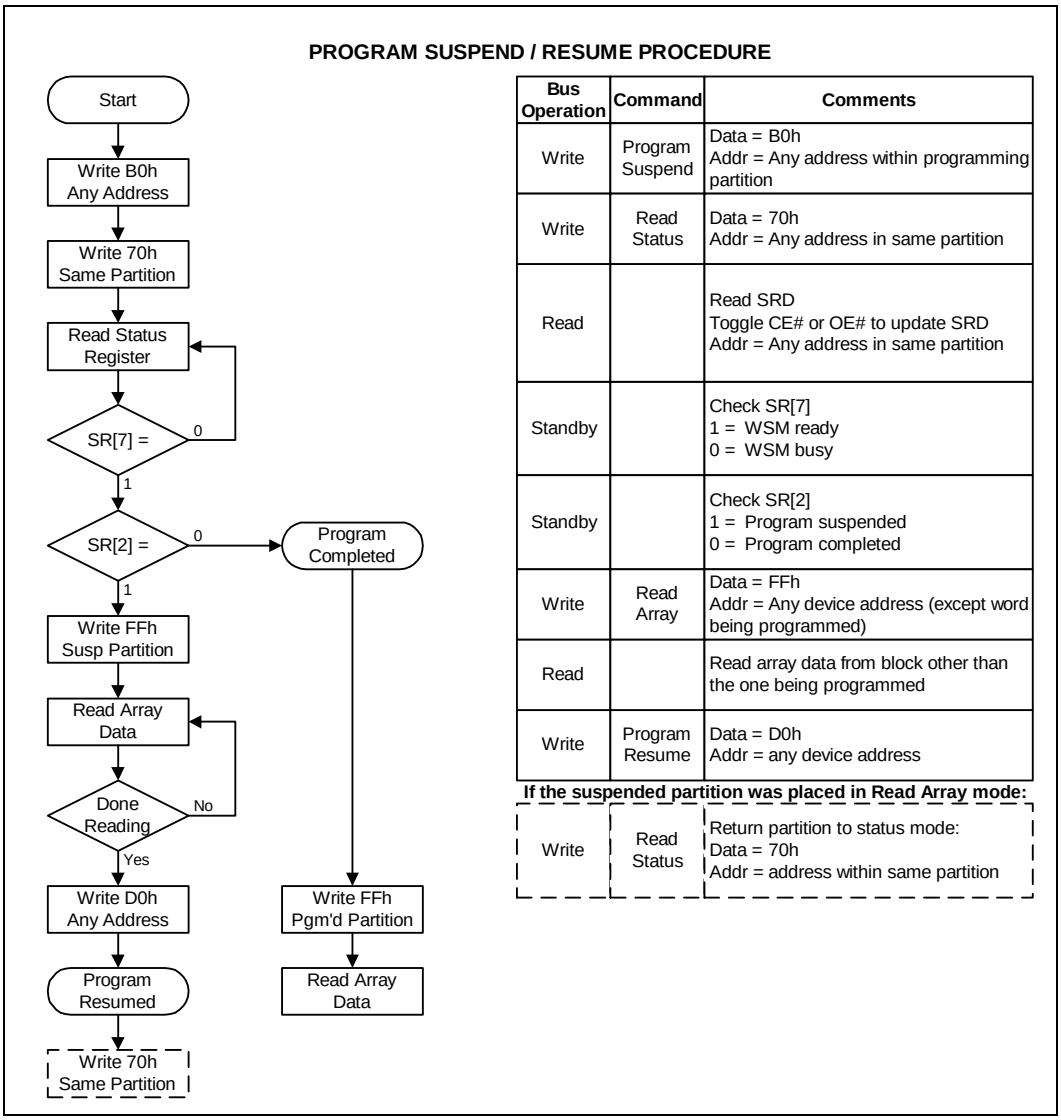
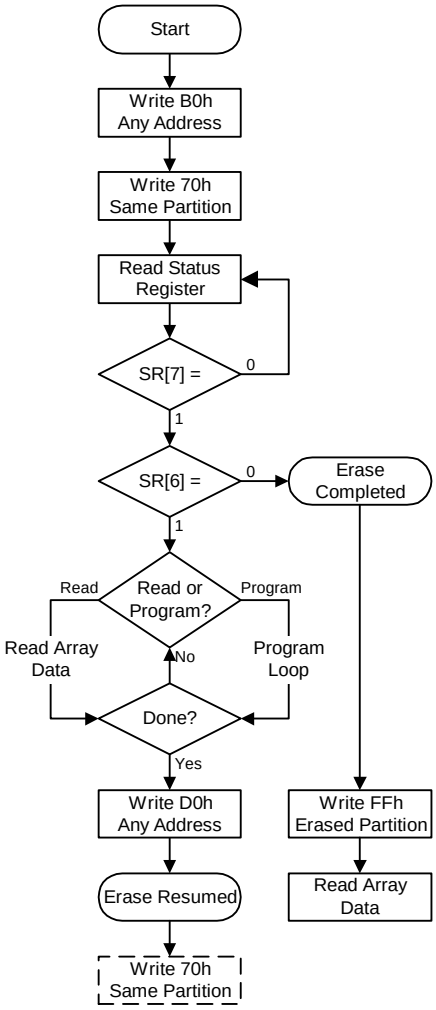


Figure 31. Erase Suspend / Resume Flowchart



Bus Operation	Command	Comments
Write	Erase Suspend	Data = B0h Addr = Any address
Write	Read Status	Data = 70h Addr = Any address in same partition
Read		Read SRD Toggle CE# or OE# to update SRD Addr = Any address in same partition
Standby		Check SR[7] 1 = WSM ready 0 = WSM busy
Standby		Check SR[6] 1 = Erase suspended 0 = Erase completed
Write	Read Array or Program	Data = FFh or 40h Addr = Any device address (except block being erased)
Read or Write		Read array or program data from/to block other than the one being erased
Write	Erase Resume	Data = D0h Addr = Any address

If the suspended partition was placed in Read Array mode or a Program Loop:

Write	Read Status	Return partition to status mode: Data = 70h Addr = Address within same partition

12.2 Block Erase

The 2-cycle block erase command sequence, consisting of Erase Setup (20h) and Erase Confirm (D0h), initiates one block erase at the addressed block. Only one partition can be in an erase mode at a time; other partitions must be in a read mode. The Erase Confirm command internally latches the address of the block to erase. Erase forces all bits within the block to 1.

SR[7] is cleared while the erase executes.

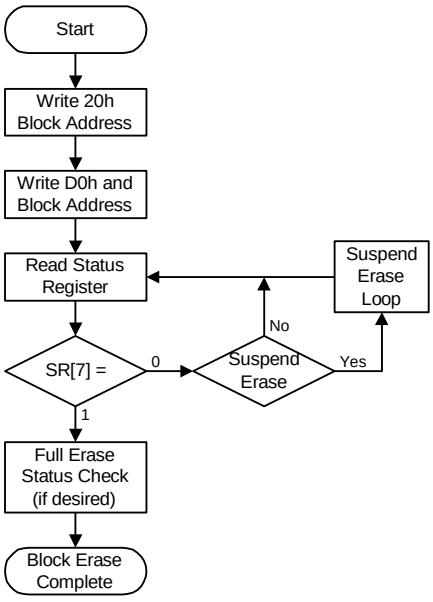
After writing the Erase Confirm command, the selected partition is placed in read status register mode. Reads performed to that partition return the current status data. The address given during the Erase Confirm command does not need to be the same address used in the Erase Setup command. For example, if the Erase Confirm command is given to partition B, then the selected block in partition B is erased, even if the Erase Setup command was to partition A.

The 2-cycle erase sequence cannot be interrupted with a bus write operation. For example, to execute properly, an Erase Setup command must be immediately followed by the Erase Confirm command. If a different command is issued between the setup and confirm commands, the following occurs:

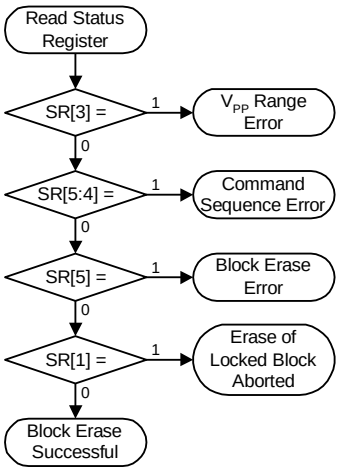
- The partition is placed in read-status mode.
- The status register signals a command sequence error.
- All subsequent erase commands to that partition are ignored until the status register is cleared.

To detect block erase completion, the CPU analyzes SR[7] of that partition. If an error bit (SR[5,3,1]) was flagged, the status register can be cleared by issuing the Clear Status Register command before attempting the next operation. The partition remains in read-status mode until another command is written to its CUI. Any CUI instruction can follow after erasing completes. The CUI can be set to read-array mode to prevent inadvertent status register reads.

Figure 32. Block Erase Flowchart



Bus Operation	Command	Comments
Write	Block Erase Setup	Data = 20h Addr = Block to be erased (BA)
Write	Erase Confirm	Data = D0h Addr = Block to be erased (BA)
Read		Read SRD Toggle CE# or OE# to update SRD
Standby		Check SR[7] 1 = WSM ready 0 = WSM busy
Repeat for subsequent block erasures. Full status register check can be done after each block erase or after a sequence of block erasures.		



Bus Operation	Command	Comments
Standby		Check SR[3] 1 = V_{PP} error
Standby		Check SR[5:4] Both 1 = Command sequence error
Standby		Check SR[5] 1 = Block erase error
Standby		Check SR[1] 1 = Attempted erase of locked block Erase aborted
SR[3,1] **must** be cleared before the WSM will allow further erase attempts. Only the Clear Status Register command clears SR[5:3,1]. If an error is detected, clear the Status register before attempting an erase retry or other error recovery.		

12.3 Read-While-Write and Read-While-Erase

The Intel® Wireless Flash Memory (W30) supports flexible multi-partition dual-operation architecture. By dividing the flash memory into many separate partitions, the flash device can read from one partition while programing (Read-While-Write) or erasing (Read-While-Eras) in another partition. Both of these features greatly enhance data storage performance.

The W30 flash memory device does not support simultaneous program and erase operations. Attempting to perform operations such as these results in a command sequence error. Only one partition can be programming or erasing while another partition is reading. However, one partition can be in erase suspend mode while a second partition is performing a program operation, and yet another partition is executing a read command. Table 18, “Command Codes and Descriptions” on page 53 describes the command codes available for all functions.

13.0 Security Modes

The W30 flash memory device offers both hardware and software security features to protect the flash memory data.

- To use the software security feature, execute the Lock Block command.
- To use the hardware security feature, execute the Lock-Down Block command *and* assert the WP# signal.

Refer to Figure 33, "Block Locking State Diagram" on page 74 for a state diagram of the flash device security features. Also see Figure 34, "Locking Operations Flowchart" on page 77.

13.1 Block Lock Operations

Individual instant block locking protects code and data by allowing any block to be locked or unlocked with no latency. This locking scheme offers two levels of protection:

- Software-only control of block locking (useful for frequently changed data blocks).
- Hardware interaction before locking can be changed (protects infrequently changed code blocks).

The following sections discuss the locking system operation. The term *state [abc]* specifies locking states, such as state [001]. In this syntax:

- a = WP# value.
- b = block lock-down status bit D1.
- c = Block Lock status register bit D0.

Figure 33, "Block Locking State Diagram" on page 74 defines possible locking states.

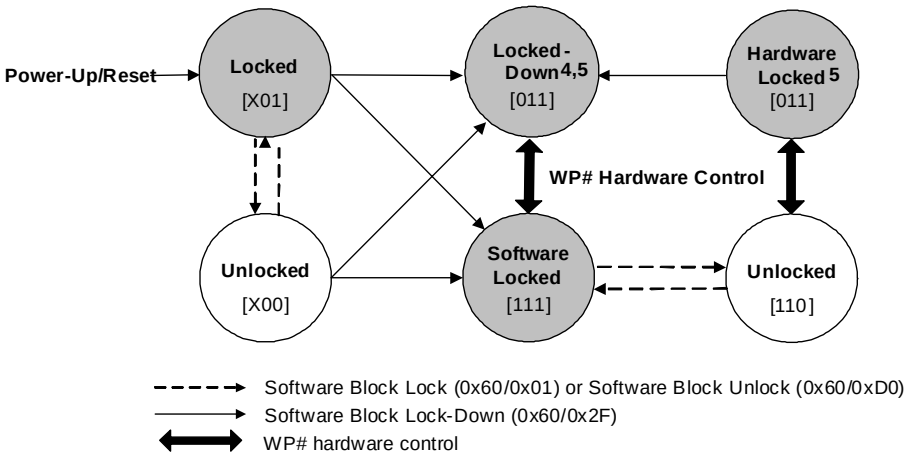
The following summarizes the locking functionality.

- All blocks power-up in a locked state.
- Unlock commands can unlock these blocks, and lock commands can lock them again.
- The Lock-Down command locks a block and prevents it from being unlocked when WP# is asserted.
  - Locked-down blocks can be unlocked or locked with commands as long as WP# is deasserted.
  - When WP# is asserted, previously locked-down blocks return to lock-down.
  - The lock-down status bit clears only when the flash device is reset or powered-down.

Block lock registers are not affected by the V_{PP} level. These registers can be modified and read even if $V_{PP} \leq V_{PPLK}$.

The locking status of each block can be set to locked, unlocked, and lock-down, as described in the following sections. See Figure 34, "Locking Operations Flowchart" on page 77.

Figure 33. Block Locking State Diagram



Notes:
1. [a,b,c] represents [WP#, D1, D0]. X = Don't Care.
2. D1 indicates block Lock-down status.
   - D1 = 0, Lock-down has not been issued to this block.
   - D1 = 1, Lock-down has been issued to this block.
3. D0 indicates block lock status.
   - D0 = 0, block is unlocked.
   - D0 = 1, block is locked.
4. Locked-down = Hardware + Software locked.
5. [011] states should be tracked by system software to determine difference between Hardware Locked and Locked-Down states.

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13.1.1 Lock

All blocks default to locked (state [x01]) after initial power-up or reset. Locked blocks are fully protected from alteration. Attempted program or erase operations to a locked block return an error in SR[1].

- To lock unlocked blocks, use the Lock Block command sequence.
- To change the status of a locked block to unlocked or lock-down, use the appropriate software commands.

13.1.2 Unlock

Unlocked blocks (states [x00] and [110]) can be programmed or erased. All unlocked blocks return to the locked state when the flash device is reset or powered-down.

- To change the status of an unlocked block to the locked or locked-down state, use the appropriate software commands.
- To unlock a locked block, write the Unlock Block command sequence if the block is not locked-down.

13.1.3 Lock-Down

Locked-down blocks (state [011]) offer an additional level of write protection beyond the protection of a regular locked block. If a block is locked-down, the software cannot change the state of the block if WP# is asserted.

- To lock-down a locked or unlocked block, write the Lock-Down Block command sequence.
- If a block was set to locked-down, then later changed to unlocked, issue the Lock-down command before asserting WP#, to put that block back in the locked-down state.
- When WP# is deasserted, locked-down blocks change to the locked state, and can then be unlocked using the Unlock Block command.

13.1.4 Block Lock Status

The lock status of every block can be read in read identifier mode.

Note: To enter this mode, issue the Read Identifier command to the flash device.

Subsequent reads at BBA + 02h output the lock status of that block. For example, to read the block lock status of block 10, the address sent to the flash device must be 50002h (for a top-parameter device).

The lowest two data bits of the read data, DQ1 and DQ0, represent the lock status.

- DQ0 indicates the block lock status. This bit is set using the Lock Block command and cleared using the Block Unlock command. It is also set when entering the lock-down state.
- DQ1 indicates lock-down status and is set using the Lock-Down command.

The lock-down status bit cannot be cleared by software–only by a flash device reset or power-down. See Table 25.

Table 25. Write Protection Truth Table

VPP	WP#	RST#	Write Protection
X	X	V_{IL}	Device is inaccessible
V_{IL}	X	V_{IH}	Word program and block erase are prohibited
X	V_{IL}	V_{IH}	All lock-down blocks are locked
X	V_{IH}	V_{IH}	All lock-down blocks can be unlocked

13.1.5 Lock During Erase Suspend

Block lock configurations can be performed during an erase suspend operation, using the standard locking command sequences to unlock, lock, or lock-down a block. This feature is useful when another block requires immediate updating.

To change block locking during an erase operation:

1. Write the Erase Suspend command.
2. Check SR[6] to determine that the erase operation has suspended.
3. Write the desired lock command sequence to a block.
   The lock status changes.
4. After completing lock, unlock, read, or program operations, resume the erase operation with the Erase Resume command (D0h).

If a block is locked or locked-down during a suspended erase of the same block, the locking status bits change immediately. When the erase operation resumes, it completes normally.

Locking operations cannot occur during program suspend. Appendix A, “Write State Machine” on page 90 shows valid commands during erase suspend.

13.1.6 Status Register Error Checking

Using nested locking or program command sequences during erase suspend can introduce ambiguity into status register results.

Because locking changes require 2-cycle command sequences—for example, 60h followed by 01h to lock a block—following the Configuration Setup command (60h) with an invalid command produces a command sequence error (SR[5:4]=11b).

If a Lock Block command error occurs during erase suspend, the flash device sets SR[4] and SR[5] to 1 even after the erase resumes. When erase is complete, possible errors during the erase cannot be detected from the status register, because of the previous locking command error. A similar situation occurs if a program operation error is nested within an erase suspend.

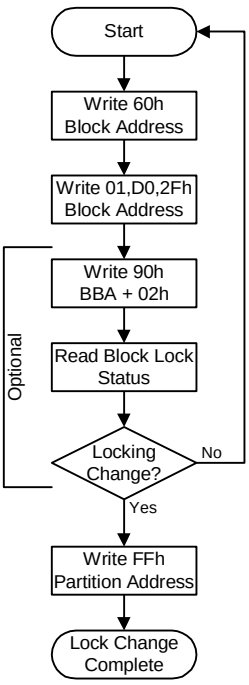
13.1.7 WP# Lock-Down Control

The Write Protect signal, WP#, adds an additional layer of block security. WP# affects only blocks that previously had the Lock-Down command written to them.

- After the lock-down status bit is set for a block, asserting WP# forces that block into the lock-down state [011] and prevents it from being unlocked.
- After WP# is deasserted, the state of the block reverts to locked [111]. Software commands can then unlock the block (for erase or program operations) and subsequently re-lock it.

Only flash device reset or power-down can clear the lock-down status bit and render WP# ineffective.

Figure 34. Locking Operations Flowchart



Bus Operation	Command	Comments
Write	Lock Setup	Data = 60h Addr = Block to lock/unlock/lock-down (BA)
Write	Lock, Unlock, or Lockdown Confirm	Data = 01h (Lock block) D0h (Unlock block) 2Fh (Lockdown block) Addr = Block to lock/unlock/lock-down (BA)
Write (Optional)	Read ID Plane	Data = 90h Addr = BBA + 02h
Read (Optional)	Block Lock Status	Block Lock status data Addr = BBA + 02h
Standby (Optional)		Confirm locking change on DQ[1:0]. (See Block Locking State Transitions Table for valid combinations.)
Write	Read Array	Data = FFh Addr = Any address in same partition

13.2 Protection Register

The W30 flash memory device includes a 128-bit Protection Register. This protection register is used to increase system security and for identification purposes. The protection register value can match the flash device to the system CPU or ASIC to prevent flash device substitution.

- The lower 64 bits within the protection register are programmed by Intel with a unique number in each flash device.
- The upper 64 OTP bits within the protection register are left for the customer to program. Once programmed, the customer segment can be locked to prevent further programming.

Note: The individual bits of the user segment of the protection register are OTP, not the register in total. The user can program each OTP bit individually, one at a time, if desired. However, after the protection register is locked, the entire user segment is locked and no more user bits can be programmed.

The protection register shares some of the same internal flash device resources as the parameter partition. Therefore, RWW is allowed only between the protection register and the main partitions. Table 26 describes the operations allowed in the protection register, parameter partition, and main partition during RWW and RWE.

Table 26. Simultaneous Operations Allowed with the Protection Register

Protection Register	Parameter Partition Array Data	Main Partitions	Description
Read	See Description	Write/Erase	While programming or erasing in a main partition, the protection register can be read from any other partition. Reading the parameter partition data is not allowed if the protection register is being read from addresses within the parameter partition.
See Description	Read	Write/Erase	While programming or erasing in a main partition, read operations are allowed in the parameter partition. Accessing the protection registers from parameter partition addresses is not allowed.
Read	Read	Write/Erase	While programming or erasing in a main partition, read operations are allowed in the parameter partition. Accessing the protection registers is allowed, but only in a partition that is *different* from the partition being programmed or erased, and also *different* from the parameter partition.
Write	No Access Allowed	Read	While programming the protection register, reads are allowed only in the other main partitions. Access to the parameter partition is not allowed, because programming of the protection register can occur only in the parameter partition, so that the parameter partition exists in status mode.
No Access Allowed	Write/Erase	Read	While programming or erasing the parameter partition, reads of the protection registers are not allowed in *any* partition. Reads in other main partitions are supported.

13.2.1 Reading the Protection Register

Writing the Read Identifier command allows the protection register data to be read 16 bits at a time from addresses shown in Table 20, “Flash Device Identification Codes” on page 57. The protection register is read from the Read Identifier command, and can be read in any partition.Writing the Read Array command returns the flash device to read-array mode.

13.2.2 Programing the Protection Register

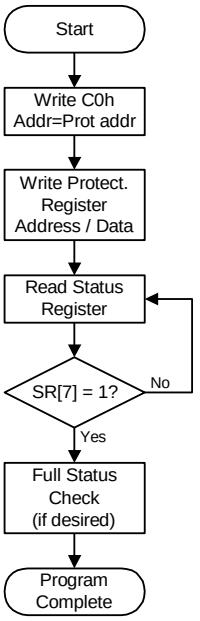
Issue the Protection Program command only at the parameter partition followed by the data to be programmed at the specified location. This command programs the upper 64 bits of the protection register 16 bits at a time. Table 20, “Flash Device Identification Codes” on page 57 shows allowable addresses. See also Figure 35, “Protection Register Programming Flowchart” on page 79. Issuing a Protection Program command outside the address space of the register results in a status register error (SR[4]=1).

13.2.3 Locking the Protection Register

- PR-LK.0 is programmed to 0 by Intel to protect the unique flash device number.
- PR-LK.1 can be programmed by the user to lock the user portion (upper 64 bits) of the protection register (See Figure 36, “Protection Register Locking). This bit is set using the Protection Program command to program a value of FFFDh into PR-LK.

After PR-LK register bits are programmed (locked), the stored values in the protection register cannot be changed. Protection Program commands written to a locked section result in a status register error (SR[4]=1, SR[5]=1).

Figure 35. Protection Register Programming Flowchart



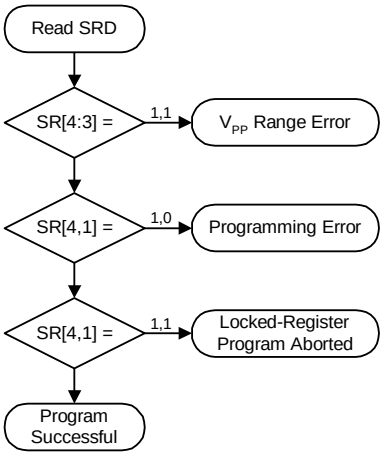
PROTECTION REGISTER PROGRAMMINGPROCEDURE

Bus Operation	Command	Comments
Write	Protection Program Setup	Data = C0h Addr = Protection address
Write	Protection Program	Data = Data to program Addr = Protection address
Read		Read SRD Toggle CE# or OE# to update SRD
Standby		Check SR[7] 1 = WSM Ready 0 = WSM Busy

Protection Program operations addresses must be within the protection register address space. Addresses outside this space will return an error.

Repeat for subsequent programming operations.

Full status register check can be done after each program or after a sequence of program operations.



FULL STATUS CHECK PROCEDURE

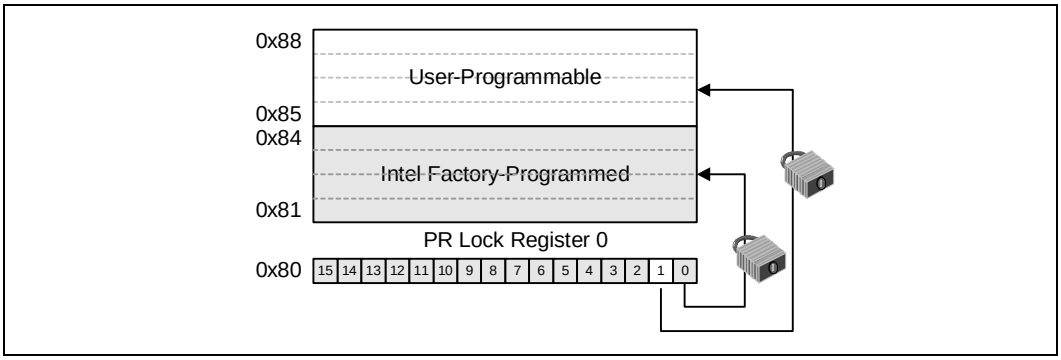
Bus Operation	Command	Comments
Standby		SR[1] SR[3] SR[4] 0 1 1 V_{PP} Error
Standby		0 0 1 Protection register program error
Standby		1 0 1 Register locked; Operation aborted

SR[3] MUST be cleared before the WSM will allow further program attempts.

Only the Clear Staus Register command clears SR[4:3,1].

If an error is detected, clear the status register before attempting a program retry or other error recovery.

Figure 36. Protection Register Locking

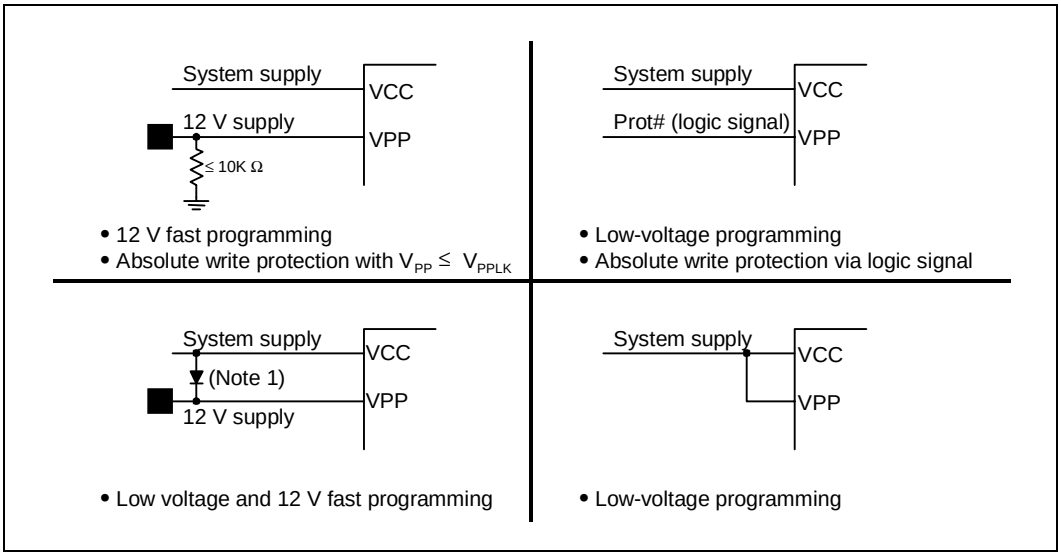


13.3 VPP Protection

The Intel® Wireless Flash Memory (W30) provides in-system program and erase at V_{PPL}. For factory programming, the W30 flash memory device also includes a low-cost, backward-compatible 12 V programming feature.(See "Factory Programming" on page 63.) The EFP feature can also be used to greatly improve factory program performance, as explained in Section 11.3, "Enhanced Factory Program (EFP)" on page 63.

In addition to flexible block locking, holding the V_{PP} programming voltage low can provide hardware write protection of all flash-device blocks. If V_{PP} is below V_{PPLK}, program or erase operations result in an error displayed in SR[3]. (See Figure 37.)

Figure 37. Examples of VPP Power Supply Configurations



Note: If the V_{CC} supply can sink adequate current, you can use an appropriately valued resistor.

14.0 Set Read Configuration Register

The Set Read Configuration Register (RCR) command sets the burst order, frequency configuration, burst length, and other parameters.

A two-bus cycle command sequence initiates this operation. The read configuration register data is placed on the lower 16 bits of the address bus (A[15:0]) during both bus cycles.

1. The Set Read Configuration Register command is written, along with the configuration data (on the address bus).
2. A second write confirms the operation and again presents the read configuration register data on the address bus.
3. The read configuration register data is latched on the rising edge of ADV#, CE#, or WE# (whichever occurs first).

This command functions independently of the applied V_{PP} voltage. After executing this command, the flash device returns to read-array mode.

To examine the contents of the read configuration register, write the Read Identifier command and then read location 05h. (See Table 27 and Table 28.)

Table 27. Read Configuration Register Definitions

Read Mode	Res'd	First Access Latency Count			WAIT Polarity	Data Output Config	WAIT Config	Burst Seq	Clock Config	Res'd	Res'd	Burst Wrap	Burst Length		
RM	R	LC2	LC1	LC0	WP	DOC	WC	BS	CC	R	R	BW	BL2	BL1	BL0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 28. Read Configuration Register Descriptions

Bit	Name	Description[1]	Notes
15	**RM** Read Mode	0 = Synchronous Burst Reads Enabled 1 = Asynchronous Reads Enabled (Default)	2,6
14	**R**	Reserved	5
13-11	**LC[2:0]** First Access Latency Count	001 = Reserved 010 = Code 2 011 = Code 3 100 = Code 4 101 = Code 5 111 = Reserved (Default)	6
10	**WP** WAIT Signal Polarity	0 = WAIT signal is asserted low 1 = WAIT signal is asserted high (Default)	3
9	**DOC** Data Output Configuration	0 = Hold Data for One Clock 1 = Hold Data for Two Clock (Default)	6
8	**WC** WAIT Configuration	0 = WAIT Asserted During Delay 1 = WAIT Asserted One Data Cycle before Delay (Default)	6
7	**BS** Burst Sequence	1 = Linear Burst Order (Default)	
6	**CC** Clock Configuration	0 = Burst Starts and Data Output on Falling Clock Edge 1 = Burst Starts and Data Output on Rising Clock Edge (Default)	
5	**R**	Reserved	5
4	**R**	Reserved	5
3	**BW** Burst Wrap	0 = Wrap bursts within burst length set by CR[2:0] 1 = Don't wrap accesses within burst length set by CR[2:0].(Default)	
2-0	**BL[2:0]** Burst Length	001 = 4-Word Burst 010 = 8-Word Burst 011 = 16-Word Burst (Available on the 130 nm lithography) 111 = Continuous Burst (Default)	4

Notes:

1. Undocumented combinations of bits are reserved by Intel for future implementations.
2. Synchronous and page read mode configurations affect reads from main blocks and parameter blocks. Status Register and configuration reads support single read cycles. RCR[15]=1 disables the configuration set by RCR[14:0].
3. Data is not ready when WAIT is asserted.
4. Set the synchronous burst length. In asynchronous page mode, the burst length equals four words.
5. Set all reserved Read Configuration Register bits to zero.
6. Setting the Read Configuration Register for synchronous burst-mode with a latency count of 2 (RCR[13:11] = 010), data hold for 2 clocks (RCR[9] = 1), and WAIT asserted one data cycle before delay (RCR[8] =1) is not supported.

14.1 Read Mode (RCR[15])

All partitions support two high-performance read configurations:

- synchronous burst mode
- asynchronous page mode (default)

RCR[15] sets the read configuration to one of these modes.

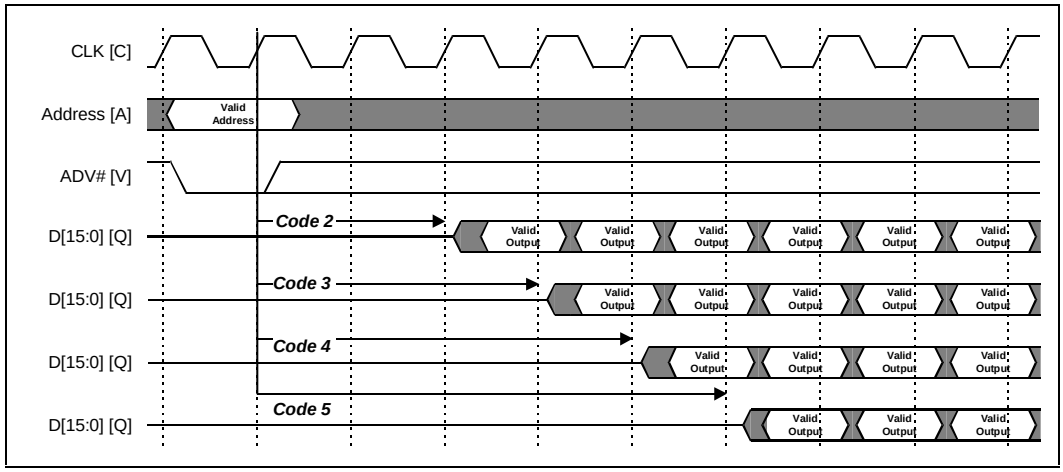
Status register, query, and identifier modes support only asynchronous and single-synchronous read operations.

14.2 First Access Latency Count (RCR[13:11])

The First Access Latency Count (RCR[13:11]) configuration tells the flash device how many clocks must elapse from ADV# de-assertion (V_{IH}) before driving the first data word onto its data pins. The input clock frequency determines this value. See Table 27, "Read Configuration Register Definitions" on page 81 for latency values.

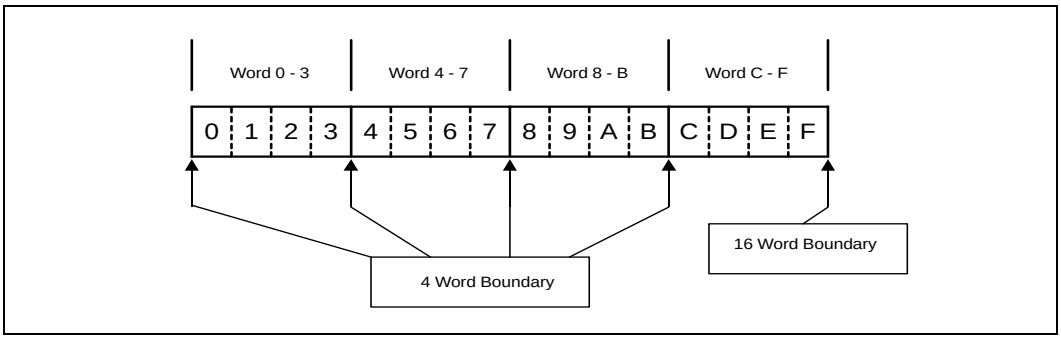
Figure 38 shows data output latency from ADV# assertion for different latencies. Refer to Section 14.2.1, "Latency Count Settings" on page 84 for Latency Code Settings.

Figure 38. First Access Latency Configuration



Note: Other First Access Latency Configuration settings are reserved.

Figure 39. Word Boundary



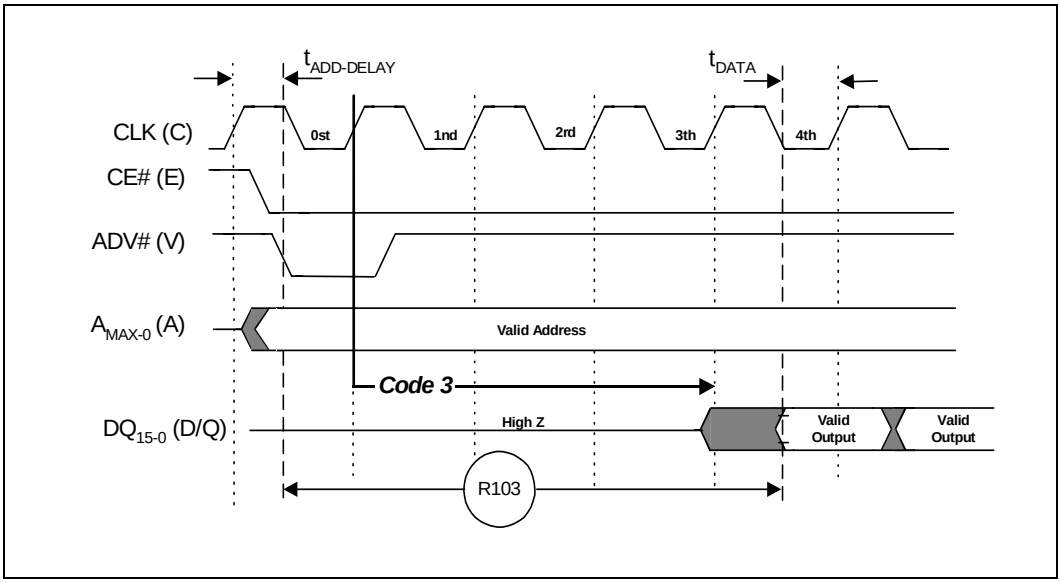
Note: The 16-word boundary is the end of the flash device sense word-line.

14.2.1 Latency Count Settings

Table 29. Latency Count Settings

	t_{AVQV}/t_{CHQV} (85ns/22ns)		t_{AVQV}/t_{CHQV} (70ns/20ns)	t_{AVQV}/t_{CHQV} (90ns/22ns)		Unit
Latency Count Settings	2	3, 4, 5	2, 3, 4, 5	2	3, 4, 5	
Frequency	≤ 31	≤ 33	≤ 40	≤ 29	≤ 33	MHz

Figure 40. Data Output with LC Setting at Code 3



14.3 WAIT Signal Polarity (RCR[10])

- If the WT bit is cleared (RCR[10]=0), then WAIT is configured to be asserted low. A 0 on the WAIT signal indicates that data is not ready and the data bus contains invalid data.
- Conversely, if RCR[10] is set, then WAIT is asserted high.

In either case, if WAIT is deasserted, then data is ready and valid. WAIT is asserted during asynchronous page mode reads.

14.4 WAIT Signal Function

The WAIT signal indicates data valid when the flash device is operating in synchronous mode (RCR[15]=0), and when addressing a partition that is currently in read-array mode. The WAIT signal is deasserted only when data is valid on the bus.

- When the flash device is operating in synchronous non-read-array mode, such as read status, read ID, or read query, WAIT is set to an asserted state, as determined by RCR[10]. See Figure 14, “WAIT Signal in Synchronous Non-Read Array Operation Waveform” on page 38.
- When the flash device is operating in asynchronous page mode or asynchronous single word read mode, WAIT is set to an asserted state, as determined by RCR[10]. See Figure 10, “Page-Mode Read Operation Waveform” on page 34, and Figure 8, “Asynchronous Read Operation Waveform” on page 32.

From a system perspective, the WAIT signal is in the asserted state (based on RCR[10]) when the flash device is operating in synchronous non-read-array mode (such as Read ID, Read Query, or Read Status), or if the flash device is operating in asynchronous mode (RCR[15]=1). In these cases, the system software must ignore (mask) the WAIT signal, because WAIT does not convey any useful information about the validity of what is appearing on the data bus.

CONDITION	WAIT
CE# = V_{IH} CE# = V_{IL}	Tri-State Active
OE#	No-Effect
Synchronous Array Read	Active
Synchronous Non-Array Read	Asserted
All Asynchronous Read and all Write	Asserted

14.5 Data Hold (RCR[9])

The Data Output Configuration (DOC) bit (RCR[9]) determines whether a data word remains valid on the data bus for one or two clock cycles. The minimum data set-up time on the processor, and the flash memory clock-to-data output delay, determine whether one or two clocks are needed.

- A DOC set at 1-clock data hold corresponds to a 1-clock data cycle.
- A DOC set at 2-clock data hold corresponds to a 2-clock data cycle.

The setting of this configuration bit depends on the system and CPU characteristics. For clarification, see Figure 41. The following is a method for determining this configuration setting.

To set the flash device at 1-clock data hold for subsequent reads, the following condition must be satisfied:

$$t_{CHQV\ (ns)} + t_{DATA}\ (ns) \leq \text{One CLK Period (ns)}$$

As an example, use a clock frequency of 54 MHz and a clock period of 25 ns. Assume the data output hold time is one clock. Apply this data to the formula above for the subsequent reads:

$$20\ ns + 4\ ns \leq 25\ ns$$

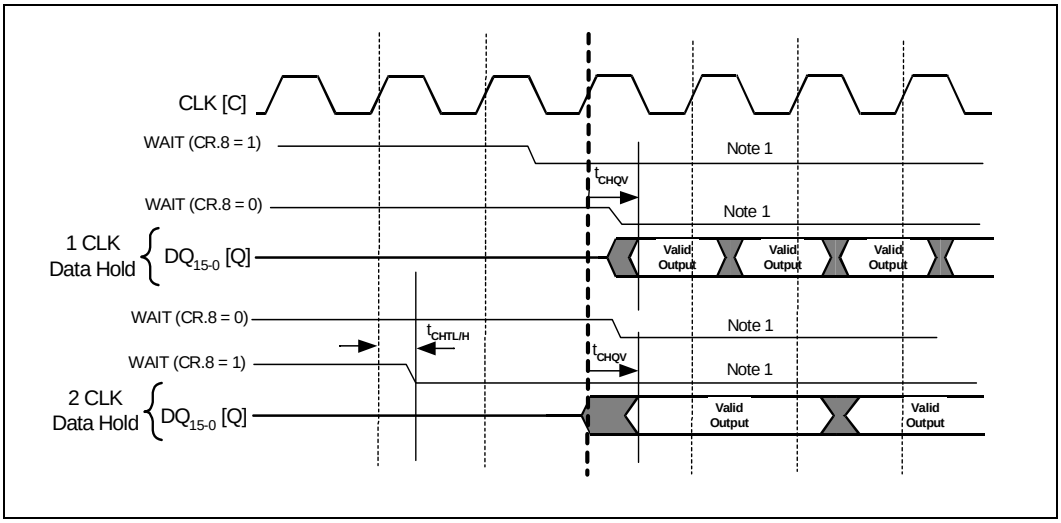
This equation is satisfied, and data output is available and valid at every clock period. If t_{DATA} is long, hold for two cycles. During page-mode reads, the initial access time can be determined using the formula:

$$t_{ADD\text{-}DELAY\ (ns)} t_{DATA}\ (ns) + t_{AVQV}\ (ns)$$

Subsequent reads in page mode are defined by:

$$t_{APA\ (ns)} + t_{DATA}\ (ns) \qquad \text{(minimum time)}$$

Figure 41. Data Output Configuration with WAIT Signal Delay



Note: WAIT shown asserted high (RCR[10]=1).

14.6 WAIT Delay (RCR[8])

The WAIT configuration bit (RCR[8]) controls WAIT signal delay behavior for all synchronous read-array modes. This bit setting depends on the system and CPU characteristics. The WAIT can be asserted either *during*, or one data cycle *before*, a valid output.

In synchronous linear read array (no-wrap mode RCR[3]=1) of 4-word, 8-word, 16-word, or continuous-word burst mode, an output delay might occur when a burst sequence crosses its first flash device-row boundary (16-word boundary).

- If the burst start address is 4-word boundary aligned, the delay does not occur.
- If the start address is misaligned to a 4-word boundary, the delay occurs once per burst-mode read sequence. The WAIT signal informs the system of this delay.

14.7 Burst Sequence (RCR[7])

The burst sequence specifies the synchronous-burst mode data order (see Table 30, “Sequence and Burst Length” on page 88). When operating in a linear burst mode, either 4-word, 8-word, or 16-word burst length with the burst wrap bit (RCR[3]) set, or in continuous burst mode, the flash device might incur an output delay when the burst sequence crosses the first 16-word boundary. (See Figure 39, “Word Boundary” on page 84 for word boundary description.)

Whether this delay occurs depends on the starting address.

- If the starting address is aligned to a 4-word boundary, there is no delay.
- If the starting address is the end of a 4-word boundary, the output delay is one clock cycle less than the First Access Latency Count; this is the worst-case delay.

The delay takes place only once, and only if the burst sequence crosses a 16-word boundary. The WAIT pin informs the system of this delay. For timing diagrams of WAIT functionality, see these figures:

- Figure 11, “Single Synchronous Read-Array Operation Waveform” on page 35
- Figure 12, “Synchronous 4-Word Burst Read Operation Waveform” on page 36
- Figure 13, “WAIT Functionality for EOWL (End-of-Word Line) Condition Waveform” on page 37

Table 30. Sequence and Burst Length

	Start Addr. (Dec)	Burst Addressing Sequence (Decimal)			
		4-Word Burst CR[2:0]=001b	8-Word Burst CR[2:0]=010b	16-Word Burst1 CR[2:0]=011b	Continuous Burst CR[2:0]=111b
		Linear	Linear	Linear	Linear
Wrap (CR[3]=0)	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2...14-15	0-1-2-3-4-5-6-...
	1	1-2-3-0	1-2-3-4-5-6-7-0	1-2-3...14-15-0	1-2-3-4-5-6-7-...
	2	2-3-0-1	2-3-4-5-6-7-0-1	2-3-4...15-0-1	2-3-4-5-6-7-8-...
	3	3-0-1-2	3-4-5-6-7-0-1-2	3-4-5...15-0-1-2	3-4-5-6-7-8-9-...
	4		4-5-6-7-0-1-2-3	4-5-6...15-0-1-2-3	4-5-6-7-8-9-10...
	5		5-6-7-0-1-2-3-4	5-6-7...15-0-1...4	5-6-7-8-9-10-11...
	6		6-7-0-1-2-3-4-5	6-7-8...15-0-1...5	6-7-8-9-10-11-12-...
	7		7-0-1-2-3-4-5-6	7-8-9...15-0-1...6	7-8-9-10-11-12-13...
	⋮	⋮	⋮	⋮	⋮
	14			14-15-0-1...13	14-15-16-17-18-19-20-...
	15			15-0-1-2-3...14	15-16-17-18-19-...
No-Wrap (CR[3]=1)	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2...14-15	0-1-2-3-4-5-6-...
	1	1-2-3-4	1-2-3-4-5-6-7-8	1-2-3...15-16	1-2-3-4-5-6-7-...
	2	2-3-4-5	2-3-4-5-6-7-8-9	2-3-4...16-17	2-3-4-5-6-7-8-...
	3	3-4-5-6	3-4-5-6-7-8-9-10	3-4-5...17-18	3-4-5-6-7-8-9-...
	4		4-5-6-7-8-9-10-11	4-5-6...18-19	4-5-6-7-8-9-10...
	5		5-6-7-8-9-10-11-12	5-6-7...19-20	5-6-7-8-9-10-11...
	6		6-7-8-9-10-11-12-13	6-7-8...20-21	6-7-8-9-10-11-12-...
	7		7-8-9-10-11-12-13-14	7-8-9...21-22	7-8-9-10-11-12-13...
	⋮	⋮	⋮	⋮	⋮
	14			14-15...28-29	14-15-16-17-18-19-20-...
	15			15-16...29-30	15-16-17-18-19-20-21-...

Note: Available on the 130 nm lithography.

14.8 Clock Edge (RCR[6])

Configuring the valid clock edge enables a flexible memory interface to a wide range of burst CPUs. Clock configuration sets the flash device to start a burst cycle, output data, and assert WAIT on the rising or falling edge of the clock.

14.9 Burst Wrap (RCR[3])

The burst wrap bit determines whether 4-word, 8-word, or 16-word burst accesses wrap within the burst-length boundary, or they cross word-length boundaries to perform linear accesses.

No-wrap mode (RCR[3]=1) enables WAIT to hold off the system processor, as it does in the continuous burst mode, until valid data is available.

In no-wrap mode (RCR[3]=0), the flash device operates similarly to continuous linear burst mode, but consumes less power during 4-word, 8-word, or 16-word bursts.

For example, if RCR[3]=0 (wrap mode) and RCR[2:0] = 1h (4-word burst), possible linear burst sequences are 0-1-2-3, 1-2-3-0, 2-3-0-1, 3-0-1-2.

If RCR[3]=1 (no-wrap mode) and RCR[2:0] = 1h (4-word burst length), then possible linear burst sequences are 0-1-2-3, 1-2-3-4, 2-3-4-5, and 3-4-5-6. RCR[3]=1 not only enables limited non-aligned sequential bursts, but also reduces power by minimizing the number of internal read operations.

Setting RCR[2:0] bits for continuous linear burst mode (7h) also achieves the above 4-word burst sequences. However, significantly more power might be consumed. The 1-2-3-4 sequence, for example, consumes power during the initial access, again during the internal pipeline lookup as the processor reads word 2, and possibly again, depending on system timing, near the end of the sequence as the flash device pipelines the next 4-word sequence. RCR[3]=1 while in 4-word burst mode (no-wrap mode) reduces this excess power consumption.

14.10 Burst Length (RCR[2:0])

The burst length is the number of words the flash device outputs in a synchronous read access. 4-word, 8-word, 16-word, and continuous-word are supported.

In 4-word, 8-word, or 16-word burst configuration, the burst wrap bit (RCR[3]) determines whether burst accesses wrap within word-length boundaries, or they cross word-length boundaries to perform a linear access.

After an address is specified, the flash device outputs data until it reaches the end of its burstable address space. Continuous burst accesses are linear only (burst wrap bit RCR[3] is ignored during continuous burst) and do not wrap within word-length boundaries (see Table 30, “Sequence and Burst Length” on page 88).

Appendix A Write State Machine

Table 31 shows the command state transitions, based on incoming commands. Only one partition can be actively programming or erasing at a time.

Table 31. Next State Table (Sheet 1 of 2)

Write State Machine (WSM) Next State Table

***Chip* Next State after Command Input**

Current Chip State[8]		Read Array[3] (FFH)	Program Setup[4,5] (10H/40H)	Erase Setup[4,5] (20H)	Enhanced Factory Pgm Setup[4] (30H)	BE Confirm, P/E Resume, ULB Confirm[9] (D0H)	Program/ Erase Suspend (B0H)	Read Status (70H)	Clear Status Register[6] (50H)	Read ID/Query (90H, 98H)
Ready		Ready	Program Setup	Erase Setup	EFP Setup	Ready				
Lock/CR Setup		Ready (Lock Error)				Ready	Ready (Lock Error)			
OTP	Setup	OTP Busy								
	Busy									
Program	Setup	Program Busy								
	Busy	Program Busy					Pgm Susp	Program Busy		
	Suspend	Program Suspend				Pgm Busy	Program Suspend			
Erase	Setup	Ready (Error)				Erase Busy	Ready (Error)			
	Busy	Erase Busy					Erase Susp	Erase Busy		
	Suspend	Erase Suspend	Pgm in Erase Susp Setup	Erase Suspend		Erase Busy	Erase Suspend			
Program in Erase Suspend	Setup	Program in Erase Suspend Busy								
	Busy	Program in Erase Suspend Busy					Pgm Susp in Erase Susp	Program in Erase Suspend Busy		
	Suspend	Program Suspend in Erase Suspend				Pgm in Erase Susp Busy	Program Suspend in Erase Suspend			
Lock/CR Setup in Erase Suspend		Erase Suspend (Lock Error)				Erase Susp	Erase Suspend (Lock Error)			
Enhanced Factory Program	Setup	Ready (Error)				EFP Busy	Ready (Error)			
	EFP Busy	EFP Busy[7]								
	EFP Verify	Verify Busy[7]								

Output Next State Table[1]

***Output* Next State after Command Input**

Pgm Setup, Erase Setup, OTP Setup, Pgm in Erase Susp Setup, EFP Setup, EFP Busy, Verify Busy	Status						
Lock/CR Setup, Lock/CR Setup in Erase Susp	Status						
OTP Busy	Array[3]	Status	Output does not change	Status	Output does not change	Status	
Ready, Pgm Busy, Pgm Suspend, Erase Busy, Erase Suspend, Pgm In Erase Susp Busy, Pgm Susp In Erase Susp						ID/Query	

Table 31. Next State Table (Sheet 2 of 2)

Chip Next State after Command Input

Write State Machine (WSM) Next State Table

Current Chip State[8]		Lock, Unlock, Lock-down, CR setup[5] (60H)	OTP Setup[5] (C0H)	Lock Block Confirm[9] (01H)	Lock-Down Block Confirm[9] (2FH)	Write CR Confirm[9] (03H)	Enhanced Fact Pgm Exit (blk add <> WA0) (XXXXH)	Illegal commands or EFP data[2] (other codes)	WSM Operation Completes
Ready		Lock/CR Setup	OTP Setup	Ready					N/A
Lock/CR Setup		Ready (Lock Error)		Ready	Ready	Ready	Ready (Lock Error)		
OTP	Setup	OTP Busy							
	Busy								Ready
Program	Setup	Program Busy							N/A
	Busy	Program Busy							Ready
	Suspend	Program Suspend							N/A
Erase	Setup	Ready (Error)							
	Busy	Erase Busy						Erase Busy	Ready
	Suspend	Lock/CR Setup in Erase Susp	Erase Suspend						N/A
Program in Erase Suspend	Setup	Program in Erase Suspend Busy							
	Busy	Program in Erase Suspend Busy							Erase Suspend
	Suspend	Program Suspend in Erase Suspend							
Lock/CR Setup in Erase Suspend		Erase Suspend (Lock Error)		Erase Susp	Erase Susp	Erase Susp	Erase Suspend (Lock Error)		N/A
Enhanced Factory Program	Setup	Ready (Error)							
	EFP Busy	EFP Busy[7]					EFP Verify	EFP Busy[7]	
	EFP Verify	Verify Busy[7]					Ready	EFP Verify[7]	Ready

Output Next State after Command Input

Output Next State Table[1]

Pgm Setup, Erase Setup, OTP Setup, Pgm in Erase Susp Setup, EFP Setup, EFP Busy, Verify Busy	Status					Output does not change
Lock/CR Setup, Lock/CR Setup in Erase Susp	Status			Array	Status	
OTP Busy	Status	Output does not change		Array	Output does not change	
Ready, Pgm Busy, Pgm Suspend, Erase Busy, Erase Suspend, Pgm In Erase Susp Busy, Pgm Susp In Erase Susp						

Notes:

1. The output state shows the type of data that appears at the outputs if the partition address is the same as the command address.
   - — A partition can be placed in Read Array, Read Status or Read ID/CFI, depending on the command issued.
   - — Each partition stays in its last output state (Array, ID/CFI or Status) until a new command changes it. The next WSM state does not depend on the output state of the partition.
   - — For example, if the partition #1 output state is Read Array and the partition #4 output state is Read Status, every read from partition #4 (without issuing a new command) outputs the Status register.

2. Illegal commands are any commands not defined in the command set.
3. All partitions default to Read Array mode at power-up. A Read Array command issued to a busy partition results in undetermined data when a partition address is read.
4. Both cycles of two-cycle commands must be issued to the same partition address. If the two cycles are issued to different partitions, the address used for the second write cycle determines the active partition. Both partitions output status information when read.
5. If the WSM is active, both cycles of a two-cycle command are ignored. This feature differs from previous Intel flash memory devices.
6. The Clear Status command clears status register error bits, except when the WSM is running (Pgm Busy, Erase Busy, Pgm Busy In Erase Suspend, OTP Busy, EFP modes) or suspended (Erase Suspend, Pgm Suspend, Pgm Suspend In Erase Suspend).
7. EFP writes are allowed only when status register bit SR.0 = 0. EFP is busy if the Block Address = the address at the EFP Confirm command. Any other commands are treated as data.
8. The current state is the state of the WSM, not the state of the partition.
9. Confirm commands (Lock Block, Unlock Block, Lock-down Block, Configuration Register) perform the operation and then move to the Ready State.
10. In Erase suspend mode, the only valid two-cycle commands are Program Word, Lock/Unlock/Lockdown Block, and CR Write. Both cycles of other two-cycle commands (Program OTP & confirm, EFP Setup & confirm, Erase setup & confirm) are ignored. In Program suspend or Program suspend in Erase suspend, both cycles of all two-cycle commands are ignored.

Appendix B Common Flash Interface

This appendix defines the data structure or *database* returned by the Common Flash Interface (CFI) Query command. System software parses this structure to gain critical information, such as block size, density, x8/x16, and electrical specifications.

Once this information has been obtained, the software can determine which command sets to use to enable flash device writes, enable block erases, and otherwise control the flash device. The Query is part of an overall specification for multiple command set and control interface descriptions, which is called the Common Flash Interface, or CFI.

B.1 Query Structure Output

The Query database allows system software to obtain information for controlling the flash device. This section describes the flash device CFI-compliant interface that allows access to Query data.

Query data are presented on the lowest-order data outputs (DQ0-7) only. The numerical offset value is the address relative to the maximum bus width that the flash device supports. On the W30 family of flash memory devices, the Query table device starting address is a 10h, which is a word address for x16 flash devices.

For a word-wide (x16) flash device, the first two Query-structure bytes, ASCII Q and R, appear on the low byte at word addresses 10h and 11h.

- This CFI-compliant flash device outputs 00h data on upper bytes.
- The flash device outputs ASCII Q in the low byte (DQ_{0-7}) and 00h in the high byte (DQ_{8-15}).

At Query addresses containing two or more bytes of information, the least significant data byte is presented at the lower address, and the most significant data byte is presented at the higher address.

In all of the following tables, addresses and data are represented in hexadecimal notation, so the *h* suffix has been dropped. In addition, because the upper byte of word-wide flash devices is always *00h*, the leading 00 has been dropped from the table notation, and only the lower byte value is shown. Any x16 flash device outputs can be assumed to have 00h on the upper byte in this mode.

Table 32. Summary of Query Structure Output as a Function of the Flash Device and Mode

Device	Hex Offset	Hex Code	ASCII Value
Device Addresses	00010: 00011: 00012:	51 52 59	Q R Y

Table 33. Example of Query Structure Output of x16- and x8 Flash Devices

Word Addressing:			Byte Addressing:		
Offset	Hex Code	Value	Offset	Hex Code	Value
A_X—A_0	D_{15}—D_0		A_X—A_0	D_7—D_0	
00010h	0051	“Q”	00010h	51	Q
00011h	0052	“R”	00011h	52	R
00012h	0059	“Y”	00012h	59	Y
00013h	P ID_{LO}	PrVendor	00013h	P ID_{LO}	PrVendor
00014h	P ID_{HI}	ID #	00014h	P ID_{LO}	ID #
00015h	P_{LO}	PrVendor	00015h	P ID_{HI}	ID #
00016h	P_{HI}	TblAdr	00016h	...	...
00017h	A ID_{LO}	AltVendor	00017h		
00018h	A ID_{HI}	ID #	00018h		
...	...	...	...		

B.2 Query Structure Overview

The Query command causes the flash device to display the Common Flash Interface (CFI) Query structure or *database*. Table 34 summarizes the structure sub-sections and address locations.

Table 34. Query Structure

Offset	Sub-Section Name	Description(1)
00000h		Manufacturer Code
00001h		Device Code
(BA+2)h(2)	Block Status register	Block-specific information
00004-Fh	Reserved	Reserved for vendor-specific information
00010h	CFI query identification string	Command set ID and vendor data offset
0001Bh	System interface information	Device timing & voltage information
00027h	Device geometry definition	Flash device layout
P(3)	Primary Intel-specific Extended Query Table	Vendor-defined additional information specific to the Primary Vendor Algorithm

Notes:
1. Refer to the Section B.1, “Query Structure Output” on page 93 and offset 28h, for the detailed definition of the offset address as a function of the flash device bus width and mode.
2. BA = Block Address beginning location (for example, 08000h is the block 1’beginning location when the block size is 32K-word).
3. Offset 15 defines P, which points to the Primary Intel-specific Extended Query Table.

B.3 Block Status Register

The Block Status Register indicates whether an erase operation completed successfully, a given block is locked, or a given block can be accessed for flash memory program/erase operations.

Block Erase Status (BSR.1) allows system software to determine the success of the last block erase operation. Use BSR.1 just after power-up to verify that the VCC supply was not accidentally removed during an erase operation.

Table 35. Block Status Register

Offset	Length	Description	Add.	Value
(BA+2)h[1]	1	Block Lock Status Register	BA+2	--00 or --01
		BSR.0 Block lock status 0 = Unlocked 1 = Locked	BA+2	(bit 0): 0 or 1
		BSR.1 Block lock-down status 0 = Not locked down 1 = Locked down	BA+2	(bit 1): 0 or 1
		BSR 2–7: Reserved for future use	BA+2	(bit 2–7): 0

Notes:

1. BA = Block Address beginning location (for example, 08000h is the block 1 beginning location when the block size is 32K-word).

B.4 CFI Query Identification String

The Identification String verifies that the component supports the Common Flash Interface specification. It also indicates the specification version and supported vendor-specified command set(s).

Table 36. CFI Identification

Offset	Length	Description	Add.	Hex Code	Value
10h	3	Query-unique ASCII string "QRY"	10: 11: 12:	--51 --52 --59	Q R Y
13h	2	Primary vendor command set and control interface ID code. 16-bit ID code for vendor-specified algorithms	13: 14:	--03 --00	
15h	2	Extended Query Table primary algorithm address	15: 16:	--39 --00	
17h	2	Alternate vendor command set and control interface ID code. 0000h means no second vendor-specified algorithm exists	17: 18:	--00 --00	
19h	2	Secondary algorithm Extended Query Table address. 0000h means none exists	19: 1A:	--00 --00	

Table 37. System Interface Information

Offset	Length	Description	Add.	Hex Code	Value
1Bh	1	V_{CC} logic supply minimum program/erase voltage bits 0–3 BCD 100 mV bits 4–7 BCD volts	1B:	--17	1.7V
1Ch	1	V_{CC} logic supply maximum program/erase voltage bits 0–3 BCD 100 mV bits 4–7 BCD volts	1C:	--19	1.9V
1Dh	1	V_{PP} [programming] supply minimum program/erase voltage bits 0–3 BCD 100 mV bits 4–7 HEX volts	1D:	--B4	11.4V
1Eh	1	V_{PP} [programming] supply maximum program/erase voltage bits 0–3 BCD 100 mV bits 4–7 HEX volts	1E:	--C6	12.6V
1Fh	1	"n" such that typical single word program time-out = 2^n µ-sec	1F:	--04	16µs
20h	1	"n" such that typical max. buffer write time-out = 2^n µ-sec	20:	--00	NA
21h	1	"n" such that typical block erase time-out = 2^n m-sec	21:	--0A	1s
22h	1	"n" such that typical full chip erase time-out = 2^n m-sec	22:	--00	NA
23h	1	"n" such that maximum word program time-out = 2^n times typical	23:	--04	256µs
24h	1	"n" such that maximum buffer write time-out = 2^n times typical	24:	--00	NA
25h	1	"n" such that maximum block erase time-out = 2^n times typical	25:	--03	8s
26h	1	"n" such that maximum chip erase time-out = 2^n times typical	26:	--00	NA

B.5 Flash Device Geometry Definition

Table 38. Flash Device Geometry Definition

Offset	Length	Description	Code		
27h	1	"n" such that device size = 2^n in number of bytes	27:	See table below	
28h	2	Flash device interface code assignment: "n" such that n+1 specifies the bit field that represents the flash device width capabilities as described in the table: 7 6 5 4 3 2 1 0 — — — — x64 x32 x16 x8 15 14 13 12 11 10 9 8 — — — — — — — —	28: 29:	--01 --00	x16
2Ah	2	"n" such that maximum number of bytes in write buffer = 2^n	2A: 2B:	--00 --00	0
2Ch	1	Number of erase block regions (x) within device: 1. x = 0 means no erase blocking; the device erases in bulk 2. x specifies the number of device regions with one or more contiguous same-size erase blocks. 3. Symmetrically blocked partitions have one blocking region	2C:	See table below	
2Dh	4	Erase Block Region 1 Information bits 0–15 = y, y+1 = number of identical-size erase blocks bits 16–31 = z, region erase block(s) size are z x 256 bytes	2D: 2E: 2F: 30:	See table below	
31h	4	Erase Block Region 2 Information bits 0–15 = y, y+1 = number of identical-size erase blocks bits 16–31 = z, region erase block(s) size are z x 256 bytes	31: 32: 33: 34:	See table below	
35h	4	Reserved for future erase block region information	35: 36: 37: 38:	See table below	

Address	32 Mbit		64 Mbit		128 Mbit	
	–B	–T	–B	–T	–B	–T
27:	--16	--16	--17	--17	--18	--18
28:	--01	--01	--01	--01	--01	--01
29:	--00	--00	--00	--00	--00	--00
2A:	--00	--00	--00	--00	--00	--00
2B:	--00	--00	--00	--00	--00	--00
2C:	--02	--02	--02	--02	--02	--02
2D:	--07	--3E	--07	--7E	--07	--FE
2E:	--00	--00	--00	--00	--00	--00
2F:	--20	--00	--20	--00	--20	--00
30:	--00	--01	--00	--01	--00	--01
31:	--3E	--07	--7E	--07	--FE	--07
32:	--00	--00	--00	--00	--00	--00
33:	--00	--20	--00	--20	--00	--20
34:	--01	--00	--01	--00	--01	--00
35:	--00	--00	--00	--00	--00	--00
36:	--00	--00	--00	--00	--00	--00
37:	--00	--00	--00	--00	--00	--00
38:	--00	--00	--00	--00	--00	--00

B.6 Intel-Specific Extended Query Table

Table 39. Primary Vendor-Specific Extended Query

Offset[1] P = 39h	Length	Description (Optional flash features and commands)	Add.	Hex Code	Value
(P+0)h	3	Primary extended query table	39:	--50	"P"
(P+1)h		Unique ASCII string "PRI"	3A:	--52	"R"
(P+2)h			3B:	--49	"I"
(P+3)h	1	Major version number, ASCII	3C:	--31	"1"
(P+4)h	1	Minor version number, ASCII	3D:	--33	"3"
(P+5)h	4	Optional feature and command support (1=yes, 0=no)	3E:	--E6	
(P+6)h		*bits 10–31 are reserved; undefined bits are "0." If bit 31 is*	3F:	--03	
(P+7)h		*"1" then another 31 bit field of Optional features follows at*	40:	--00	
(P+8)h		*the end of the bit–30 field.*	41:	--00	
		bit 0 Chip erase supported	bit 0	= 0	No
		bit 1 Suspend erase supported	bit 1	= 1	Yes
		bit 2 Suspend program supported	bit 2	= 1	Yes
		bit 3 Legacy lock/unlock supported	bit 3	= 0	No
		bit 4 Queued erase supported	bit 4	= 0	No
		bit 5 Instant individual block locking supported	bit 5	= 1	Yes
		bit 6 Protection bits supported	bit 6	= 1	Yes
		bit 7 Pagemode read supported	bit 7	= 1	Yes
		bit 8 Synchronous read supported	bit 8	= 1	Yes
		bit 9 Simultaneous operations supported	bit 9	= 1	Yes
(P+9)h	1	Supported functions after suspend: read Array, Status, Query	42:	--01	
		Other supported operations are:			
		bits 1–7 reserved; undefined bits are "0"			
		bit 0 Program supported after erase suspend	bit 0	= 1	Yes
(P+A)h	2	Block status register mask	43:	--03	
(P+B)h		*bits 2–15 are Reserved; undefined bits are "0"*	44:	--00	
		bit 0 Block Lock-Bit Status register active	bit 0	= 1	Yes
		bit 1 Block Lock-Down Bit Status active	bit 1	= 1	Yes
(P+C)h	1	V_{CC} logic supply highest performance program/erase voltage	45:	--18	1.8V
		bits 0–3 BCD value in 100 mV			
		bits 4–7 BCD value in volts			
(P+D)h	1	V_{PP} optimum program/erase supply voltage	46:	--C0	12.0V
		bits 0–3 BCD value in 100 mV			
		bits 4–7 HEX value in volts			

Table 40. Protection Register Information

Offset[1] P = 39h	Length	Description (Optional flash device features and commands)	Add.	Hex Code	Value
(P+E)h	1	Number of Protection register fields in JEDEC ID space. 00h indicates that 256 protection fields are available	47:	--01	1
(P+F)h (P+10)h (P+11)h (P+12)h	4	Protection Field 1: Protection Description This field describes user-available One Time Programmable (OTP) Protection register bytes. • Some bytes are pre-programmed with flash device-unique serial numbers. • Other bytes are user programmable. Bits 0-15 point to the Protection register Lock byte, the first byte in the section. The following bytes are factory pre-programmed and user-programmable. • bits 0--7 = Lock/bytes Jedec-plane physical low address • bits 8--15 = Lock/bytes Jedec-plane physical high address • bits 16--23 = *n* such that 2*n* = factory pre-programmed bytes • bits 24--31 =*n* such that 2*n* = user programmable bytes	48: 49: 4A: 4B:	--80 --00 --03 --03	80h 00h 8 byte 8 byte

Table 41. Burst Read Information for Non-Multiplexed Flash Device

Offset[1] P = 39h	Length	Description (Optional flash features and commands)	Add.	Hex Code	Value
(P+13)h	1	Page Mode Read capability bits 0–7 = "n" such that 2^n HEX value represents the number of read-page bytes. See offset 28h for device word width to determine page-mode data output width. 00h indicates no read page buffer.	4C:	--03	8 byte
(P+14)h	1	Number of synchronous mode read configuration fields that follow. 00h indicates no burst capability.	4D:	--04	4
(P+15)h	1	Synchronous mode read capability configuration 1 Bits 3–7 = Reserved bits 0–2 "n" such that 2^{n+1} HEX value represents the maximum number of continuous synchronous reads when the device is configured for its maximum word width. A value of 07h indicates that the device is capable of continuous linear bursts that will output data until the internal burst counter reaches the end of the device's burstable address space. This field's 3-bit value can be written directly to the Read Configuration Register bits 0–2 if the device is configured for its maximum word width. See offset 28h for word width to determine the burst data output width.	4E:	--01	4
(P+16)h	1	Synchronous mode read capability configuration 2	4F:	--02	8
(P+17)h	1	Synchronous mode read capability configuration 3	50:	--03	16
(P+18)h	1	Synchronous mode read capability configuration 4	51:	--07	Cont

Table 42. Partition and Erase-Block Region Information

Offset[1] P = 39h		Description	See table below		
				Address	
Bottom	Top	(Optional flash features and commands)	Len	Bot	Top
(P+19)h	(P+19)h	Number of device hardware-partition regions within the device. x = 0: a single hardware partition device (no fields follow). x specifies the number of device partition regions containing one or more contiguous erase block regions.	1	52:	52:

Table 43. Partition Region 1 Information

Offset[1] P = 39h		Description	See table below		
				Address	
Bottom	Top	(Optional flash features and commands)	Len	Bot	Top
(P+1A)h (P+1B)h	(P+1A)h (P+1B)h	Number of identical partitions within the partition region	2	53: 54:	53: 54:
(P+1C)h	(P+1C)h	Number of program or erase operations allowed in a partition bits 0–3 = number of simultaneous Program operations bits 4–7 = number of simultaneous Erase operations	1	55:	55:
(P+1D)h	(P+1D)h	Simultaneous program or erase operations allowed in other partitions while a partition in this region is in Program mode bits 0–3 = number of simultaneous Program operations bits 4–7 = number of simultaneous Erase operations	1	56:	56:
(P+1E)h	(P+1E)h	Simultaneous program or erase operations allowed in other partitions while a partition in this region is in Erase mode bits 0–3 = number of simultaneous Program operations bits 4–7 = number of simultaneous Erase operations	1	57:	57:
(P+1F)h	(P+1F)h	Types of erase block regions in this Partition Region. x = 0 = no erase blocking; the Partition Region erases in bulk x = number of erase block regions w/ contiguous same-size erase blocks. Symmetrically blocked partitions have one blocking region. Partition size = (Type 1 blocks)x(Type 1 block sizes) + (Type 2 blocks)x(Type 2 block sizes) +…+ (Type n blocks)x(Type n block sizes)	1	58:	58:
(P+20)h (P+21)h (P+22)h (P+23)h	(P+20)h (P+21)h (P+22)h (P+23)h	Partition Region 1 Erase Block Type 1 Information bits 0–15 = y, y+1 = number of identical-size erase blocks bits 16–31 = z, region erase block(s) size are z x 256 bytes	4	59: 5A: 5B: 5C:	59: 5A: 5B: 5C:
(P+24)h (P+25)h	(P+24)h (P+25)h	Partition 1 (Erase Block Type 1) Minimum block erase cycles x 1000	2	5D: 5E:	5D: 5E:
(P+26)h	(P+26)h	Partition 1 (erase block Type 1) bits per cell; internal ECC bits 0–3 = bits per cell in erase region bit 4 = reserved for “internal ECC used” (1=yes, 0=no) bits 5–7 = reserve for future use	1	5F:	5F:
(P+27)h	(P+27)h	Partition 1 (erase block Type 1) page mode and synchronous mode capabilities defined in Table 10. bit 0 = page-mode host reads permitted (1=yes, 0=no) bit 1 = synchronous host reads permitted (1=yes, 0=no) bit 2 = synchronous host writes permitted (1=yes, 0=no) bits 3–7 = reserved for future use	1	60:	60:
(P+28)h (P+29)h (P+2A)h (P+2B)h		Partition Region 1 Erase Block Type 2 Information bits 0–15 = y, y+1 = number of identical-size erase blocks bits 16–31 = z, region erase block(s) size are z x 256 bytes (bottom parameter device only)	4	61: 62: 63: 64:	
(P+2C)h (P+2D)h		Partition 1 (Erase block Type 2) Minimum block erase cycles x 1000	2	65: 66:	
(P+2E)h		Partition 1 (Erase block Type 2) bits per cell bits 0–3 = bits per cell in erase region bit 4 = reserved for “internal ECC used” (1=yes, 0=no) bits 5–7 = reserve for future use	1	67:	
(P+2F)h		Partition 1 (Erase block Type 2) pagemode and synchronous mode capabilities defined in Table 10 bit 0 = page-mode host reads permitted (1=yes, 0=no) bit 1 = synchronous host reads permitted (1=yes, 0=no) bit 2 = synchronous host writes permitted (1=yes, 0=no) bits 3–7 = reserved for future use	1	68:	

Table 44. Partition Region 2 Information

Offset[1] P = 39h		Description	See table below		
				Address	
Bottom	Top	(Optional flash features and commands)	Len	Bot	Top
(P+30)h (P+31)h	(P+28)h (P+29)h	Number of identical partitions within the partition region	2	69: 6A:	61: 62:
(P+32)h	(P+2A)h	Number of program or erase operations allowed in a partition bits 0–3 = number of simultaneous Program operations bits 4–7 = number of simultaneous Erase operations	1	6B:	63:
(P+33)h	(P+2B)h	Simultaneous program or erase operations allowed in other partitions while a partition in this region is in Program mode bits 0–3 = number of simultaneous Program operations bits 4–7 = number of simultaneous Erase operations	1	6C:	64:
(P+34)h	(P+2C)h	Simultaneous program or erase operations allowed in other partitions while a partition in this region is in Erase mode bits 0–3 = number of simultaneous Program operations bits 4–7 = number of simultaneous Erase operations	1	6D:	65:
(P+35)h	(P+2D)h	Types of erase block regions in this Partition Region. x = 0 = no erase blocking; the Partition Region erases in bulk x = number of erase block regions w/ contiguous same-size erase blocks. Symmetrically blocked partitions have one blocking region. Partition size = (Type 1 blocks)x(Type 1 block sizes) + (Type 2 blocks)x(Type 2 block sizes) +…+ (Type n blocks)x(Type n block sizes)	1	6E:	66:
(P+36)h (P+37)h (P+38)h (P+39)h	(P+2E)h (P+2F)h (P+30)h (P+31)h	Partition Region 2 Erase Block Type 1 Information bits 0–15 = y, y+1 = number of identical-size erase blocks bits 16–31 = z, region erase block(s) size are z x 256 bytes	4	6F: 70: 71: 72:	67: 68: 69: 6A:
(P+3A)h (P+3B)h	(P+32)h (P+33)h	Partition 2 (Erase block Type 1) Minimum block erase cycles x 1000	2	73: 74:	6B: 6C:
(P+3C)h	(P+34)h	Partition 2 (Erase block Type 1) bits per cell bits 0–3 = bits per cell in erase region bit 4 = reserved for “internal ECC used” (1=yes, 0=no) bits 5–7 = reserve for future use	1	75:	6D:
(P+3D)h	(P+35)h	Partition 2 (erase block Type 1) pagemode and synchronous mode capabilities as defined in Table 10. bit 0 = page-mode host reads permitted (1=yes, 0=no) bit 1 = synchronous host reads permitted (1=yes, 0=no) bit 2 = synchronous host writes permitted (1=yes, 0=no) bits 3–7 = reserved for future use	1	76:	6E:
	(P+36)h (P+37)h (P+38)h (P+39)h	Partition Region 2 Erase Block Type 2 Information bits 0–15 = y, y+1 = number of identical-size erase blocks bits 16–31 = z, region erase block(s) size are z x 256 bytes	4		6F: 70: 71: 72:
	(P+3A)h (P+3B)h	Partition 2 (Erase Block Type 2) Minimum block erase cycles x 1000	2		73: 74:
	(P+3C)h	Partition 2 (Erase Block Type 2) bits per cell bits 0–3 = bits per cell in erase region bit 4 = reserved for “internal ECC used” (1=yes, 0=no) bits 5–7 = reserved for future use	1		75:
	(P+3D)h	Partition 2 (Erase block Type 2) pagemode and synchronous mode capabilities as defined in Table 10. bit 0 = page-mode host reads permitted (1=yes, 0=no) bit 1 = synchronous host reads permitted (1=yes, 0=no) bit 2 = synchronous host writes permitted (1=yes, 0=no) bits 3–7 = reserved for future use	1		76:
(P+3E)h	(P+3E)h	Features Space definitions (Reserved for future use)	TBD	77:	77:
(P+3F)h	(P+3F)h	Reserved for future use	Resv'd	78:	78:

Table 45. Partition and Erase-Block Region Information

Address	32 Mbit		64Mbit		128Mbit	
	–B	–T	–B	–T	–B	–T
52:	--02	--02	--02	--02	--02	--02
53:	--01	--07	--01	--0F	--01	--1F
54:	--00	--00	--00	--00	--00	--00
55:	--11	--11	--11	--11	--11	--11
56:	--00	--00	--00	--00	--00	--00
57:	--00	--00	--00	--00	--00	--00
58:	--02	--01	--02	--01	--02	--01
59:	--07	--07	--07	--07	--07	--07
5A:	--00	--00	--00	--00	--00	--00
5B:	--20	--00	--20	--00	--20	--00
5C:	--00	--01	--00	--01	--00	--01
5D:	--64	--64	--64	--64	--64	--64
5E:	--00	--00	--00	--00	--00	--00
5F:	--01	--01	--01	--01	--01	--01
60:	--03	--03	--03	--03	--03	--03
61:	--06	--01	--06	--01	--06	--01
62:	--00	--00	--00	--00	--00	--00
63:	--00	--11	--00	--11	--00	--11
64:	--01	--00	--01	--00	--01	--00
65:	--64	--00	--64	--00	--64	--00
66:	--00	--02	--00	--02	--00	--02
67:	--01	--06	--01	--06	--01	--06
68:	--03	--00	--03	--00	--03	--00
69:	--07	--00	--0F	--00	--1F	--00
6A:	--00	--01	--00	--01	--00	--01
6B:	--11	--64	--11	--64	--11	--64
6C:	--00	--00	--00	--00	--00	--00
6D:	--00	--01	--00	--01	--00	--01
6E:	--01	--03	--01	--03	--01	--03
6F:	--07	--07	--07	--07	--07	--07
70:	--00	--00	--00	--00	--00	--00
71:	--00	--20	--00	--20	--00	--20
72:	--01	--00	--01	--00	--01	--00
73:	--64	--64	--64	--64	--64	--64
74:	--00	--00	--00	--00	--00	--00
75:	--01	--01	--01	--01	--01	--01
76:	--03	--03	--03	--03	--03	--03

Notes:

1. The *P* variable is a pointer which is defined at CFI offset 15h.
2. TPD - Top parameter device.
   BPD - Bottom parameter device.
3. Partition: Each partition is 4 Mb in size. It can contain main blocks OR a combination of both main and parameter blocks.
4. Partition Region: Symmetrical partitions form a partition region.
   — Partition region A. contains all partitions that are made up of main blocks only.
   — Partition region B. contains the partition that is made up of the parameter and the main blocks.

Appendix C Ordering Information

Figure 42. VF BGA Ordering Information

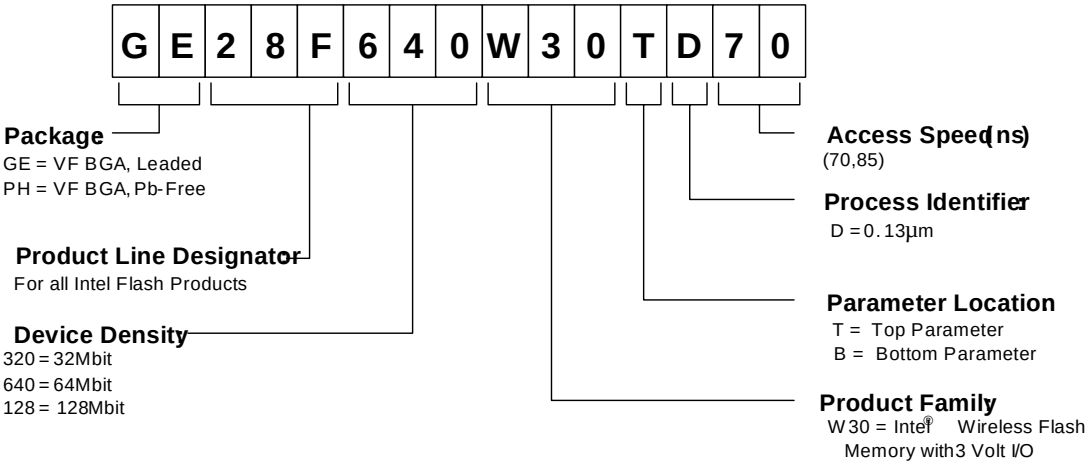


Figure 43. SCSP Ordering Information

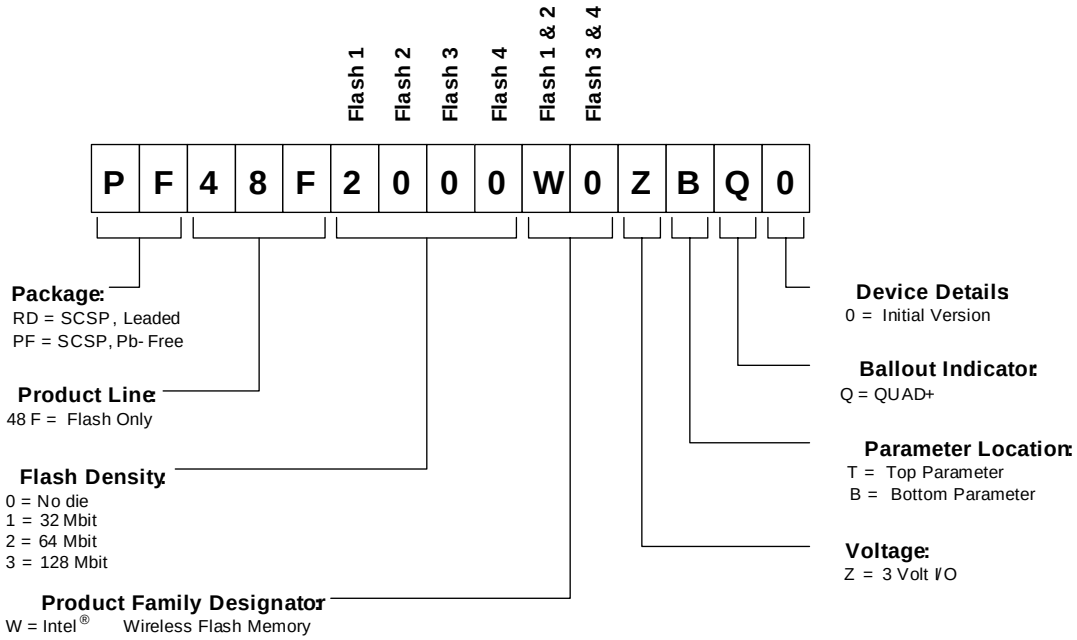


Table 46. W30 Flash Memory Family: Available Product Ordering Information

I/O Voltage (V)	Flash Density	Package Size (mm)	Ballout Name	Ballout Type	Part Number
3.0	32 Mbit	9x7.7x1.0	VF BGA	Leaded	GE28F320W30BD70 GE28F320W30TD70 GE28F320W30BD85 GE28F320W30TD85
				Lead Free	PH28F320W30BD70 PH28F320W30TD70
		10x8x1.2	SCSP	Lead Free	PF48F1000W0ZBQ0 PF48F1000W0ZTQ0
	64 Mbit	9x7.7x1.0	VF BGA	Leaded	GE28F640W30BD70 GE28F640W30TD70
				Lead Free	PH28F640W30BD70 PH28F640W30TD70
		10x8x1.2	SCSP	Lead Free	PF48F2000W0ZBQ0 PF48F2000W0ZTQ0
	128 Mbit	9x11x1.0	VF BGA	Leaded	GE28F128W30BD70 GE28F128W30TD70
		10x8x1.2	SCSP	Leaded	RD48F3000W0ZBQ0 RD48F3000W0ZTQ0