2910A
PCM CODEC - μLAW
8-BIT COMPANDED A/D AND D/A CONVERTER

- **Per Channel, Single Chip Codec**
- **CCITT G711 and G712 Compatible, ATT T1 Compatible with 8th Bit Signaling**
- **Microcomputer Interface with On-Chip Timeslot Computation**
- **Simple Direct Mode Interface When Fixed Timeslots are Used**
- **±5% Power Supplies: +12V, +5V, −5V**
- **78dB Dynamic Range, with Resolution Equivalent to 12-Bit Linear Conversion Around Zero**
- **Precision On-Chip Voltage Reference**
- **Low Power Consumption 230 mW Typ. Standby Power 33mW Typ.**
- **Fabricated with Reliable N-Channel MOS Process**

The Intel 2910A is a fully integrated PCM (Pulse Code Modulation) Codec (Coder-Decoder), fabricated with N-channel silicon gate technology. The high density of integration allows the sample and hold circuits, the digital-to-analog converter, the comparator and the successive approximation register to be integrated on the same chip, along with the logic necessary to interface a full duplex PCM link and provide in-band signaling.

The primary applications are in telephone systems:

- Transmission —T1 Carrier
- Switching —Digital PBX's and Central Office Switching Systems
- Concentration —Subscriber Carrier/Concentrators

The wide dynamic range of the 2910A (78dB) and the minimal conversion time (80μsec minimum) make it an ideal product for other applications, like:

- Date Acquisition • Telemetry • Secure Communications Systems • Signal Processing Systems

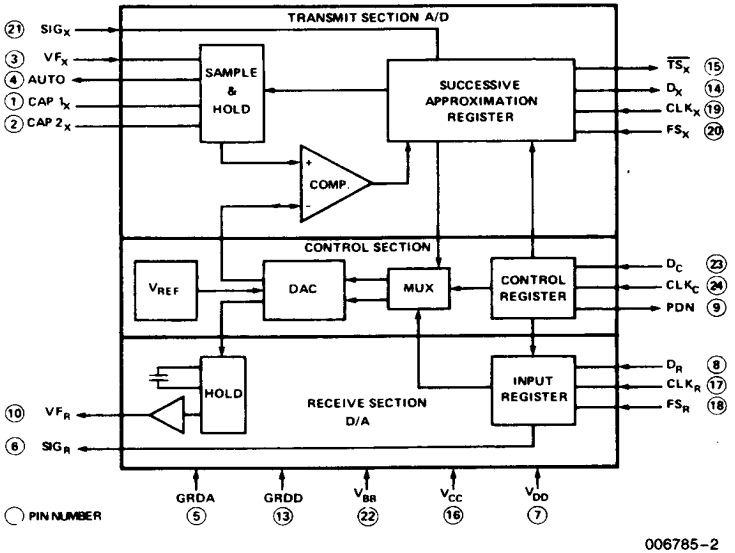

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Figure 1. Block Diagram

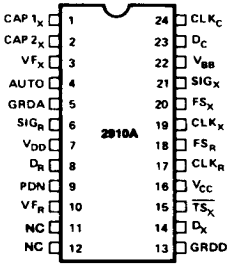

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Figure 2. Pin Configuration

CAP 1_X, CAP 2_X	Holding Capacitor
VF_X	Analog Input
VF_R	Analog Output
D_R, D_C, SIG_X	Digital Input
SIG_R, D_X, $\overline{TS}_X$	Digital Output
CLK_C, CLK_X, CLK_R	Clock Input
FS_X, FS_R	Frame Sync Input
AUTO	Auto Zero Output
V_{BB}	Power (−5V)
V_{CC}	Power (+5V)
V_{DD}	Power (+12V)
PDN	Power Down
GRDA	Analog Ground
GRDD	Digital Ground
NC	No Connect

Figure 3. Pin Names

November 1986
Order Number: 006785-002

Pin Description

Pin No.	Symbol	Function	Description
1	$CAP1_X$	Hold	Connections for the transmit holding capacitor. Refer to Applications section.
2	$CAP2_X$		
3	VF_X	Input	Analog input to be encoded into a PCM word. The signal on this lead is sampled at the same rate as the transmit frame synchronization pulse FS_X, and the sample value is held in the external capacitor connected to the $CAP1_X$ and $CAP2_X$ leads until the encoding process is completed.
4	AUTO	Output	Most significant bit of the encoded PCM word (+5V for negative, −5V for positive inputs). Refer to the Codec Applications section.
5	GRDA	Ground	Analog return common to the transmit and receive analog circuits. Not connected to GRDD internally.
6	SIG_R	Output	Signaling output. SIG_R is updated with the 8th bit of the receive PCM word on signaling frames, and is latched between two signaling frames. TTL interface.
7	V_{DD}	Power	+12V ± 5%; referenced to GRDA.
8	D_R	Input	Receive PCM highway (serial bus) interface. The Codec serially receives a PCM word (8 bits) through this lead at the proper time defined by FS_R, CLK_R, D_C, and CLK_C.
9	PDN	Output	Active high when Codec is in the power down state. Open drain output.
10	VF_R	Output	Analog output. The voltage present on VF_R is the decoded value of the PCM word received on lead D_R. This value is held constant between two conversions.
11	NC	No Connects	Recommended practice is to strap these NC's to GRDA.
12	NC		
13	GRDD	Ground	Ground return common to the logic power supply, V_{CC}.
14	D_X	Output	Output of the transmit side onto the send PCM highway (serial bus). The 8-bit PCM word is serially sent out on this pin at the proper time defined by FS_X, CLK_X, D_C, and CLK_C. TTL three-state output.
15	$\overline{TS}_X$	Output	Normally high, this signal goes low while the Codec is transmitting an 8-bit PCM word on the D_X lead. (Timeslot information used for diagnostic purposes and also to gate the data on the D_X lead.) Open drain output.
16	V_{CC}	Power	+5V ± 5%, referenced to GRDD.
17	CLK_R	Input	Master receive clock defining the bit rate on the receive PCM highway. Typically 1.544 Mbps for a T1 carrier system. Maximum rate 2.1 Mbps. 50% duty cycle. TTL interface.
18	FS_R	Input	Frame synchronization pulse for the receive PCM highway. Resets the on-chip timeslot counter for the receive side. Maximum repetition rate 12 KHz. Also used to differentiate between non-signaling frames and signaling frames on the receive side. TTL interface.

Pin Description (Continued)

Pin No.	Symbol	Function	Description
19	CLK_X	Input	Master transmit clock defining the bit rate on the transmit PCM highway. Typically 1.544 Mbps for a T1 carrier system. Maximum rate 2.1 Mbps. 50% duty cycle. TTL interface.
20	FS_X	Input	Frame synchronization pulse for the transmit PCM highway. Resets the on-chip timeslot counter for the transmit side. Maximum repetition rate 12 KHz. Also used to differentiate between non-signaling frames and signaling frames on the transmit side. TTL interface.
21	SIG_X	Input	Signaling input. This digital input is transmitted as the 8th bit of the PCM word on the D_X lead, on signaling frames. TTL interface.
22	V_{BB}	Power	$-5V \pm 5\%$, referenced to GRDA.
23	D_C	Input	Data input to program the Codec for the chosen mode of operation. Becomes an active low chip select when CLK_C is tied to V_{CC}. TTL interface.
24	CLK_C	Input	Clock input to clock in the data on the D_C lead when the timeslot assignment feature is used; tied to V_{CC} to disable this feature. TTL interface.

FUNCTIONAL DESCRIPTION

The 2910A PCM Codec provides the analog-to-digital and the digital-to-analog conversions necessary to interface a full duplex (4 wires) voice telephone circuit with the PCM highways of a time division multiplexed (TDM) system.

In a typical telephone system the Codec is used between the PCM highways and the channel filters.

The Codec provides two major functions:

- Encoding and decoding of analog signals (voice and call progress tones)
- Encoding and decoding of the signaling and supervision information

On a non-signaling frame, the Codec encodes the incoming analog signal at the frame rate (FS_X) into an 8-bit PCM word which is sent out on the D_X lead at the proper time. Similarly, the Codec fetches an 8-bit PCM word from the receive highway (D_R lead) and decodes an analog value which will remain constant on lead VF_R until the next receive frame. Transmit and receive frames are independent. They can be asynchronous (transmission) or synchronous (switching) with each other.

For channel associated signaling, the Codec transmit side will encode the incoming analog signal as previously described and substitute the signal present on lead SIG_X for the least significant bit of the encoded PCM word. Similarly, on a receive signaling frame, the Codec will decode the 7 most significant bits according to the CCITT G733 recommendation and will output the least significant bit value on the SIG_R lead until the next signaling frame. Signaling frames on the send and receive sides are independent of each other, and are selected by a double-width frame sync pulse on the appropriate channel.

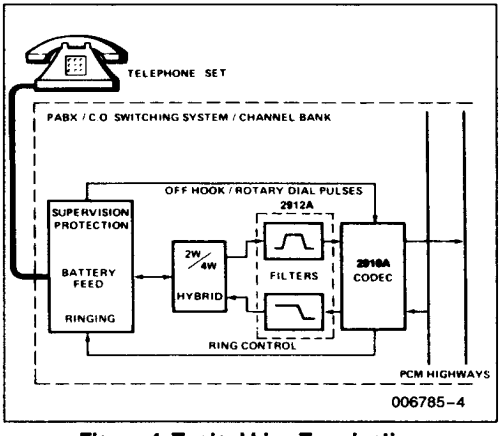


Figure 4. Typical Line Termination

The 2910A Codec is intended to be used on line and trunk terminations. The call progress tones (dial tone, busy tone, ring-back tone, re-order tone), and the prerecorded announcements, can be sent through the voice-path; digital signaling (off hook and disconnect supervision, rotary dial pulses, ring control) is sent through the signaling path.

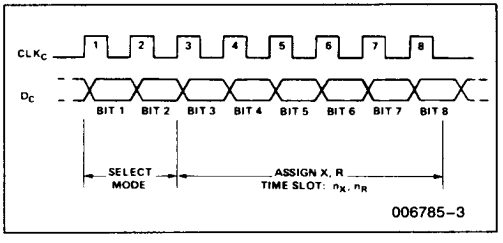
Circuitry is provided within the Codec to internally define the transmit and receive timeslots. In small systems this may eliminate the need for any external timeslot exchange; in large systems it provides one level of concentration. This feature can be bypassed and discrete timeslots sent to each Codec within a system.

In the power-down mode, most functions of the Codec are directly disabled to reduce power dissipation to a minimum.

CODEC OPERATION

Codec Control

The operation of the 2910A is defined by serially loading an 8-bit word through the D_C lead (data) and the CLK_C lead (clock). The loading is asynchronous with the other operations of the Codec, and takes place whenever transitions occur on the CLK_C lead. The D_C input is loaded in during the trailing edge of the CLK_C input.



The control word contains two fields:

Bit 1 and Bit 2 define whether the subsequent 6 bits apply to both the transmit and receive side (00), the transmit side only (01), the receive side only (10), or whether the Codec should go into the standby, powerdown mode (11). In the last case (11), the following 6 bits are irrelevant.

The last 6 bits of the control word define the timeslot assignment, from 000000 (timeslot 1) to 111111 (timeslot 64). Bit 3 is the most significant bit and bit 8 the least significant bit and last into the Codec.

Bit 1	Bit 2	Mode
0	0	X & R
0	1	X
1	0	R
1	1	Standby

Bit						
3	4	5	6	7	8	Timeslot
0	0	0	0	0	0	1
0	0	0	0	0	1	2
			•			•
			•			•
			•			•
			•			•
1	1	1	1	1	1	64

The Codec will retain the control word (or words) until a new word is loaded in or until power is lost. This feature permits dynamic allocation of timeslots for switching applications.

Microcomputer Control Mode

In the microcomputer mode, each Codec performs its own timeslot computation independently for the transmit and receive channels by counting clock pulses (CLK_X and CLK_R). All Codecs tied to the same data bus receive identical framing pulses (FS_X and FS_R). The framing pulses reset the on-chip timeslot counters every frame; hence the timeslot counters of all devices are synchronized. Each Codec is programmed via CLK_C and D_C for the desired transmit and receive timeslots according to the description in the Codec Control Section. All Codecs tied to the same D_R bus will, in general, have different receive timeslots, although that is not a device requirement. There may be separate busses for transmit and receive or all Codecs may transmit and receive over the same bus, in which case the transmit and receive channels must be synchronous ($CLK_X = CLK_R$). There are no other restrictions on timeslot assignments; a device may have the same transmit and receive timeslot even if a single bus is used.

There are several requirements for using the CLK_C-D_C interface in the microcomputer mode.

1) A complete timeslot assignment, consisting of eight negative transitions of CLK_C, must be made in less than one frame period. The assignment

can overlap a framing pulse so long as all 8 control bits are clocked in within a total span of 125 μs (for an 8 KHz frame rate). CLK_C must be left at a TTL low level when not assigning a timeslot.

2) A dead period of two frames must always be observed between successive timeslot assignments. The two frame delay is measured from the rising edge of the first CLK_C transition of the previous timeslot assigned.
3) When the device is in the power-down state (Standby), the following three-step sequence must be followed to power-up the codec to avoid contention on the transmit PCM highway.
   a) Assign a dummy transmit timeslot. The dummy should be at least two timeslots greater than the maximum valid system timeslot (usually 24 or 32). For example, in a 24 timeslot system, the dummy could be any timeslot between 26 and 64. This will power-up the transmit side, but prevent any spurious D_X or $\overline{TS}_X$ outputs.
   b) Two frames later, assign the desired transmit timeslot.
   c) Two frames later assign the desired receive timeslot.
4) Initialization sequence: The device contains an on-chip power-on clear function which guarantees that with proper sequencing of the supplies (V_{CC} or V_{DD} on last), the device will initialize with no timeslot assigned to either the transmit or receive channel. After a supply failure or whenever the supplies are applied, it is recommended that either power down assignment be made first, or the first timeslot assignment be a transmit timeslot or a transmit/receive timeslot. The consequence of making a receive timeslot assignment first, after supply application, is that the transmit channel will assume timeslot 1, potentially producing bus contention.
5) Transmit only/receive only operation is permitted provided that a power down assignment is made first. Otherwise, special circuits which use only one channel should be physically disconnected from the unused bus; this allows a timeslot to be made to an unused channel without consequence.
6) Both frame synchronizing pulses (FS_X, FS_R) must be active at all times after power on clear (after power supplies are turned on). This requirement must be met during powerdown and receive only or transmit only operation, as well as during normal transmit and receive operation.

Example of Microcomputer Control Mode:

The two words 01000001 and 10000010 have been loaded into the Codec. The transmit side is now programmed for timeslot 2 and the receive side for timeslot 3. The Codec will output a PCM word on the transmit PCM highway (bus) during the timeslot 2 of the transmit frame, and will fetch a PCM word from the receive PCM highway during timeslot 3.

5

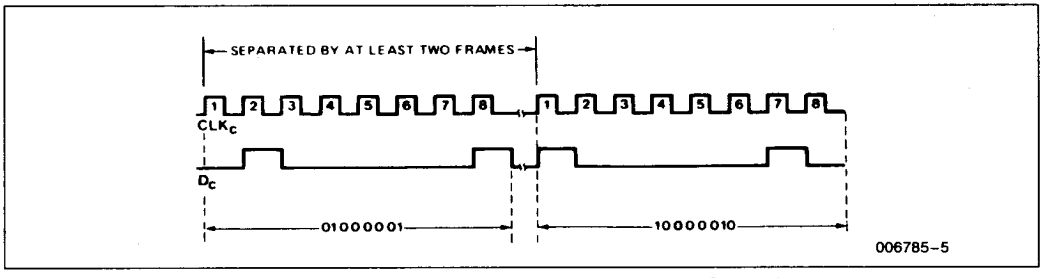


Figure 5. Microcomputer Mode Programming Example

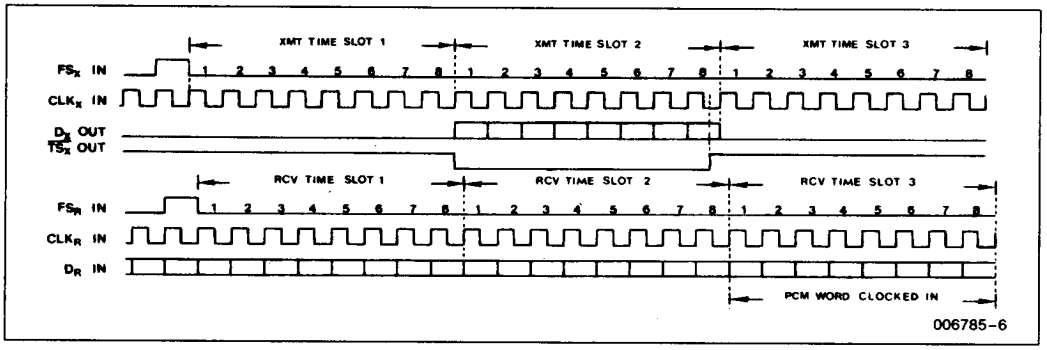


Figure 6. Microcomputer Mode PCM Highway Example

In this example the Codec interface to the PCM highway then functions as shown above. (FS_X and FS_R may be asynchronous.)

Direct Control Mode

The direct mode of operation will be selected when the CLK_C pin is strapped to the +5 volt supply (V_{CC}). In this mode, the D_C pin is an active low chip select. In other words, when D_C is low, the device transmits and receives in the timeslots which follow the appropriate framing pulses. With D_C high the device is in the power down state. Even though CLK_C characteristics are simpler for the 2910A it will operate properly when plugged into a 2910 board.

Deactivation of a channel by removal of the appropriate framing pulse (FS_X or FS_R) is not permitted. Specifically, framing pulses must be applied for a minimum of two frames after a change in state of D_C in order for the D_C change to be internally sensed. In particular, when entering standby in the direct mode, framing pulses must be applied as usual for two frames after D_C is brought high.

The Codec will enter the direct mode within three frame times (375 μs) as measured from the time the device power supplies settle to within the specified limits. This assumes that CLK_C is tied to V_{CC} and that all clocks are available at the time the supplies have settled.

General Control Requirements

All bit and frame clocks should be applied whenever the device is active. In particular, an unused channel cannot be deactivated by removal of its associated frame or bit clock while the other channel of the same device remains active.

A single channel cannot be deactivated except by physical disconnection of the data lead (D_X or D_R) from the system data bus. A device (both transmit and receive channels) may be deactivated in either control mode by powering down the device. Both channels are always powered down together.

Encoding

The VF signal to be encoded is input on the VF_X lead. An internal switch samples the signal and the hold function is performed by the external capacitor connected to the $CAP1_X$ and $CAP2_X$ leads. The sampling and conversion is synchronized with the

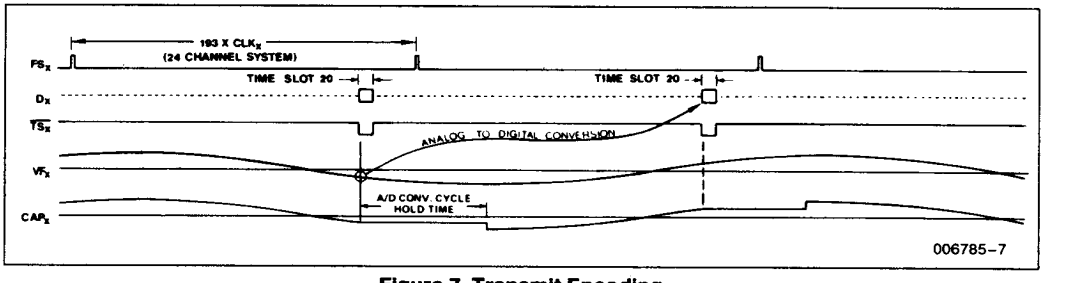


Figure 7. Transmit Encoding

transmit timeslot. The PCM word is then output on the D_X lead at the proper timeslot occurrence of the following frame. The A/D converter saturates at approximately ±2.2 volts RMS (±3.1 volts peak).

Decoding

The PCM word is fetched by the D_R lead from the PCM highway at the proper timeslot occurrence. The decoded value is held on an internal sample and hold capacitor. The buffered non-return to zero output signal on the VF_R lead has a dynamic range of approximately ±2.2 volts RMS (±3.1 volts peak).

Signaling

The duration of the FS_X and FS_R pulses defines whether a frame is an information frame or a signaling frame:

- A frame synchronization pulse which is a full clock period in duration (CLK_X period for FS_X, CLK_R period for FS_R) designates a non-signaling frame.
- A frame synchronization pulse which is two full clock periods in duration (two CLK_X periods for FS_X, two CLK_R periods for FS_R) designates a signaling frame.

On the encoding side, when the FS_X pulse is widened, the 8th bit of the PCM word will be replaced by the value on the SIG_X input at the time when the 8th bit is output on the D_X lead.

On the decoding side, when the FS_R pulse is widened, the 8th bit of the PCM word is detected and transmitted on the SIG_R lead. That output is latched until the next receiving signaling frame.

The remaining 7 bits are decoded according to the value given in the CCITT G733 recommendation. The SIG_R lead is reset to a TTL low level whenever the Codec is in the power-down state.

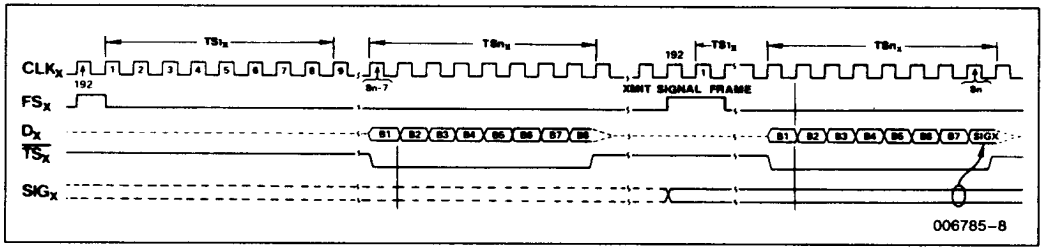


Figure 8. Transmit 8th Bit Signaling

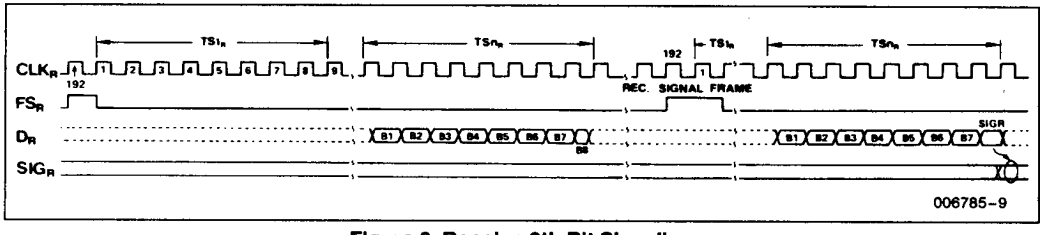


Figure 9. Receive 8th Bit Signaling

T1 Framing

The Codec will accept the standard D3/D4 framing format of 193 clock pulses per frame (equivalent to CLK_X, CLK_R of 1.544 Mb/s). However, the 193rd bit may be blanked (equivalent to CLK_X, CLK_R of 1.536 Mb/s) if desired.

Standby Mode—Power Down

To minimize power consumption and heat dissipation a standby mode is provided where all Codec functions are disabled except for D_C and CLK_C leads. These allow the Codec to be reactivated. In the microcomputer mode the Codec is placed into standby by loading a control word (D_C) with a "1" in bits 1 and 2 locations. In the direct mode when D_C is brought high, the all "1's" control word is internally transferred to the control register, invoking the standby condition.

While in the standby mode, the D_X output is actively held in a high impedance state to guarantee that the PCM bus will not be driven. The SIG_R output is held low to provide a known condition and remains this way upon activation until it is changed by signaling.

The power consumption in the standby mode is typically 33 mW.

Power-On Clear

Whether the device is used in the direct or microcomputer mode, an internal reset (power-on clear) is generated, forcing the device into the power down state, when power is supplied by any of the following methods. (1) Device power supplies are turned on in a system power-up situation where either V_{CC} or V_{DD} is applied last. (2) A large supply transient causes either of the two positive supplies to drop to less than approximately 2 volts. (3) A board containing Codecs is plugged into a "hot" system where V_{CC} or V_{DD} is the last contact made. It may be necessary to trim back the edge connector pins or fingers on V_{CC} or V_{DD} relative to the other supply to guarantee that the power-on clear will operate properly when a board is plugged into a "hot" system. Furthermore, the Codec will inhibit activity on $\overline{TS}x$ and D_X during the application of power supplies.

The device is also tolerant of transients in the negative supply (V_{BB}) so long as V_{BB} remains more negative than -3.5 volts. V_{BB} transients which exceed this level should be detected and followed by a system reinitialization.

Precision Voltage Reference for the D/A Converter

The voltage reference is generated on the chip and is calibrated during the manufacturing process. The technique uses the difference in sub-surface charge density between two suitably implanted MOS devices to derive a temperature stable and bias stable reference voltage.

A gain setting op amp, programmed during manufacturing, "trims" the reference voltage source to the final precision voltage reference value provided to the D/A converter. The precision voltage reference determines the initial gain and dynamic range characteristics described in the A.C. Transmission Specification section.

μ-Law Conversion

μ-law represents a particular implementation of a piece-wise linear approximation to a logarithmic compression curve which is:

$$F(x) = \mathrm{Sgn}(x)\frac{\ln(1+\mu|x|)}{\ln(1+\mu)}\ 0 \le |x| \le 1$$

where x = input signal

Sgn(x) = sign of input signal

μ = 255 (defined by AT & T)

The 2910A $\mu = 255$ law Codec uses a 15 segment approximation to the logarithmic law. Each segment consists of 16 steps. In adjacent segments the step sizes are in a ratio of two to one. Within each segment the step size is constant except for the first step of the first segment of the encoder, as indicated in the attached table. The output levels are midway between the corresponding decision levels. The output levels y_n are related to the input levels x_n by the expression:

$$y_n = \frac{x_n + x_{n+1}}{2} \text{ for } 1 \le n \le 127$$

$$y_0 = x_0 = 0 \text{ for } n = 0$$

These relationships are implicit in the following table.

Theoretical μ-Law—Positive Input Values (for Negative Input Values, Invert Bit 1)

1 Segment Number	2 No. of Steps x Step Size	3 Value at Segment End Points	4 Decision Value Number n	5 Decision Value x_n(1)	6 PCM Word(3) MSB 1 2 3 4 5 6 7 8 LSB	7 Normalized Value at Decoder Output y_n(4)	8 Decoder Output Value Number
		8159(5)	(128)	(8159)			
			127	7903	1 0 0 0 0 0 0 0	8031	127
8	16 x 256				(see Note 2)		
			113	4319	1 0 0 0 1 1 1 1	4191	112
		4063	112	4063			
7	16 x 128				(see Note 2)		
			97	2143	1 0 0 1 1 1 1 1	2079	96
		2015	96	2015			
6	16 x 64				(see Note 2)		
			81	1055	1 0 1 0 1 1 1 1	1023	80
		991	80	991			
5	16 x 32				(see Note 2)		
			65	511	1 0 1 1 1 1 1 1	495	64
		479	64	479			
4	16 x 16				(see Note 2)		
			49	239	1 1 0 0 1 1 1 1	231	48
		223	48	223			
3	16 x 8				(see Note 2)		
			33	103	1 1 0 1 1 1 1 1	99	32
		95	32	95			
2	16 x 4				(see Note 2)		
			17	35	1 1 1 0 1 1 1 1	33	16
		31	16	31			
	15 x 2				(see Note 2)		
			2	3			
1 ↓					1 1 1 1 1 1 1 0	2	1
	1 x 1		1	1	1 1 1 1 1 1 1 1		
			0	0		0	0

NOTES:
1. 8159 normalized value units correspond to the value of the on-chip voltage reference.
2. The PCM word corresponding to positive input values between two successive decision values numbered n and n+1 (see column 4) is (255−n) expressed as a binary number.
3. The PCM word on the highways is the same as the one shown in column 6.
4. The voltage output on the VF_R lead is equal to the normalized value given in the table, augmented by an offset. The offset value is approximately 15 mV.
5. x_{128} is a virtual decision value.

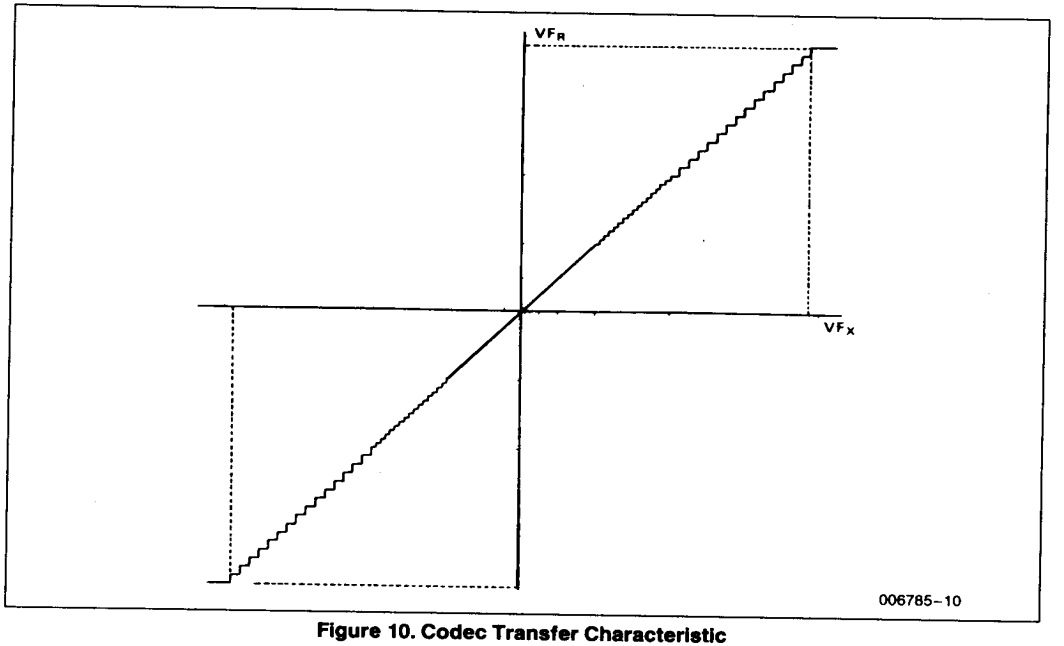


Figure 10. Codec Transfer Characteristic

During signaling frames, a 7-bit transfer characteristic is implemented in the decoder. This characteristic is derived from the decoder values in the attached table by assuming a value of "1" for the LSB (8th bit) and shifting the decoder transfer characteristics one half-step away from the origin. For example, the maximum decoder output level for signaling frames has normalized value 7903, whereas it has value 8031 in normal (non-signaling) frames.

APPLICATIONS

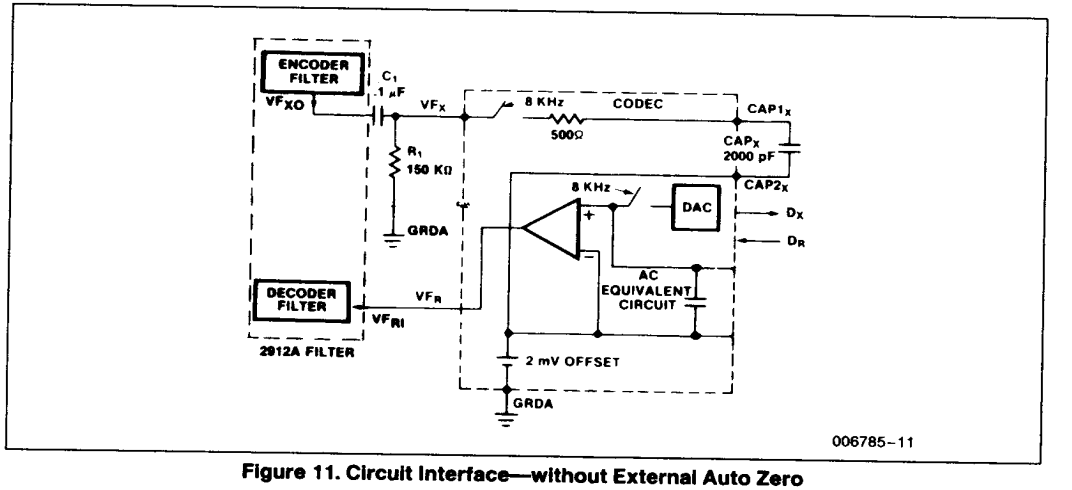


Figure 11. Circuit Interface—without External Auto Zero

Holding Capacitor

For an 8 KHz sampling system the transmit holding capacitor CAP_X should be 2000 pF ±20%.

Auto Zero

The 2910A contains a transparent on-chip auto zero plus a device pin for implementing a sign-bit driven external auto zero feedback loop. The on-chip auto zero reduces the input offset voltage of the encoder (VF_X) to less than 3 mV. For most telephony applications, this input offset is perfectly acceptable, since it insures the encoder is biased in the lower 25% of the first segment.

Where lower input offset is required the external auto zero loop may be used to bias the encoder exactly at the zero crossing point. The consequence of the external auto zero loop, aside from extra components, is the addition of the dithering auto-zero signal to the input signal, resulting in slightly higher idle channel noise (approximately 2dB) than when the external loop is not used. Consequently, where the application permits, it is recommended that the external auto zero loop not be used. When not used, the AUTO pin should float.

The circuit interface with auto zero drawing shows a possible connection between the VF_X and AUTO leads with the recommended values of $C_1 = 0.3\ \mu F$, $R_1 = 150\ K\Omega$, $R_2 = 330\ K\Omega$, and $R_3 = 470\ K\Omega$.

Filters Interface

The filters may be interfaced as shown in the circuit interface diagrams. Note that the output pulse stream is of the non-return-to-zero type and hence requires the (sin x)/x correction provided by the 2912A filter.

D_X Buffering

For higher drive capability or increased system reliability it may be desirable that the D_X output of a group of Codecs be buffered from the system PCM bus with an external three-state or open collector buffers. A buffer can be enabled with the appropriate Codec generated $\overline{TS}x$ signal or signals. $\overline{TS}x$ signal may also be used to activate external zero code suppression logic, since the occurrence of an active state of any $\overline{TS}x$ implies the existence of PCM voice bits (as opposed to transparent data bits) on the bus.

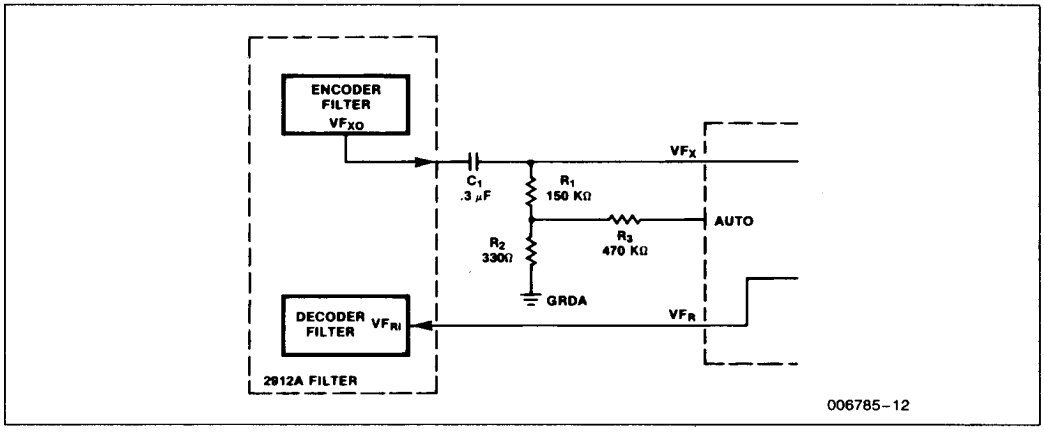


Figure 12. Circuit Interface—with External Auto Zero

5

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −10°C to +80°C
Storage Temperature ..... −65°C to +150°C
All Input or Output Voltages with Respect to V_{BB} ..... −0.3V to +20V
V_{CC}, V_{DD}, GRDD, and GRDA with Respect to V_{BB} ..... −0.3V to +20V
Power Dissipation 1.35W

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS

$T_A = 0°C$ to $+70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GRDA = 0V, GRDD = 0V, unless otherwise specified

DIGITAL INTERFACE

Symbol	Parameter	Limits			Units	Test Conditions
		Min	Typ(1)	Max		
I_{IL}	Low Level Input Current			10	μA	$V_{IN} < V_{IL}$
I_{IH}	High Level Input Current			10	μA	$V_{IN} > V_{IH}$
V_{IL}	Input Low Voltage			0.6	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	D_X, I_{OL} = 4.0 mA SIG_R, I_{OL} = 0.5 mA $\overline{TS}x$, I_{OL} = 3.2 mA, Open Drain PDN, I_{OL} = 1.6 mA, Open Drain
V_{OH}	Output High Voltage	2.4			V	D_X, I_{OH} = 15 mA SIG_R, I_{OH} = 0.08 mA

ANALOG INTERFACE

Symbol	Parameter	Limits			Units	Test Conditions
		Min	Typ(1)	Max		
Z_{AI}	Input Impedance when Sampling, VF_X	125	300	500	Ω	in Series with CAP_X to GRDA, $-3.1V < V_{IN} < 3.1V$
Z_{AO}	Small Signal Output Impedance, VF_R	100	180	300	Ω	$-3.1V < V_{OUT} < 3.1V$
V_{OR}	Output Offset Voltage at VF_R			±50	mV	all "1s" code sent to D_R
V_{IX}	Input Offset Voltage at VF_X			±5	mV	VF_X Voltage Required to Produce all "1s" Code at D_X
V_{OL}	Output Low Voltage at AUTO		V_{BB}	(V_{BB} + 2)	V	400 KΩ to GRDA
V_{OH}	Output High Voltage at AUTO	(V_{CC} − 2)	V_{CC}		V	400 KΩ to GRDA

POWER DISSIPATION

Symbol	Parameter	Limits			Units	Test Conditions
		Min	Typ(1)	Max		
I_{DDO}	Standby Current		0.7	1.1	mA	Auto Output = Open Clock Frequency = 2.048 MHz
I_{CCO}	Standby Current		4	7.0	mA	
I_{BBO}	Standby Current		1	2.5	mA	
I_{DDI}	Operating Current		11	16	mA	
I_{CCI}	Operating Current		13	21	mA	
I_{BBI}	Operating Current		4	6.0	mA	

NOTE:
1. Typical values are for T_A = 25°C and nominal power supply values.

A.C. CHARACTERISTICS

$T_A = 0°C$ to $+70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GRDA = 0V, GRDD = 0V, unless otherwise specified

TRANSMISSION

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ(1)	Max		
S/D	Signal/Tone Distortion Ratio,					VF_X = 1.02 KHz, Sinusoid
	C-Message Weighted	36			dB	-30 dBm0 ≤ VF_X ≤ 0 dBm0
	Half Channel	30			dB	-40 dBm0 ≤ VF_X < -30 dBm0
	(See Figure 1)	27			dB	-45 dBm0 ≤ VF_X < -40 dBm0
ΔG						VF_X = 1.02 KHz, Sinusoid
	Gain Tracking Deviation		±0.25	±0.30	dB	-37 dBm0 ≤ VF_X ≤ +3 dBm0
	Half Channel(2)		±0.60	±0.70	dB	-50 dBm0 ≤ VF_X < -37 dBm0
	Reference Level 0 dBm0		±1.5	±1.8	dB	-55 dBm0 ≤ VF_X < -50 dBm0
ΔG_V	ΔG Variation with Supplies		±0.0002	±0.0004	dB/mV	-37 dBm0 ≤ VF_X ≤ +3 dBm0
	Half Channel		±0.0004	±0.0008	dB/mV	-50 dBm0 ≤ VF_X < -37 dBm0
ΔG_T	ΔG Variation with Temperature		±0.001	±0.002	dB/°C	-37 dBm0 ≤ VF_X ≤ +3 dBm0
	Half Channel		±0.002	±0.005	dB/°C	-50 dBm0 ≤ VF_X < -37 dBm0
N_{IC1}	Idle Channel Noise, C-Message Weighted		2	7	dBrnc0	No Signaling(3)
N_{IC2}	Idle Channel Noise, C-Message Weighted		10	13	dBrnc0	with 6th and 12th Frame Signaling(3)
N_{IC3}	Idle Channel Noise, C-Message Weighted		14	18	dBrnc0	with 1 KHz Sign Bit Toggle
HD	Harmonic Distortion (2nd or 3rd)		-48	-44	dB	VF_X = 1.02 KHz, 0 dBm0; Measured at Decoder Output VF_R
IMD	Intermodulation Distortion					4-Tone Stimulus in Accordance
	2nd Order			-45	dB	with BSTR PUB 41009
	3rd Order			-55	dB	

NOTES:
1. Typical values are for T_A = 25°C and nominal supply values.
2. Measured in one direction, either decoder or encoder and an ideal device, at 23°C, nominal supplies.
3. If the external auto-zero is used N_{IC1} has a typical value of 8 dBrnc0 and N_{IC2} has a typical value of 13 dBrnc0.
4. D_R of Device Under Test (D.U.T.) driven with repetitive digital word sequence specified in CCITT recommendation G.711. Measurement made at VF_R output.
5. With the D.C. method the positive and negative clipping levels are measured and A_{IR} is calculated. With the A.C. method a sinusoidal input signal to VF_X is used where A_{IR} is measured directly.

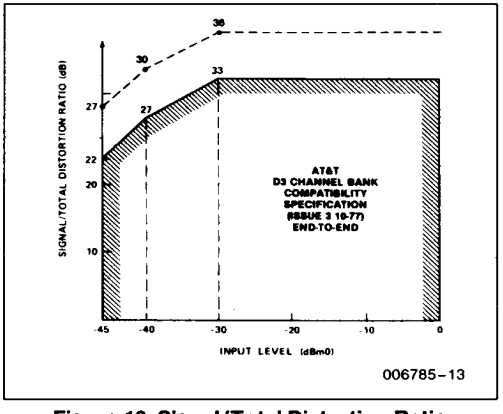


Figure 13. Signal/Total Distortion Ratio (Half-Channel)

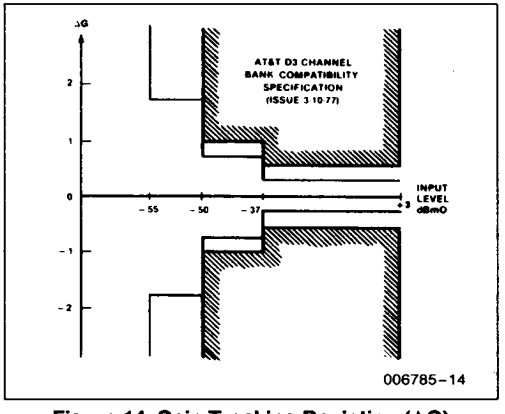


Figure 14. Gain Tracking Deviation (ΔG) (Half-Channel)

A.C. CHARACTERISTICS

$T_A = 0°C$ to $+70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GRDA = 0V, GRDD = 0V, unless otherwise specified (Continued)

GAIN AND DYNAMIC RANGE

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ(1)	Max		
DmW	Digital Milliwatt Response	5.53	5.63	5.73	dBm	23°C, Nominal Supplies(4)
DmW_T	DmW_O Variation with Temperature		−0.001	−0.002	dB/°C	Relative to 23°C(4)
DmW_S	DmW_O Variation with Supplies			±0.07	dB	Supplies ±5%(4)
A_{IR}	Input Dynamic Range	2.17	2.20	2.23	V_{RMS}	Using D.C. and A. C. Tests(5) 23°C, Nominal Supplies
A_{IRT}	Input Dynamic Range with Temperature			−0.5	mV_{RMS}/°C	Relative to 23°C
A_{IRS}	Input Dynamic Range with Supplies			±18	mV_{RMS}	Supplies ±5%
A_{OR}	Output Dynamic Range, VF_R	2.13	2.16	2.19	V_{RMS}	23°C, Nominal Supplies
A_{ORT}	A_{OR} Variation with Temperature			−0.5	mV_{RMS}/°C	Relative to 23°C
A_{ORS}	A_{OR} Variation with Supplies			±18	mV_{RMS}	Supplies ±5%

SUPPLY REJECTION AND CROSSTALK

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ(1)	Max		
$PSRR_1$	V_{DD} Power Supply Rejection Ratio	45			dB	Decoder Alone(2)
$PSRR_2$	V_{BB} Power Supply Rejection Ratio	35			dB	Decoder Alone(2)
$PSRR_3$	V_{CC} Power Supply Rejection Ratio	50			dB	Decoder Alone(2)
$PSRR_4$	V_{DD} Power Supply Rejection Ratio	50			dB	Encoder Alone(3)
$PSRR_5$	V_{BB} Power Supply Rejection Ratio	45			dB	Encoder Alone(3)
$PSRR_6$	V_{CC} Power Supply Rejection Ratio	50			dB	Encoder Alone(3)
CT_R	Crosstalk Isolation, Receive Side	75	80		dB	(Note 4)
CT_T	Crosstalk Isolation, Transmit Side	75	80		dB	(Note 5)
CAPX	Input Sample and Hold Capacitor	1600	200	2400	pF	

NOTES:
1. Typical values are for $T_A = 25°C$ and nominal power supply values.
2. D.U.T. decoder; impose 200 mV_{P-P}, 1.02 KHz on appropriate supply; measurement made at decoder output; decoder in idle channel conditions.
3. D.U.T. encoder; impose 200 mV_{P-P}, 1.02 KHz on appropriate supply; measurement made at encoder output; encoder in idle channel conditions.
4. VF_X of D.U.T. encoder = 1.02 KHz, 0 dBm0. Decoder under quiet channel conditions; measurement made at decoder output.
5. VF_X = 0 Vrms. Decoder = 1.02 KHz, 0 dBm0. Encoder under quiet channel conditions; measurement made at encoder output.

A.C. CHARACTERISTIC—TIMING SPECIFICATION(1)

$T_A = 0°C$ to $+70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GRDA = 0V, GRDD = 0V, unless otherwise specified

CLOCK SECTION

Symbol	Parameter	Limits		Units	Comments
		Min	Max		
t_{CY}	Clock Period	485		ns	CLK_X, CLK_R (2.048 MHz Systems), CLK_C
t_r, t_f	Clock Rise and Fall Time	0	30	ns	CLK_X, CLK_R, CLK_C
t_{CLK}	Clock Pulse Width	215		ns	CLK_X, CLK_R, CLK_C
t_{CDC}	Clock Duty Cycle ($t_{CLK} \div t_{CY}$)	45	55	%	CLK_X, CLK_R

TRANSMIT SECTION

Symbol	Parameter	Limits		Units	Comments
		Min	Max		
t_{VFX}	Analog Input Conversion	20		Timeslot	from Leading Edge of Transmit Timeslot (2)
t_{DZX}	Data Enabled on TS Entry	50	180	ns	$0 < C_{LOAD} < 100$ pF
t_{DHX}	Data Hold Time	80	230	ns	$0 < C_{LOAD} < 100$ pF
t_{HZX}	Data Float on TS Exit	75	245	ns	$C_{LOAD} = 0$
t_{SON}	Timeslot X to Enable	30	220	ns	$0 < C_{LOAD} < 100$pF
t_{SOFF}	Timeslot X to Disable	70	225	ns	$C_{LOAD} = 0$
t_{SS}	Signal Setup Time	0		ns	Relative to Bit 7 Falling Edge
t_{SH}	Signal Hold Time	100		ns	Relative to Bit 8 Falling Edge
t_{FSD}	Frame Sync Delay	15	150	ns	

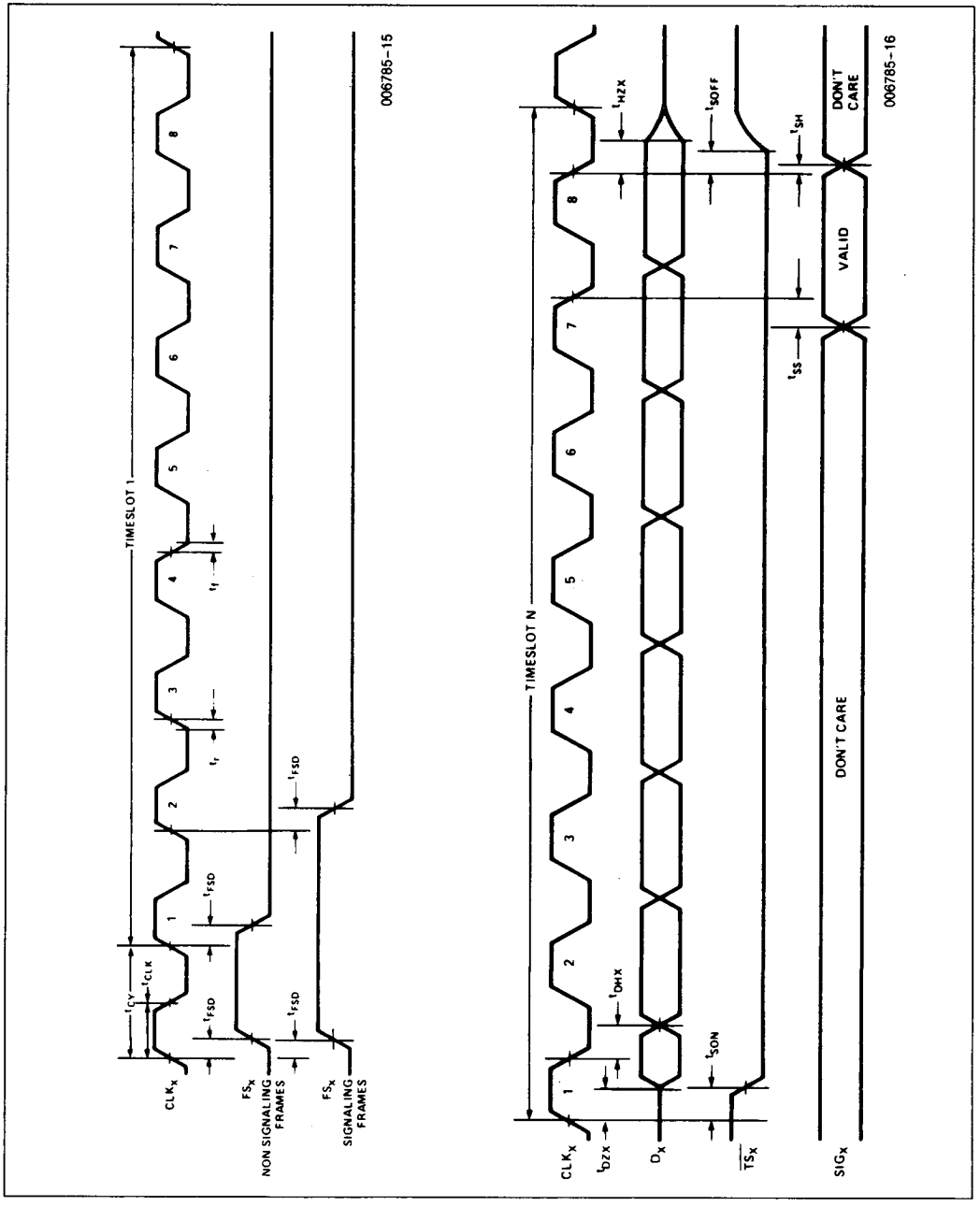
RECEIVE AND CONTROL SECTIONS

Symbol	Parameter	Limits		Units	Comments
		Min	Max		
t_{VFR}	Analog Output Update	9 1/16	9 1/16	Timeslot	from Leading Edge of the Channel Timeslot
t_{DSR}	Receive Data Setup	20		ns	
t_{DHR}	Receive Data Hold	60		ns	
t_{SIGR}	SIG_R Update		1	μs	from Trailing Edge of the Channel Timeslot
t_{FSD}	Frame Sync Delay	15	150	ns	
t_{DSC}	Control Data Setup	115		ns	Microcomputer Mode Only
t_{DHC}	Control Data Hold	115		ns	Microcomputer Mode Only

NOTES:
1. All timing parameters referenced to 1.5V, except t_{HZX} and t_{SOFF} which reference to high impedance state.
2. The 20 timeslot minimum insures that the complete A/D conversion will take place under any combination of receive interrupt or asynchronous operation of the Codec. If the transmit channel *only* is operated, the A/D conversion can be completed in a minimum of 11 timeslots. Refer to the Codec Control General Requirement section for instructions on setting a channel in an idle condition.

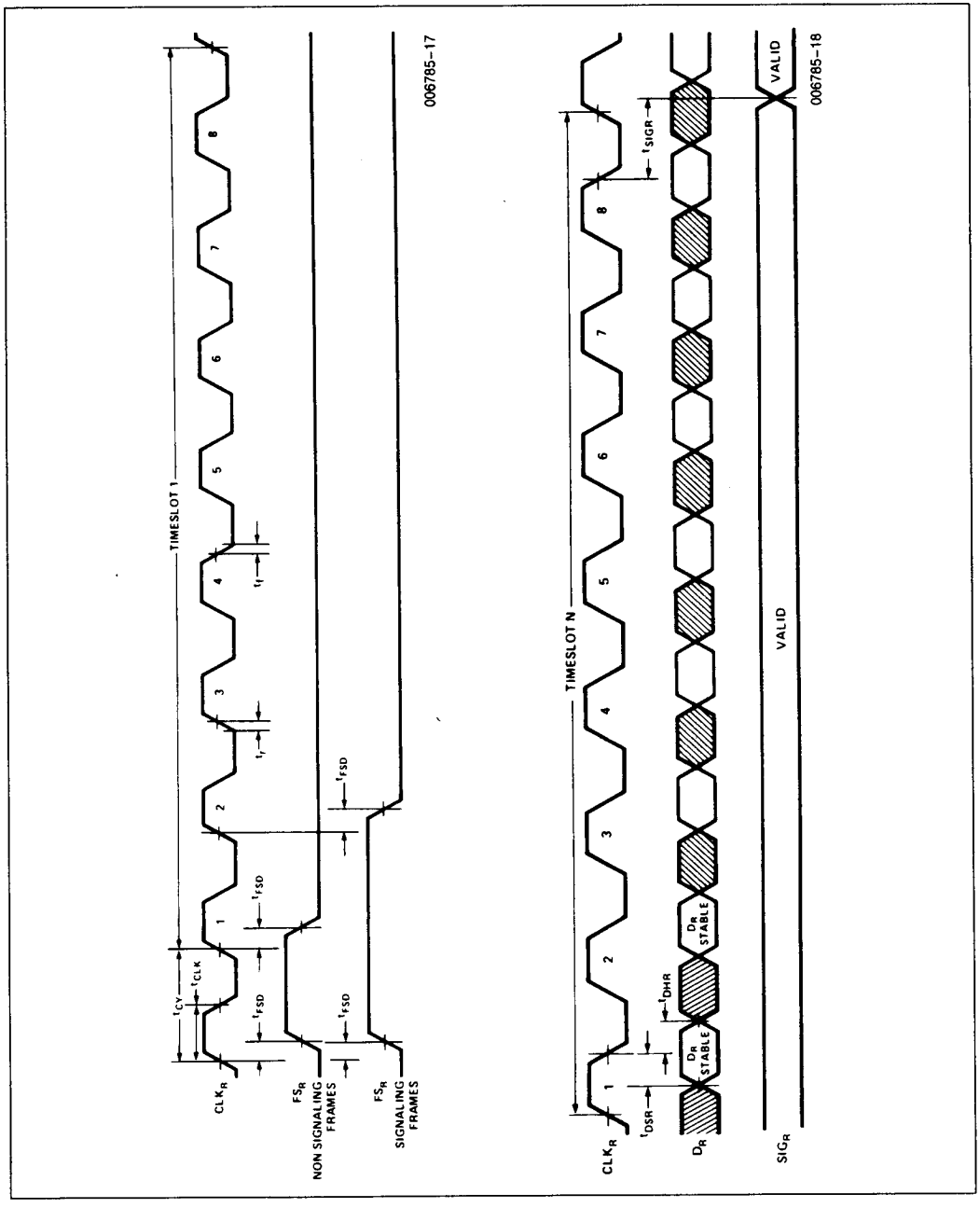
TIMING WAVEFORMS

TRANSMIT TIMING



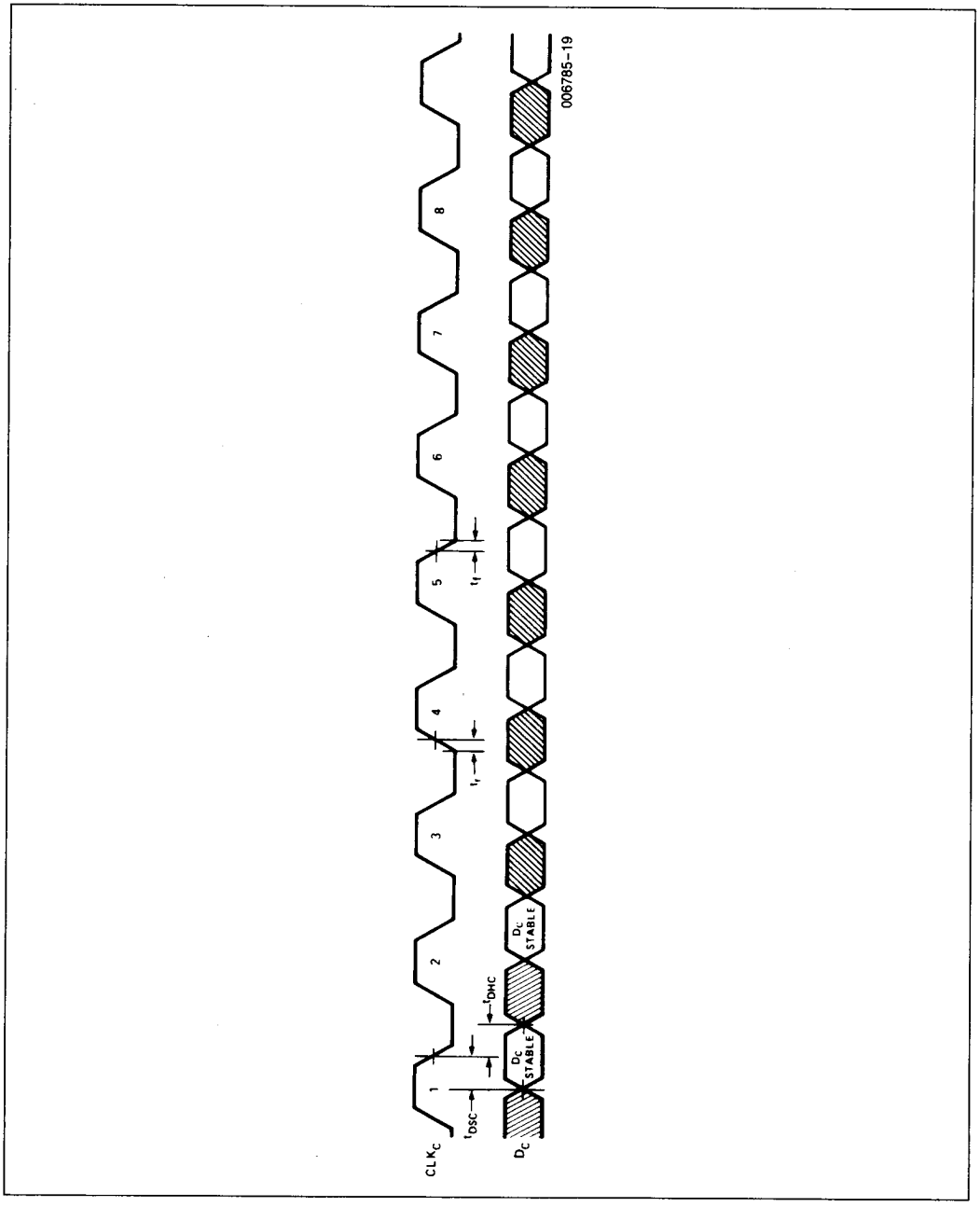
TIMING WAVEFORMS (Continued)

RECEIVE TIMING



TIMING WAVEFORMS (Continued)

CONTROL TIMING



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