REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
C	Added CAGE number 1FN41 and 34335 to the drawing as approved sources of supply. Added vendor CAGE number 18324 to device types 01ZX, 02ZX, and 03ZX, with changes to margin test methods A and B. Added device type 07 to the drawing for vendor CAGE number 65579 with changes to table I. Deleted figure 5 and table III. Also, deleted program method column from 6.6. Editorial changes throughout.	1989 OCT 30	

CURRENT CAGE CODE 67268

REV																									
SHEET																									
REV																									
SHEET																									
REV STATUS OF SHEETS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C									
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15									

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY James E. Jamison

CHECKED BY Charles Reusing

APPROVED BY

DRAWING APPROVAL DATE 10 JANUARY 1986

REVISION LEVEL C

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, 65,536 BIT (8K X 8) CMOS UV ERASABLE PROM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	14933	85102

SHEET 1 OF 15

DESC FORM 193-1
SEP 87

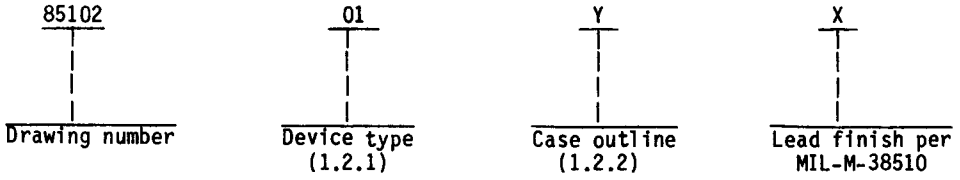
* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60912

5962-E1282

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit	Access
01	27C64-25	8K x 8-bit CMOS UVEPROM	250 ns
02	27C64-35	8K x 8-bit CMOS UVEPROM	350 ns
03	27C64-20	8K x 8-bit CMOS UVEPROM	200 ns
04	27C64-90	8K x 8-bit CMOS UVEPROM	90 ns
05	27C64-12	8K x 8-bit CMOS UVEPROM	120 ns
06	27C64-15	8K x 8-bit CMOS UVEPROM	150 ns
07	57C64-70	8K x 8-bit CMOS UVEPROM	70 ns

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline 1/
Y	D-10 (28-pin, 1.490" x .610" x .232"), dual-in-line package
Z	C-12 (32-terminal, .560" x .458" x .120"), rectangular chip carrier package

1.3 Absolute maximum ratings.

Storage temperature range	-65°C to +150°C
All input or output voltages with respect to ground	-2.0 V dc to +7.0 V dc 2/
Voltage on A_9 with respect to ground	-2.0 V dc to +13.5 V dc 2/
V_{PP} supply voltage with respect to ground during programming	-2.0 V dc to +14.0 V dc 2/
Maximum power dissipation (P_D): 3/	
Device types 01 and 03	170 mW
Device type 02	140 mW
Device types 04, 05, 06, and 07	550 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases Y and Z	See MIL-M-38510, appendix C
Junction temperature (T_J)	+150°C

1/ Lid shall be transparent to permit ultraviolet light erasure.
2/ Minimum dc input voltage is -0.5 V dc, during transitions, the inputs may undershoot to -2.0 V dc for periods less than 20 ns.
3/ Must withstand the added P_D due to short-circuit test; e.g., I_{OS}.

1.4 Recommended operating conditions.

Case operating temperature range (T_C) - - -	-55°C to +125°C
Input low voltage ±10% supply (V_{IL}) - - - -	-0.5 V dc to +0.8 V dc
Input high voltage ±10% supply (V_{IH})- - - -	2.0 V dc to V_{CC} +0.5 V dc
Supply voltage range(V_{CC}) - - - - - - - - - -	4.5 V dc to 5.5 V dc

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth tables. The truth tables shall be as specified on figure 2.

3.2.2.1 Unprogrammed or erased devices. The truth table for unprogrammed devices shall be as specified on figure 2.

3.2.2.2 Program devices. The requirements for supplying programmed devices are not a part of this drawing.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Input load current	I_{LI}	V_{IN} = 5.5 V or GND 1/	1, 2, 3	All	-10	10	µA
Output leakage current	I_{LO}	V_{OUT} = 5.5 V or GND	1, 2, 3	All	-10	10	µA
Operating current, TTL inputs 2/	I_{CC} TTL	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}, O_0-O_7 = 0 mA, f = 5 MHz min	1, 2, 3	04		75	mA
				01, 03		30	
				02		25	
				05		65	
				06		60	
				07		65	
Operating current 3/	I_{CC} CMOS	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}, O_0-O_7 = 0 mA, f = 5 MHz min	1, 2, 3	04		60	mA
				01,02, 03		10	
				05		55	
				06		50	
				07		70	
Standby current, TTL inputs 2/	I_{SB} TTL	$\overline{OE}$ = $\overline{CE}$ = V_{IH}, f = 0 MHz, O_0-O_7 = disabled	1, 2, 3	01,02, 03		1	mA
				04,05, 06		2	
				07		15	
Standby current, CMOS inputs 4/	I_{SB} CMOS	$\overline{OE}$ = $\overline{CE}$ = V_{IH}, f = 0 MHz, O_0-O_7 = disabled	1, 2, 3	01,02, 03		140	µA
				04,05, 06		200	
				07		500	
V_{PP} read current 5/	I_{PP}	V_{PP} = V_{CC}	1, 2, 3	All		100	µA
Input low voltage ±10% supply	V_{IL}	V_{PP} = V_{CC}	1, 2, 3	All	-0.5 6/	0.8	V
Input high voltage ±10% supply	V_{IH}	V_{PP} = V_{CC}	1, 2, 3	All	2.0	V_{CC} +0.5 6/	V
Output low voltage	V_{OL}	V_{IL} = 0.8 V, V_{IH} = 2.0 V, I_{OL} = 2.1 mA	1, 2, 3	01-06		0.45	V
				07		0.4	
Output high voltage	V_{OH}	V_{IL} = 0.8 V, V_{IH} = 2.0 V, I_{OH} = -400 µA	1, 2, 3	All	2.4		V
Output short-circuit current	I_{OS} 6/		1, 2, 3	All		100	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$, unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Vpp read voltage 7/	V_{PP}		1, 2, 3	All	V_{CC} -.7	V_{CC}	V
Input capacitance	C_{IN}	V_{IN} = 0 V See 4.3.1c	4	All		10	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V See 4.3.1c	4	All		12	
Functional tests		See 4.3.1e	7, 8	All			
Address to output delay 8/ 9/	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	9, 10, 11	04		90	ns
				01		250	
				02		350	
				03		200	
				05		120	
				06		150	
				07		70	
$\overline{CE}$ to output delay 8/ 9/	t_{CE}	$\overline{OE}$ = V_{IL}	9, 10, 11	04		90	ns
				01		250	
				02		350	
				03		200	
				05		120	
				06		150	
				07		70	
$\overline{OE}$ to output delay 8/ 9/	t_{OE}	$\overline{CE}$ = V_{IL}	9, 10, 11	04, 07		30	ns
				01		100	
				02		120	
				03		75	
				05		35	
				06		45	
$\overline{OE}$ high to output float 8/ 9/	t_{DF} 6/	$\overline{CE}$ = V_{IL}	9, 10, 11	04, 07	0	25	ns
				01, 03	0	55	
				02	0	105	
				05	0	35	
				06		40	
Output hold from addresses, $\overline{CE}$ or $\overline{OE}$ whichever occurred first 8/ 9/	t_{OH} 6/	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	9, 10, 11	01-06	0		ns
				07	10		

See footnotes on next page.

1/ Pins not tested are all at GND and 5.5 V respectively.
2/ TTL inputs: Specify V_{IL} and V_{IH} levels.
3/ CMOS inputs: GND ±0.2 V to V_{CC} ±0.2 V.
4/ $\overline{CE}$ = V_{CC} ±0.2 V. All other inputs can have any value within specified limits.
5/ Maximum active power usage is the sum of I_{PP} + I_{CC}.
6/ If not tested, shall be guaranteed to the limits specified in table I.
7/ V_{PP} may be connected directly to V_{CC} except during programming.
8/ Outputs shall be loaded in accordance with figure 3.
9/ See figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in MIL-Bul-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.10.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4 herein.

3.10.2 Programmability of EPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5.

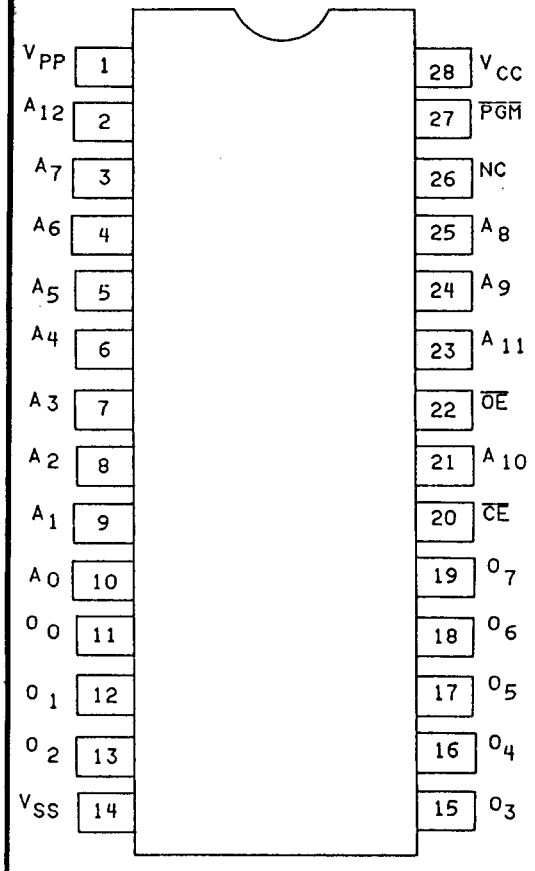
3.10.3 Verification of erasure of programmability of EPROMS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

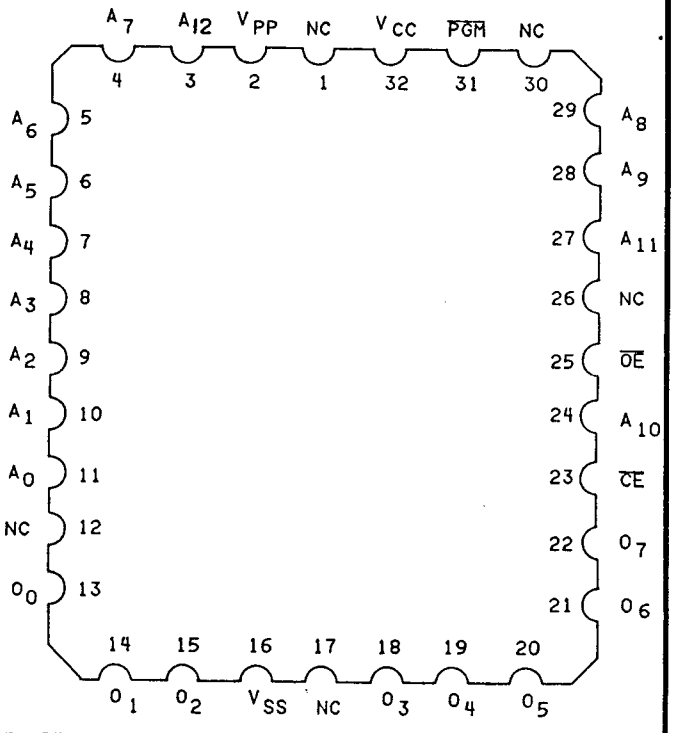
Devices types 01-07

Case Y



Devices types 01-07

Case Z



Pin names

A_0 - A_{12}	Addresses
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
O_0 - O_7	Outputs
$\overline{PGM}$	Program pin (method A only)

FIGURE 1. Terminal connections.

Read modes (see notes 1 and 2)

Mode Pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	D_{OUT}
Output disable	V_{IL}	V_{IH}	V_{IH}	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	High Z

Programming modes (see notes 1 and 2)

Mode Pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	A_0	V_{PP}	V_{CC}	Outputs
Intelligent programming	V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP}	6.0 V See note 3	D_{IN}
Program verify	V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	6.0 V See note 3	D_{OUT}
Program inhibit	V_{IH}	X	X	X	X	V_{PP}	V_{CC}	High Z
Intelligent identifier --manufacturer See note 4	V_{IL}	V_{IL}	V_{IL} / V_{IH}	V_H	V_{IL}	V_{CC}	V_{CC}	89 H 8F H 01 H 15 H 1F H 23 H
Intelligent identifier See note 4	V_{IL}	V_{IL}	V_{IH}	V_H	V_{IH}	V_{CC}	V_{CC}	07 H C2 H 0B H 91 H 15 H

NOTES:
1. X can be V_{IL} or V_{IH}.
2. V_H = 12.0 V ±0.5 V.
3. V_{CC} = 6.0 V ±0.25 V.
4. A_1 - A_8, A_{10} - A_{12} = V_{IL}.

FIGURE 2. Truth tables.

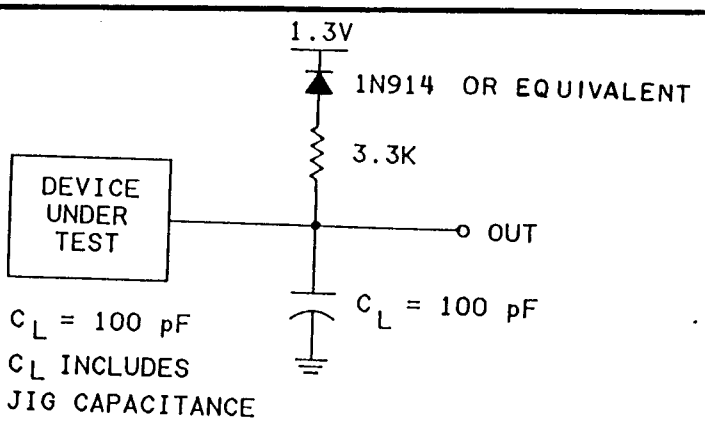
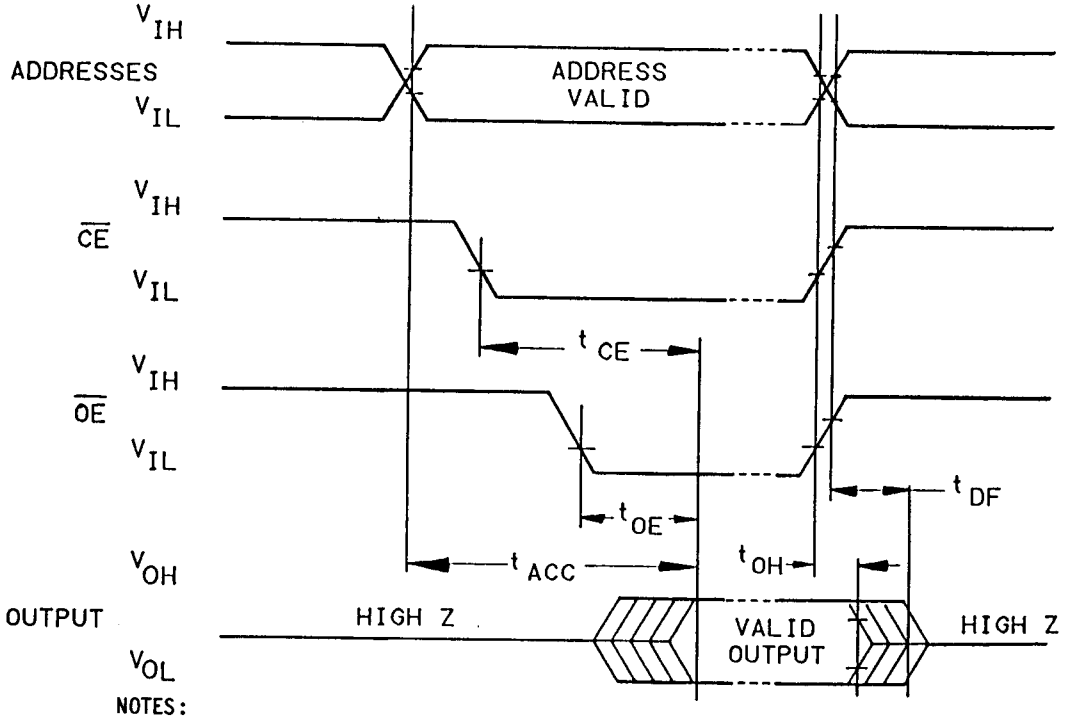


FIGURE 3. Output load.



NOTES:
1. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
3. AC characteristics tested at V_{IH} = 2.4 V and V_{IL} = 0.45 V, timing measurement made at 2.0 V and .8 V levels.

FIGURE 4. AC waveforms.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. The percent defective allowable (PDA) shall be as specified in MIL-M-38510.

d. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps.

Margin test method A.

(1) Program greater than 95 percent of the bit locations, including the slowest programming cell (see 3.10.2). The remaining cells shall provide a worst case speed pattern.

(2) Bake, unbiased, for 72 hours at +140°C, or at 72 hours at +225°C (unassembled devices only).

(3) Perform a margin test using Vm = +5.9 V (loose timing, room temperature).

(4) Perform dynamic burn-in in accordance with MIL-STD-883.

(5) Perform a margin test at V_m = +5.9 V.

(6) Perform 100 percent electrical testing at +25°C, +125°C, and -55°C.

(7) Final quality assurance procedures.

(8) Steps 1 through 3 may be performed at wafer level.

(9) The maximum unbiased bake temperature shall not exceed +200°C for packaged devices or +300°C for unassembled devices.

Margin test method B.

(1) Program at +25°C 100 percent of the bits.

(2) Bake, unbiased, for 24 hours at +250°C, or 72 hours at +225°C (unassembled devices only).

(3) Perform margin test at V_m = 5.9 V.

(4) Erase (see 3.10.1).

(5) Perform interim electrical tests in accordance with table II.

(6) Program with checkerboard pattern and verify (see 3.10.2).

(7) Perform dynamic burn-in (see 4.2a).

(8) One-hundred percent test at +25°C (group A, subgroups 1 and 7). V_m = 5.9 V with loose timing, apply PDA.

(9) Perform remaining final electrical subgroups and group A testing.

(10) Erased, devices may be submitted for groups B, C, and D at this time.

(11) Verify erasure (see 3.10.3). Steps 1 through 4 are performed at wafer level.

(12) The maximum unbiased bake temperature shall not exceed +200°C for packaged devices or +300°C for unassembled devices.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

d. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified (except devices submitted for groups C and D testing).

e. Subgroups 7 and 8 shall consist of verifying the EPROM pattern specified.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

(4) All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified.

4.4 Erasing procedure. The recommended erasure procedure for the device is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (A). The integrated dose (i.e. UV intensity times exposure time) for erasure should be a minimum of 15 Ws/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000 $\mu W/cm^2$ power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose that the device can be exposed to without damage is 7,258 Ws/cm^2 (1 week at 12,000 $\mu W/cm^2$). Exposure of these CMOS EPROMS to high intensity ultraviolet light of longer periods may cause permanent damage.

4.5 Programming procedures for method A. The programming procedure shall be as specified by the device manufacture.

TABLE II. Electrical test requirements. 1/ 2/

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 8 (+125°C), 10

* PDA applies to subgroups 1 and 7. Any or all subgroups may be combined when using a high speed tester.

1/ Subgroups 7 and 8 shall consist of verifying the pattern specified.

2/ For all electrical tests, the device shall be programmed to the pattern specified.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. Additional sources will be added to MIL-BUL-103 as they become available. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS. The approved sources of supply listed below are for information purposes only and are current only to the date of the last action of this document.

Military drawing part number	Vendor CAGE number	Vendor 1/ similar part number	Replacement military specification part number	Margin test method
8510201YX	34649	MD27C64-25/B		A
	27014	NMC27C64Q25/883		A
	18324	27C64A/BXA-25		B
	66579	WS27C64L-25DMB		A
8510201ZX	34649	MR27C64-25/B		A
	66579	WS27C64L-25CMB		A
	18324	27C64A/BUA-25		B
8510202YX	34649	MD27C64-35/B		A
	27014	NMC27C64Q35/883		A
	18324	27C64A/BXA-35		B
	66579	WS27C64L-35DMB		A

See footnote at end of table.

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Military drawing part number	Vendor CAGE number	Vendor 1/ similar part number	Replacement military specification part number	Margin test method
8510202ZX	34649	MR27C64-35/B		A
	66579	WS27C64L-35CMB		A
	18324	27C64A/BUA-35		B
8510203YX	34649	MD27C64-20/B		A
	27014	NMC27C64Q20/883		A
	18324	27C64A/BXA-20		B
	66579	WS27C64L-20DMB		A
8510203ZX	34649	MR27C64-20/B		A
	18324	27C64A/BUA-20		B
	66579	WS27C64L-20CMB		B
8510204YX	34335	AM27C64-90/BXA		A
	66579	WS27C64L-90DMB		A
	1FN41	AT27HC64L-90DM/883		A
8510204ZX	34335	AM27C64-90/BUA		A
	66579	WS27C64L-90CMB		A
	1FN41	AT27HC64L-90LM/883		A
8510205YX	34335	AM27C64-120/BXA		A
	66579	WS27C64L-12DMB		A
8510205ZX	34335	AM27C64-120/BUA		A
	66579	WS27C64L-12CMB		A
8510206YX	34335	AM27C64-150/BXA		A
	66579	WS27C64L-15DMB		A
8510206ZX	34335	AM27C64-150/BUA		A
	66579	WS27C64L-15CMB		A

See footnote at end of table.

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Military drawing part number	Vendor CAGE number	Vendor 1/ similar part number	Replacement military specification part number	Margin test method
8510207YX	66579	WS57C64F-70DMB		A
8510207ZX	66579	WS57C64F-70CMB		A

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address	Manufacturer's identification code (see figure 2)	Intelligent identifier (see figure 2)
18324	Signetics Corporation 4130 South Market Court Sacramento, CA 95834	15 H	0B H
27014	National Semiconductor 2900 Semiconductor Drive Santa Clara, CA 95052	8F H	C2 H
34335	Advance Micro Devices 901 Thompson Place P.O. Box 3453 Sunnyvale, CA 94088	01 H	15 H
34649	Intel Corporation 3065 Bowers Avenue Santa Clara, CA 95051	89 H	07 H
66579	Waferscale Integration Incorporated 47280 Kato Road Fremont, CA 94539	23 H	
1FN41	Atmel Corporation 2095 Ringwood Avenue San Jose, CA 95131	1F H	91 H