

# IS61LV256

## 32K x 8 LOW VOLTAGE CMOS STATIC RAM

### FEATURES

- High-speed access times:  
-- 8, 10, 12, 15, 20 ns
- Automatic power-down when chip is deselected
- CMOS low power operation  
-- 345 mW (max.) operating  
-- 7 mW (max.) CMOS standby
- TTL compatible interface levels
- Single 3.3V power supply
- Fully static operation: no clock or refresh required
- Three-state outputs

### DESCRIPTION

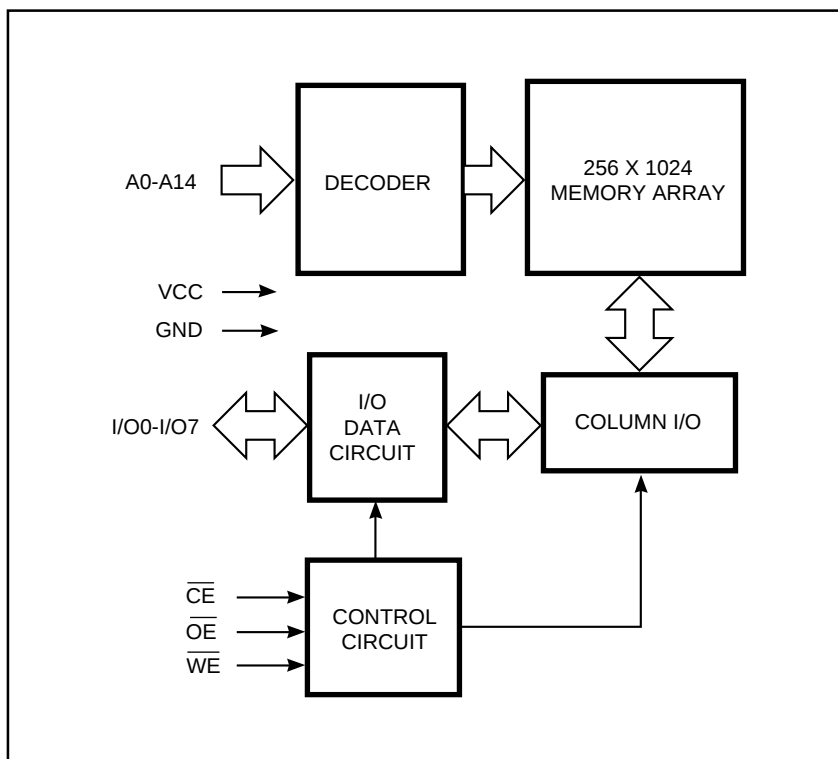
The *ICSI* IS61LV256 is a very high-speed, low power, 32,768-word by 8-bit static RAM. It is fabricated using *ICSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 8 ns maximum.

When  $\overline{CE}$  is HIGH (deselected), the device assumes a standby mode at which the power dissipation is reduced to 50  $\mu$ W (typical) with CMOS input levels.

Easy memory expansion is provided by using an active LOW Chip Enable ( $\overline{CE}$ ). The active LOW Write Enable ( $\overline{WE}$ ) controls both writing and reading of the memory.

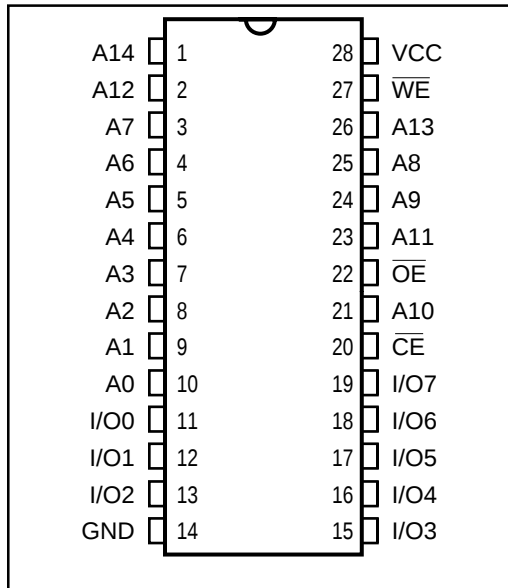
The IS61LV256 is available in the JEDEC standard 28-pin, 300mil SOJ and the 8\*13.4mm TSOP-1 package.

### FUNCTIONAL BLOCK DIAGRAM



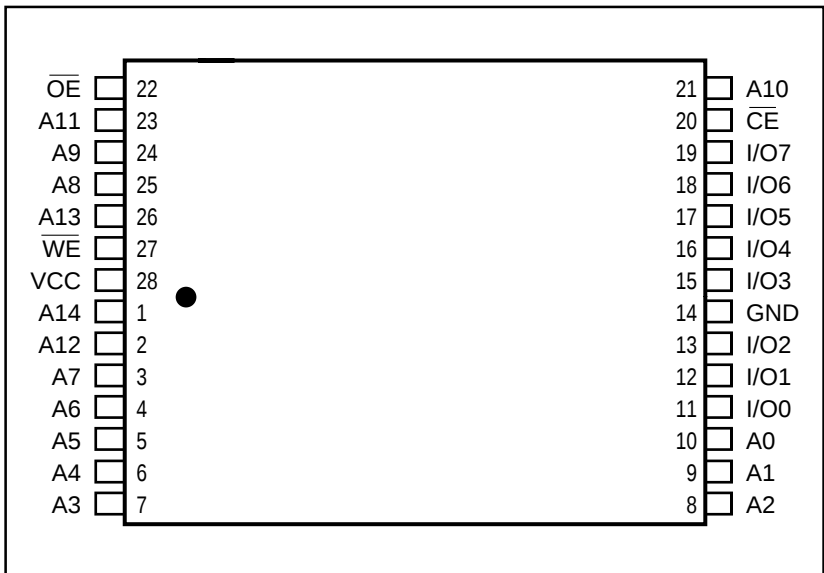
## PIN CONFIGURATION

28-Pin SOJ



## PIN CONFIGURATION

8x13.4mm TSOP-1



## PIN DESCRIPTIONS

|           |                     |
|-----------|---------------------|
| A0-A14    | Address Inputs      |
| CE        | Chip Enable Input   |
| OE        | Output Enable Input |
| WE        | Write Enable Input  |
| I/O0-I/O7 | Input/Output        |
| Vcc       | Power               |
| GND       | Ground              |

## TRUTH TABLE

| Mode                      | WE | CE | OE | I/O Operation | Vcc Current |
|---------------------------|----|----|----|---------------|-------------|
| Not Selected (Power-down) | X  | H  | X  | High-Z        | IsB1, IsB2  |
| Output Disabled           | H  | L  | H  | High-Z        | Icc         |
| Read                      | H  | L  | L  | DOUT          | Icc         |
| Write                     | L  | L  | X  | DIN           | Icc         |

ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

| Symbol | Parameter                            | Value                              | Unit |
|--------|--------------------------------------|------------------------------------|------|
| VCC    | Power Supply Voltage Relative to GND | -0.5 to +4.6                       | V    |
| VTERM  | Terminal Voltage with Respect to GND | -0.5 to +4.6                       | V    |
| TBIAS  | Temperature Under Bias               | Com. -10 to +85<br>Ind. -45 to +90 | °C   |
| TSTG   | Storage Temperature                  | -65 to +150                        | °C   |
| PD     | Power Dissipation                    | 1                                  | W    |
| IOUT   | DC Output Current                    | ±20                                | mA   |

## Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## OPERATING RANGE

| Range      | Ambient Temperature | Speed     | V <sub>CC</sub> |
|------------|---------------------|-----------|-----------------|
| Commercial | 0°C to +70°C        | 8, 10, 12 | 3.3V, +10%, -5% |
|            |                     | 15, 20    | 3.3V ± 10%      |
| Industrial | -40°C to +85°C      | All       | 3.3V + 10%, -5% |

## DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

| Symbol          | Parameter                        | Test Conditions                                             | Min.         | Max.                  | Unit |
|-----------------|----------------------------------|-------------------------------------------------------------|--------------|-----------------------|------|
| V <sub>OH</sub> | Output HIGH Voltage              | V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA           | 2.4          | —                     | V    |
| V <sub>OL</sub> | Output LOW Voltage               | V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA            | —            | 0.4                   | V    |
| V <sub>IH</sub> | Input HIGH Voltage               |                                                             | 2.2          | V <sub>CC</sub> + 0.3 | V    |
| V <sub>IL</sub> | Input LOW Voltage <sup>(1)</sup> |                                                             | -0.3         | 0.8                   | V    |
| I <sub>LI</sub> | Input Leakage                    | GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>                     | Com.<br>Ind. | -1<br>5               | μA   |
| I <sub>LO</sub> | Output Leakage                   | GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Outputs Disabled | Com.<br>Ind. | -1<br>5               | μA   |

Notes:

1. V<sub>IL</sub> (min.) = -0.3V (DC); V<sub>IL</sub> (min.) = -2.0V (pulse width ≤ 2.0 ns).  
V<sub>IH</sub> (max.) = V<sub>CC</sub> + 0.5V (DC); V<sub>IH</sub> (max.) = V<sub>CC</sub> + 2.0V (pulse width ≤ 2.0 ns).
2. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

## POWER SUPPLY CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

| Sym.             | Parameter                                        | Test Conditions                                                                                                                                  |      | -8 ns     | -10 ns    | -12 ns    | -15 ns    | -20 ns    | Unit |
|------------------|--------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------|------|-----------|-----------|-----------|-----------|-----------|------|
|                  |                                                  |                                                                                                                                                  |      | Min. Max. | Min. Max. | Min. Max. | Min. Max. | Min. Max. |      |
| I <sub>CC</sub>  | V <sub>CC</sub> Dynamic Operating Supply Current | V <sub>CC</sub> = Max., $\overline{CE}$ = V <sub>IL</sub><br>I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub>                                       | Com. | - 120     | - 110     | - 100     | - 90      | - 80      | mA   |
|                  |                                                  |                                                                                                                                                  | Ind. | - 130     | - 120     | - 110     | - 100     | - 90      |      |
| I <sub>SB1</sub> | TTL Standby Current (TTL Inputs)                 | V <sub>CC</sub> = Max.,<br>V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub><br>$\overline{CE} \geq V_{IH}$ , f = 0                           | Com. | - 25      | - 25      | - 25      | - 25      | - 25      | mA   |
|                  |                                                  |                                                                                                                                                  | Ind. | - 30      | - 30      | - 30      | - 30      | - 30      |      |
| I <sub>SB2</sub> | CMOS Standby Current (CMOS Inputs)               | V <sub>CC</sub> = Max.,<br>$\overline{CE} \leq V_{CC} - 0.2V$ ,<br>V <sub>IN</sub> > V <sub>CC</sub> - 0.2V, or<br>V <sub>IN</sub> ≤ 0.2V, f = 0 | Com. | - 2       | - 2       | - 2       | - 2       | - 2       | mA   |
|                  |                                                  |                                                                                                                                                  | Ind. | - 5       | - 5       | - 5       | - 5       | - 5       |      |

Notes:

1. At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

## CAPACITANCE<sup>(1,2)</sup>

| Symbol           | Parameter          | Conditions            | Max. | Unit |
|------------------|--------------------|-----------------------|------|------|
| C <sub>IN</sub>  | Input Capacitance  | V <sub>IN</sub> = 0V  | 6    | pF   |
| C <sub>OUT</sub> | Output Capacitance | V <sub>OUT</sub> = 0V | 5    | pF   |

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T<sub>A</sub> = 25°C, f = 1 MHz, V<sub>CC</sub> = 3.3V.

## READ CYCLE SWITCHING CHARACTERISTICS<sup>(1)</sup> (Over Operating Range)

| Symbol           | Parameter                        | -8 ns |      | -10 ns |      | -12 ns |      | -15 ns |      | -20 ns |      | Unit |
|------------------|----------------------------------|-------|------|--------|------|--------|------|--------|------|--------|------|------|
|                  |                                  | Min.  | Max. | Min.   | Max. | Min.   | Max. | Min.   | Max. | Min.   | Max. |      |
| $t_{RC}$         | Read Cycle Time                  | 8     | —    | 10     | —    | 12     | —    | 15     | —    | 20     | —    | ns   |
| $t_{AA}$         | Address Access Time              | —     | 8    | —      | 10   | —      | 12   | —      | 15   | —      | 20   | ns   |
| $t_{OHA}$        | Output Hold Time                 | 2     | —    | 2      | —    | 2      | —    | 2      | —    | 2      | —    | ns   |
| $t_{ACE}$        | $\overline{CE}$ Access Time      | —     | 8    | —      | 10   | —      | 12   | —      | 15   | —      | 20   | ns   |
| $t_{DOE}$        | $\overline{OE}$ Access Time      | —     | 4    | —      | 5    | —      | 6    | —      | 7    | —      | 8    | ns   |
| $t_{LZOE}^{(2)}$ | $\overline{OE}$ to Low-Z Output  | 0     | —    | 0      | —    | 0      | —    | 0      | —    | 0      | —    | ns   |
| $t_{HZOE}^{(2)}$ | $\overline{OE}$ to High-Z Output | —     | 4    | —      | 5    | —      | 5    | —      | 6    | —      | 6    | ns   |
| $t_{LZCE}^{(2)}$ | $\overline{CE}$ to Low-Z Output  | 3     | —    | 3      | —    | 3      | —    | 3      | —    | 3      | —    | ns   |
| $t_{HZCE}^{(2)}$ | $\overline{CE}$ to High-Z Output | —     | 4    | —      | 5    | —      | 6    | —      | 7    | —      | 7    | ns   |
| $t_{PU}^{(3)}$   | $\overline{CE}$ to Power-Up      | 0     | —    | 0      | —    | 0      | —    | 0      | —    | 0      | —    | ns   |
| $t_{PD}^{(4)}$   | $\overline{CE}$ to Power-Down    | —     | 8    | —      | 10   | —      | 12   | —      | 15   | —      | 20   | ns   |

### Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured  $\pm 200$  mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

## AC TEST CONDITIONS

| Parameter                                    | Unit                |
|----------------------------------------------|---------------------|
| Input Pulse Level                            | 0V to 3.0V          |
| Input Rise and Fall Times                    | 3 ns                |
| Input and Output Timing and Reference Levels | 1.5V                |
| Output Load                                  | See Figures 1 and 2 |

## AC TEST LOADS

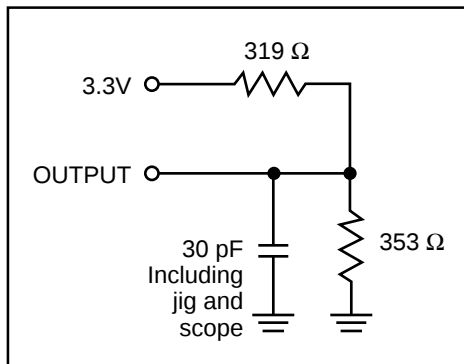


Figure 1.

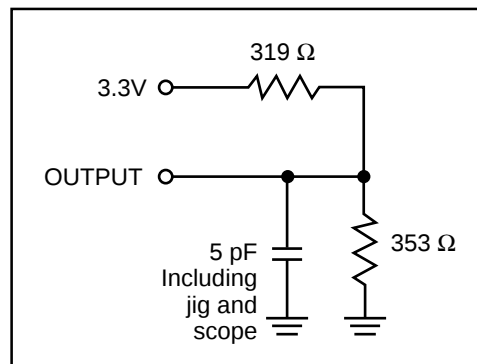
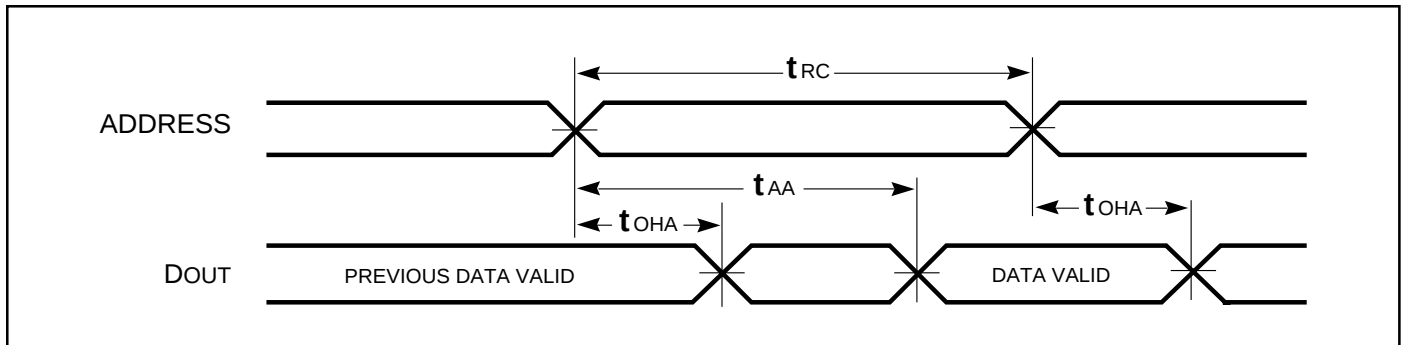
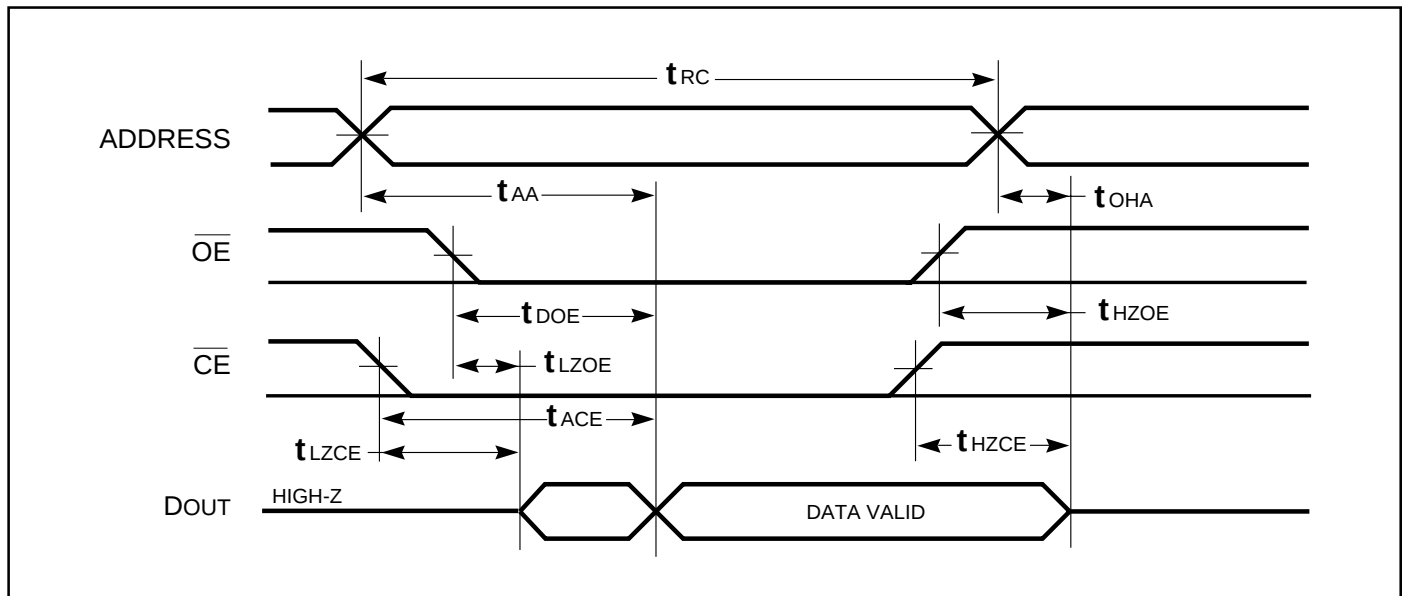


Figure 2.

## AC WAVEFORMS

READ CYCLE NO. 1<sup>(1,2)</sup>READ CYCLE NO. 2<sup>(1,3)</sup>

## Notes:

1.  $\overline{WE}$  is HIGH for a Read Cycle.
2. The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .
3. Address is valid prior to or coincident with  $\overline{CE}$  LOW transitions.

## WRITE CYCLE SWITCHING CHARACTERISTICS<sup>(1,2)</sup> (Over Operating Range)

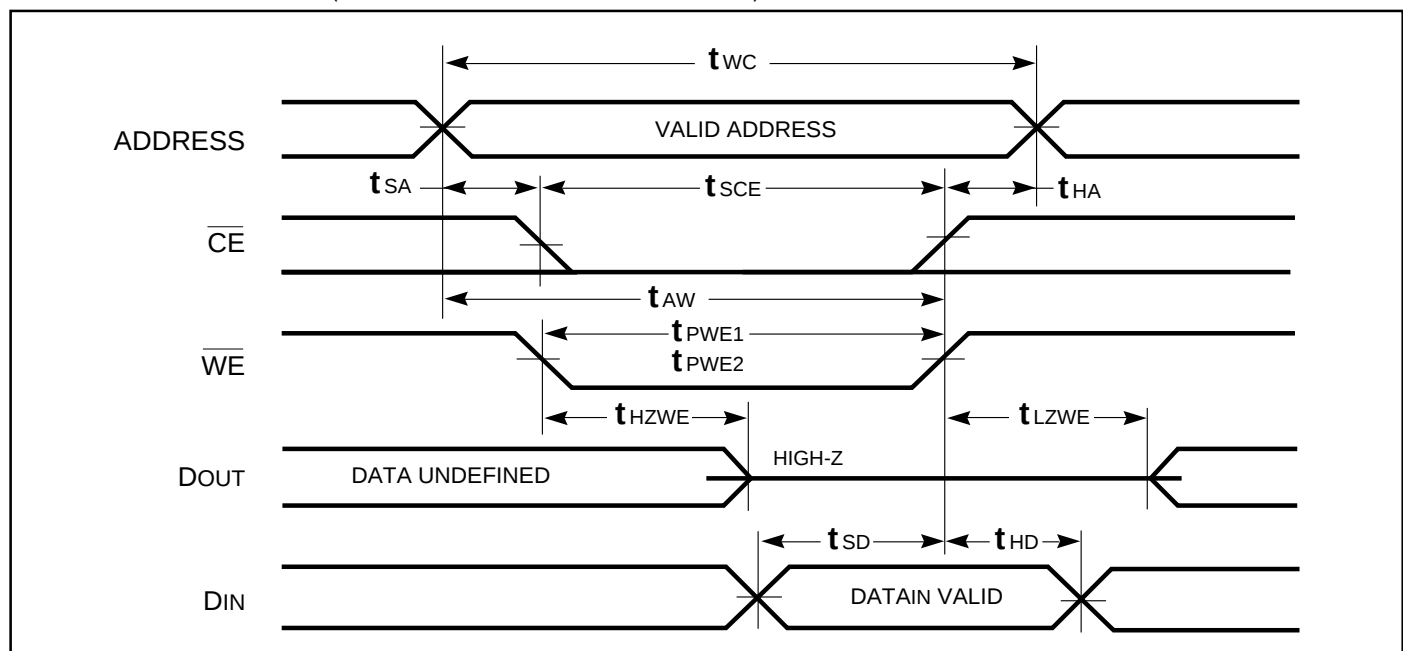
| Symbol           | Parameter                                          | -8 ns |      | -10 ns |      | -12 ns |      | -15 ns |      | -20 ns |      | Unit |
|------------------|----------------------------------------------------|-------|------|--------|------|--------|------|--------|------|--------|------|------|
|                  |                                                    | Min.  | Max. | Min.   | Max. | Min.   | Max. | Min.   | Max. | Min.   | Max. |      |
| $t_{WC}$         | Write Cycle Time                                   | 8     | —    | 10     | —    | 12     | —    | 15     | —    | 20     | —    | ns   |
| $t_{SCE}$        | $\overline{CE}$ to Write End                       | 7     | —    | 8      | —    | 8      | —    | 10     | —    | 12     | —    | ns   |
| $t_{AW}$         | Address Setup Time to Write End                    | 7     | —    | 8      | —    | 8      | —    | 10     | —    | 12     | —    | ns   |
| $t_{HA}$         | Address Hold from Write End                        | 0     | —    | 0      | —    | 0      | —    | 0      | —    | 0      | —    | ns   |
| $t_{SA}$         | Address Setup Time                                 | 0     | —    | 0      | —    | 0      | —    | 0      | —    | 0      | —    | ns   |
| $t_{PWE1}$       | $\overline{WE}$ Pulse Width( $\overline{OE}$ High) | 7     | —    | 10     | —    | 12     | —    | 15     | —    | 20     | —    | ns   |
| $t_{PWE2}$       | $\overline{WE}$ Pulse Width( $\overline{OE}$ Low)  | 6.5   | —    | 7      | —    | 8      | —    | 10     | —    | 12     | —    | ns   |
| $t_{SD}$         | Data Setup to Write End                            | 4.5   | —    | 5      | —    | 6      | —    | 7      | —    | 10     | —    | ns   |
| $t_{HD}$         | Data Hold from Write End                           | 0     | —    | 0      | —    | 0      | —    | 0      | —    | 0      | —    | ns   |
| $t_{HZWE}^{(3)}$ | $\overline{WE}$ LOW to High-Z Output               | —     | 3.5  | —      | 4    | —      | 6    | —      | 7    | —      | 7    | ns   |
| $t_{LZWE}^{(3)}$ | $\overline{WE}$ HIGH to Low-Z Output               | 0     | —    | 0      | —    | 0      | —    | 0      | —    | 0      | —    | ns   |

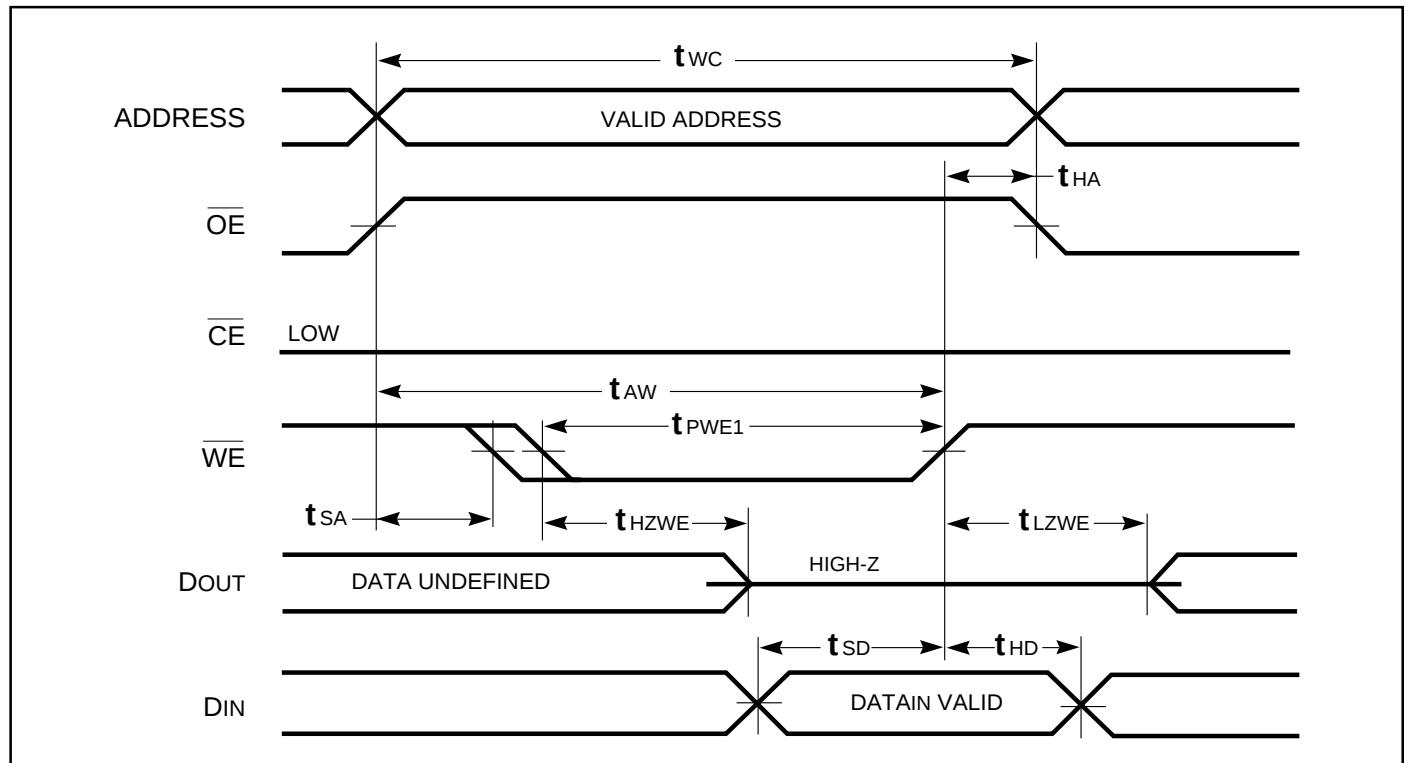
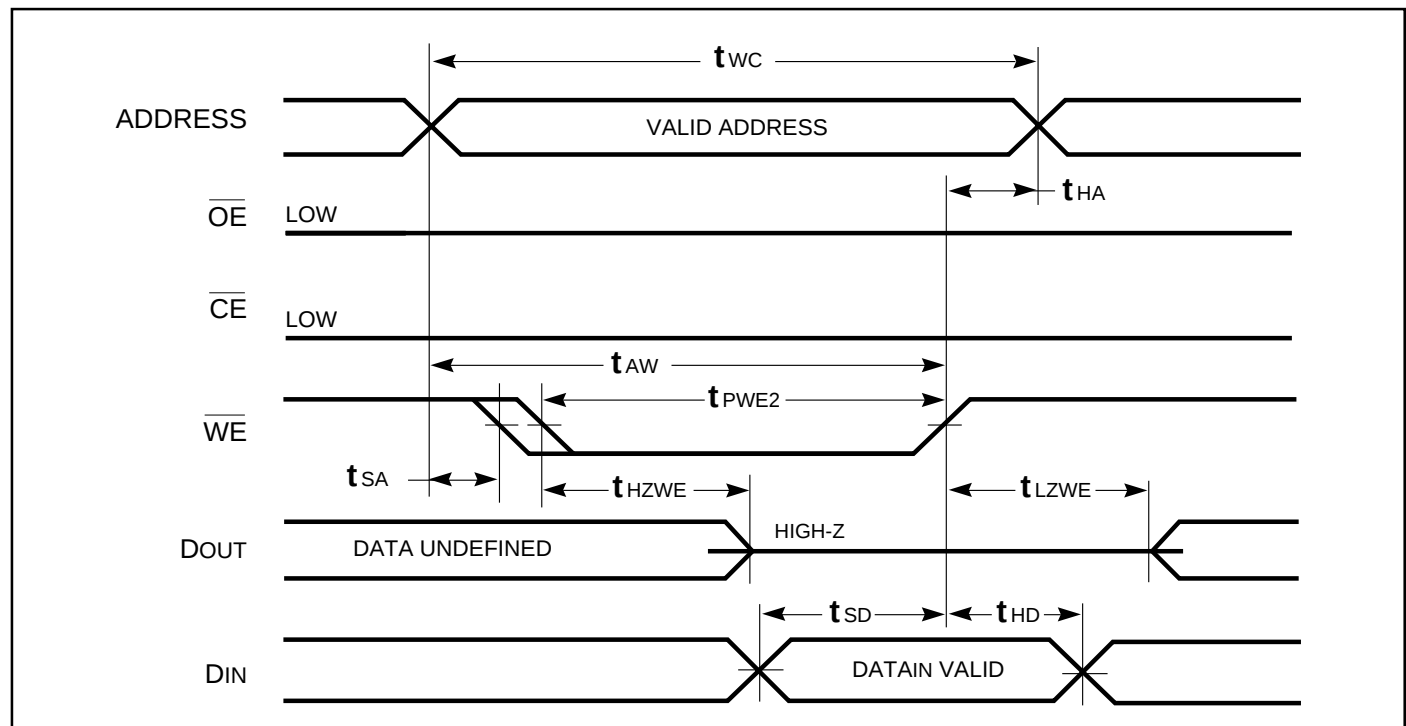
### Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
3. Tested with the load in Figure 2. Transition is measured  $\pm 500$  mV from steady-state voltage. Not 100% tested.

## AC WAVEFORMS

### WRITE CYCLE NO. 1 ( $\overline{CE}$ Controlled, $\overline{OE}$ is HIGH or LOW) <sup>(1)</sup>



**WRITE CYCLE NO. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  is HIGH During Write Cycle) <sup>(1,2)</sup>**

**WRITE CYCLE NO. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  is LOW During Write Cycle) <sup>(1)</sup>**

**Notes:**

1. The internal write time is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if  $\overline{OE} \geq V_{IH}$ .

## ORDERING INFORMATION

Commercial Range: 0°C to +70°C

| Speed (ns) | Order Part No. | Package         |
|------------|----------------|-----------------|
| 8          | IS61LV256-8T   | 8*13.4mm TSOP-1 |
|            | IS61LV256-8J   | 300mil SOJ      |
| 10         | IS61LV256-10T  | 8*13.4mm TSOP-1 |
|            | IS61LV256-10J  | 300mil SOJ      |
| 12         | IS61LV256-12T  | 8*13.4mm TSOP-1 |
|            | IS61LV256-12J  | 300mil SOJ      |
| 15         | IS61LV256-15T  | 8*13.4mm TSOP-1 |
|            | IS61LV256-15J  | 300mil SOJ      |
| 20         | IS61LV256-15T  | 8*13.4mm TSOP-1 |
|            | IS61LV256-20J  | 300mil SOJ      |

## ORDERING INFORMATION

Industrial Range: -40°C to +85°C

| Speed (ns) | Order Part No. | Package         |
|------------|----------------|-----------------|
| 8          | IS61LV256-8TI  | 8*13.4mm TSOP-1 |
|            | IS61LV256-8JI  | 300mil SOJ      |
| 10         | IS61LV256-10TI | 8*13.4mm TSOP-1 |
|            | IS61LV256-10JI | 300mil SOJ      |
| 12         | IS61LV256-12TI | 8*13.4mm TSOP-1 |
|            | IS61LV256-12JI | 300mil SOJ      |
| 15         | IS61LV256-15TI | 8*13.4mm TSOP-1 |
|            | IS61LV256-15JI | 300mil SOJ      |
| 20         | IS61LV256-20TI | 8*13.4mm TSOP-1 |
|            | IS61LV256-20JI | 300mil SOJ      |

*Integrated Circuit Solution Inc.*

HEADQUARTER:

NO.2, TECHNOLOGY RD. V, SCIENCE-BASED INDUSTRIAL PARK,  
HSIN-CHU, TAIWAN, R.O.C.

TEL: 886-3-5780333

Fax: 886-3-5783000

BRANCH OFFICE:

7F, NO. 106, SEC. 1, HSIN-TAI 5<sup>TH</sup> ROAD,  
HSICHIH TAIPEI COUNTY, TAIWAN, R.O.C.

TEL: 886-2-26962140

FAX: 886-2-26962252

<http://www.icsi.com.tw>