IMS1420
IMS1421
High Performance 4Kx4 Static RAM

inmos

FEATURES

- 4K x 4 Bit Organization
- 40nsec and 50nsec Address Access Times
- 605mW Maximum Power Dissipation
- Fully TTL Compatible
- Common Data Inputs & Outputs
- 20-pin, 300-mil DIP
- Single +5V ± 10% Operation

IMS1420
- 45nsec and 55nsec Chip Enable Access Times
- Power Down Function
- 165mW Maximum Standby Power

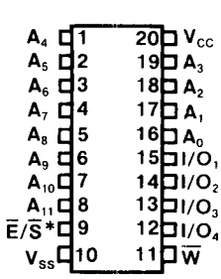
IMS1421
- High Speed Chip Select Function
- 30nsec and 40nsec Chip Select Access Times

DESCRIPTION

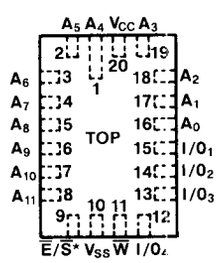
The IMS1420 and IMS1421 feature fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1420 provides a Chip Enable ($\overline{E}$) function that can be used to place the device into a low-power standby mode, thus reducing power to 165mW. In place of the Chip Enable function, the IMS1421 provides a high speed Chip Select ($\overline{S}$) function which allows faster access times to be achieved. With these two options, the designer can select the device which better fits his particular application.

The IMS1420 is packaged in a 20-pin 300-mil plastic DIP, and both the IMS1420 and IMS1421 are available in ceramic DIPs and ceramic chip carriers.

PIN CONFIGURATION

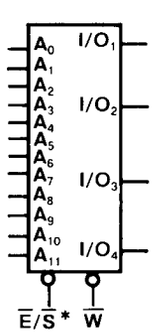


DIP

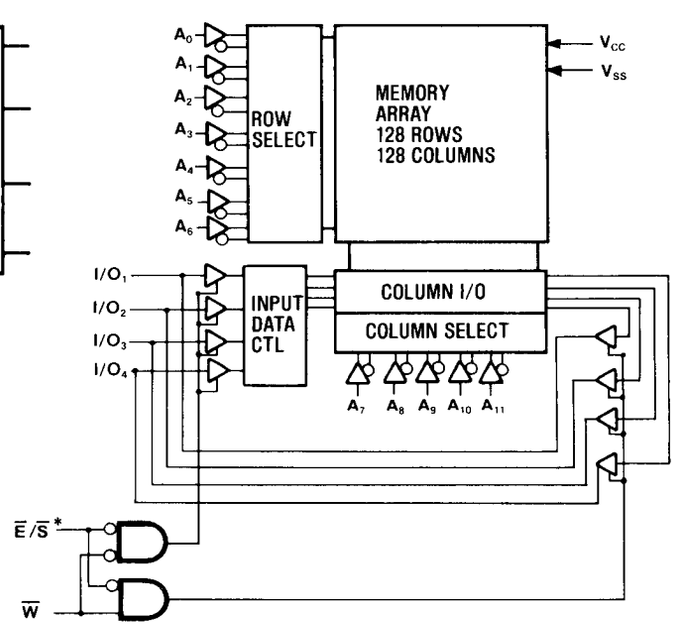


CHIP CARRIER

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0-A_{11}	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{W}$	WRITE ENABLE	V_{SS}	GROUND
$\overline{E}$ *	CHIP ENABLE		
$\overline{S}$ *	CHIP SELECT		
I/O	DATA IN/OUT		

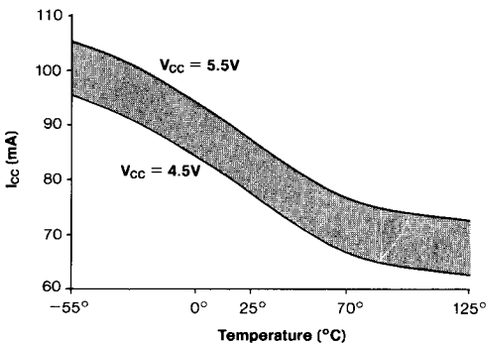
* $\overline{E}$ IMS1420 ONLY
$\overline{S}$ IMS1421 ONLY

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to V_{SS} . . . −3.5 to 7.0V
Temperature Under Bias. . . . . −55°C to 125°C
Storage Temperature (Ambient) . . −65°C to 150°C
Power Dissipation. 1W
DC Output Current. 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TYPICAL DYNAMIC I_{CC} VS TEMPERATURE



DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		6.0	V	
V_{IL}	Input Logic "0" Voltage	−2.0		0.8	V	
T_A	Ambient Operating Temperature	0		70	°C	400 Linear ft/min transverse air flow

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +70°C$) ($V_{CC} = 5.0V \pm 10\%$)

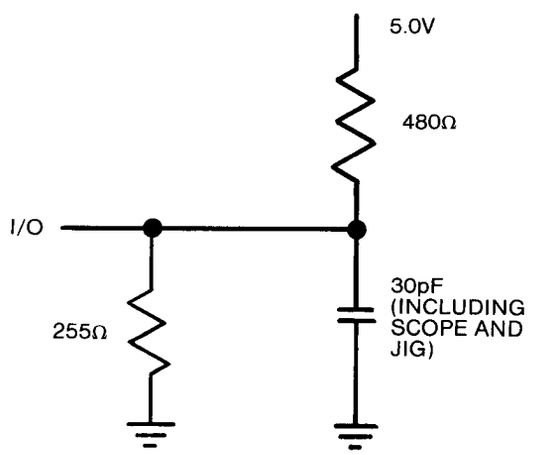
SYMBOL	PARAMETER	1420		1421		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I_{CC1}	Average V_{CC} Power Supply Current AC		110		110	mA	$t_C = t_{C(min)}$
I_{CC2}	V_{CC} Power Supply Current (Stdby)		30		NA	mA	$\overline{E} \geq V_{IH(min)}$
I_{IN}	Input Leakage Current (Any Input)		10		10	μA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off State Output Leakage Current		50		50	μA	V_{CC} = max $V_{OUT} = V_{SS}$ to V_{CC}
V_{OH}	Output Logic "1" Voltage $I_{OUT} = -4mA$	2.4		2.4		V	
V_{OL}	Output Logic "0" Voltage $I_{OUT} = 8mA$		.4		.4	V	

AC TEST CONDITIONS[a]

Input Pulse Levels. . . . . V_{SS} to 3V
Input Rise and Fall Times. 5ns
Input and Output Timing Reference Levels. 1.5V
Output Load. . . . . See Figure 1

Note a: Operation to specifications guaranteed 2ms after V_{CC} applied.

FIGURE 1. OUTPUT LOAD



CAPACITANCE[b] ($T_A = 25°C$, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNIT	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V
$C_{E/\overline{S}}$	$\overline{E}/\overline{S}$ Capacitance	6	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

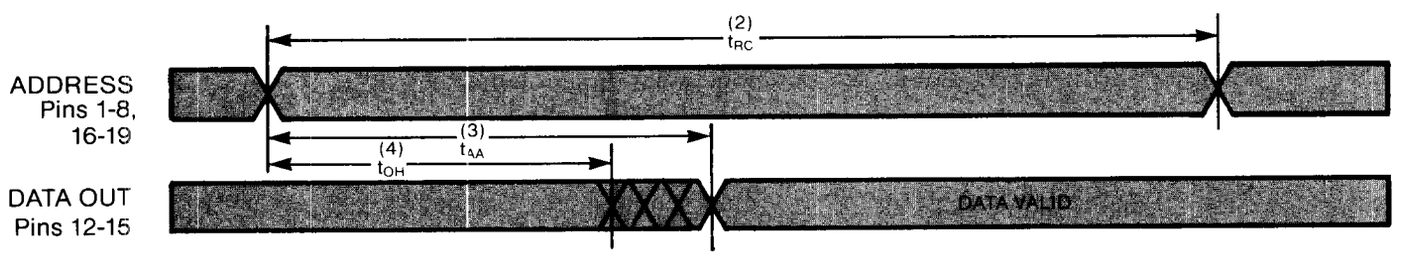
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE

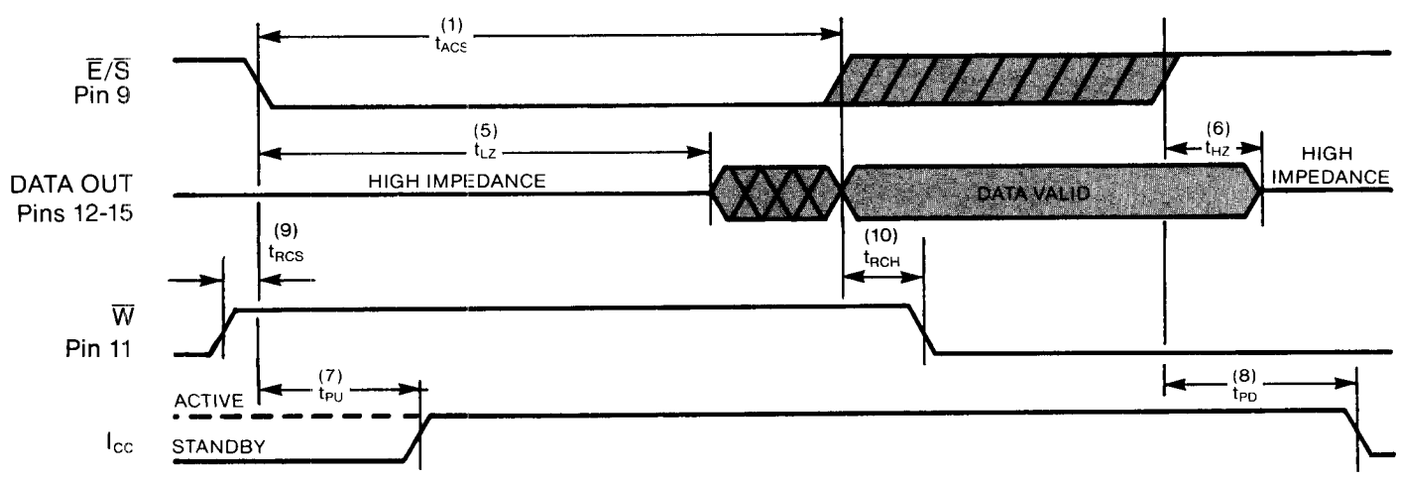
NO.	SYMBOL	PARAMETER	1420-45		1420-55		1421-40		1421-50		UNITS	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{ACS}	Chip Enable/Select Access Time		45		55		30		40	ns	
2	t_{RC}	Read Cycle Time	40		50		40		50		ns	c
3	t_{AA}	Address Access Time		40		50		40		50	ns	d
4	t_{OH}	Output Hold After Address Change	3		3		3		3		ns	
5	t_{LZ}	Chip Enable/Select to Output Active	20		20		20		20		ns	
6	t_{HZ}	Chip Disable/Select to Output Disable		20		25		20		25	ns	f
7	t_{PU}	Chip Enable to Power Up	0		0		NA		NA		ns	
8	t_{PD}	Chip Disable to Power Down		45		55		NA		NA	ns	
9	t_{RCS}	Read Command Set-up Time	−5		−5		−5		−5		ns	
10	t_{RCH}	Read Command Hold Time	−5		−5		−5		−5		ns	
	t_t	Input Rise and Fall Times		50		50		50		50	ns	e

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected. $\overline{E}/\overline{S}$ low.
Note e: Measured between V_{IL} max. and V_{IH} min.
Note f: Measured ± 200mV from steady state output voltage.

READ CYCLE 1[c,d]



READ CYCLE 2[c]



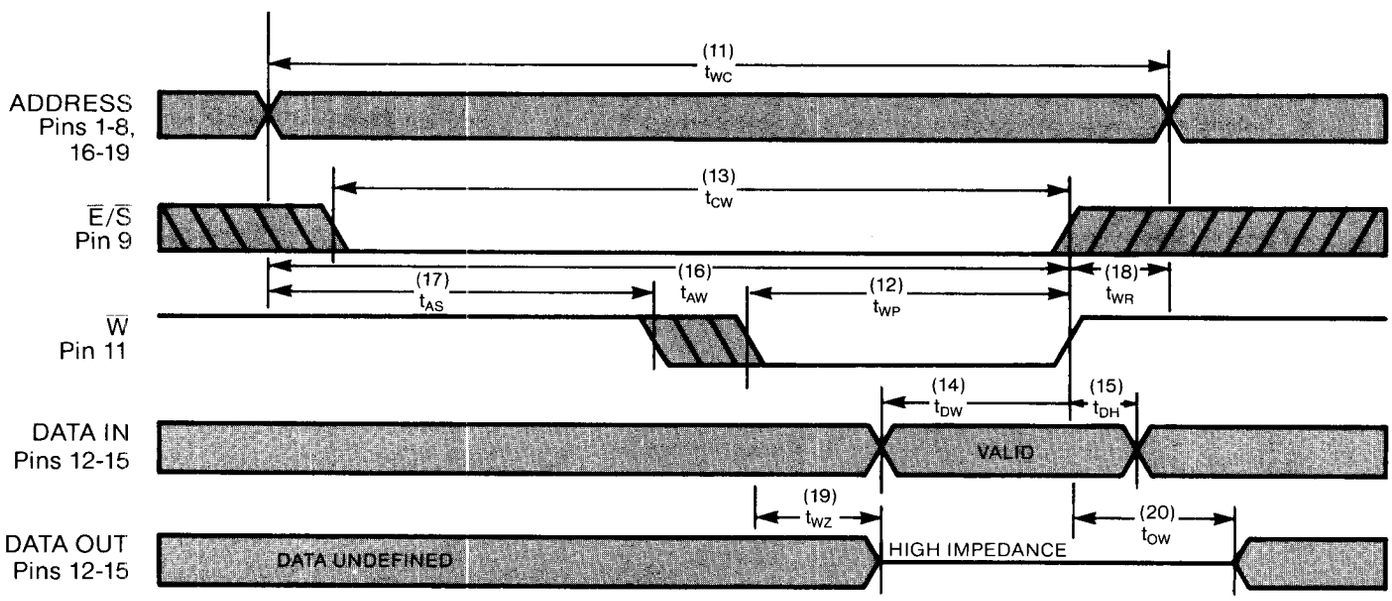
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[h]

NO.	SYMBOL	PARAMETER	1420-45		1420-55		1421-40		1421-50		UNITS	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
11	t_{WC}	Write Cycle Time	40		50		40		50		ns	
12	t_{WP}	Write Pulse Width	35		45		35		45		ns	
13	t_{CW}	Chip Enable/Select to End of Write	35		45		30		40		ns	
14	t_{DW}	Data Set-up to End of Write	15		20		15		20		ns	
15	t_{DH}	Data Hold After End of Write	3		3		3		3		ns	
16	t_{AW}	Address Set-up to End of Write	35		45		40		50		ns	
17	t_{AS}	Address Set-up to Beginning of Write	0		0		0		0		ns	
18	t_{WR}	Address Hold After End of Write	5		5		0		0		ns	
19	t_{WZ}	Write Enable to Output Disable		20		25		20		25	ns	f
20	t_{OW}	Output Active After End of Write	8		8		8		8		ns	g

Note f: Measured ± 200mV from steady state output voltage.
Note g: If $\overline{E}/\overline{S}$ goes low with $\overline{W}$ low, Output remains in high impedance state.
Note h: $\overline{E}/\overline{S}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.

WRITE CYCLE 1



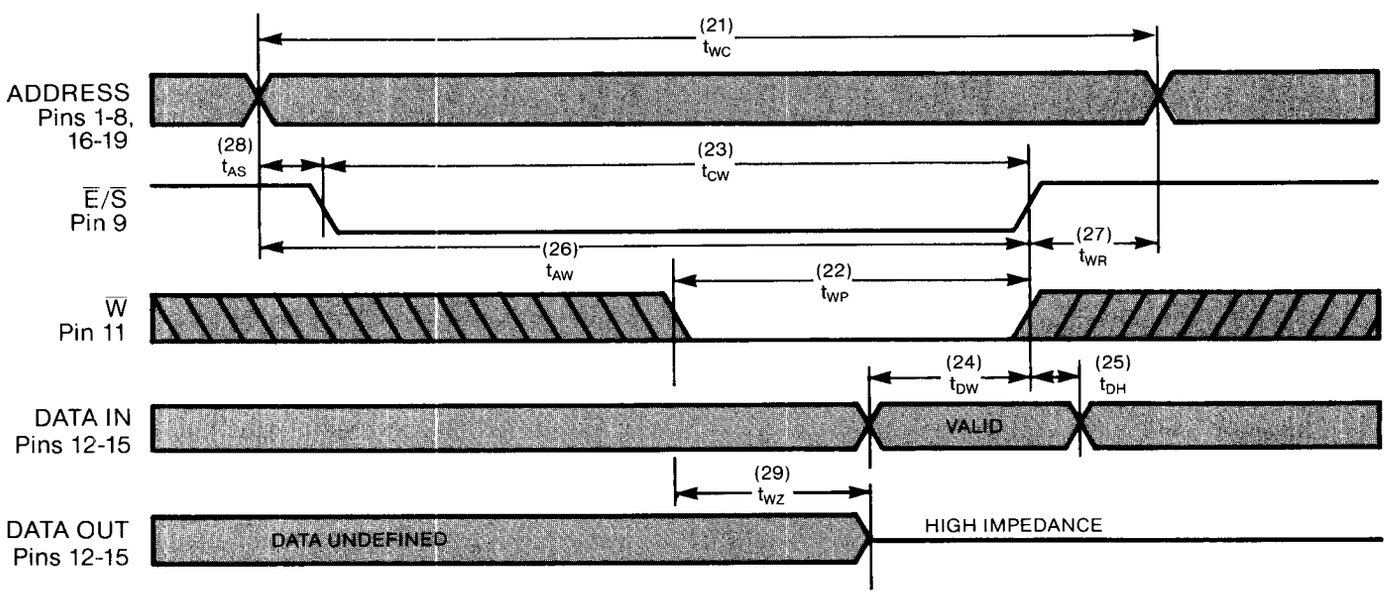
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 2: $\overline{E}/\overline{S}$ CONTROLLED[h]

NO.	SYMBOL	PARAMETER	1420-45		1420-55		1421-40		1421-50		UNITS	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
21	t_{WC}	Write Cycle Time	40		50		40		50		ns	
22	t_{WP}	Write Pulse Width	35		45		35		45		ns	
23	t_{CW}	Chip Enable/Select to End of Write	35		45		30		40		ns	
24	t_{DW}	Data Set-up to End of Write	15		20		15		20		ns	
25	t_{DH}	Data Hold After End of Write	5		5		5		5		ns	
26	t_{AW}	Address Set-up to End of Write	30		40		35		45		ns	
27	t_{WR}	Address Hold After End of Write	5		5		5		5		ns	
28	t_{AS}	Address Set-up to Beginning of Write	−5		−5		0		0		ns	
29	t_{WZ}	Write Enable to Output Disable		20		25		20		25	ns	f

Note f: Measured ± 200mV from steady state output voltage.
Note h: $\overline{E}/\overline{S}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.

WRITE CYCLE 2



DEVICE OPERATION (IMS1420)

The IMS1420 has two control inputs, Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$), twelve address inputs, and four Data I/O lines.

When V_{CC} is first applied to pin 20, a circuit associated with the $\overline{E}$ input forces the device into the lower power standby mode regardless of the state of the $\overline{E}$ input. After V_{CC} is applied for 2ms, the $\overline{E}$ input controls device selection as well as active and standby modes.

With $\overline{E}$ low, the device is selected and the twelve address inputs are decoded to select one 4-bit word out of 4096. Read and Write operations on the memory cell are controlled by $\overline{W}$ input. With $\overline{E}$ high, the device is deselected, the output is disabled, and the power consumption is reduced to less than one-third of the active mode power.

READ CYCLE

A read cycle is defined as $\overline{W} \geq V_{IH}$ min. with $\overline{E} \leq V_{IL}$ max. Read access time is measured from either $\overline{E}$ going low or from valid address.

The READ CYCLE 1 waveform on page 3 shows a read access that is initiated by a change in the address inputs while $\overline{E}$ is low. The output remains active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and the output remains valid for a minimum of 3ns. As long as $\overline{E}$ remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform on page 3 shows a read access that is initiated by $\overline{E}$ going low. As long as address is stable within 5ns after $\overline{E}$ goes low, valid data is at the output at the specified Chip Enable access time. If address is not valid within 5ns after $\overline{E}$ goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

A write cycle is initiated by the latter of $\overline{W}$ or $\overline{E}$ going low and terminated by $\overline{W}$ (WRITE CYCLE 1) or $\overline{E}$ (WRITE CYCLE 2) going high. During the write cycle, data on the inputs is written into the selected cells and the outputs are floating.

If a write cycle is initiated by $\overline{W}$ going low, the address must be stable for the WRITE CYCLE 1 set-up time. If a write cycle is initiated by $\overline{E}$ going low, the address need not be stable until a maximum of 5ns after $\overline{E}$ goes low. The address must be held stable for the entire write cycle. After $\overline{W}$ or $\overline{E}$ goes high to terminate the write cycle, addresses may change. If these address set-up and hold times are not met, contents of other cells may be altered in unpredictable ways.

WRITE CYCLE 1 waveform on page 4 shows a write cycle terminated by $\overline{W}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{W}$. With $\overline{W}$ high, the outputs become active. When $\overline{W}$ goes high at the end of a write cycle and the outputs of the memory go active, the data from the memory will be the same as the data just written into the memory. Thus, no data bus contention will occur.

WRITE CYCLE 2 waveform on page 5 shows a write cycle terminated by $\overline{E}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{E}$. With $\overline{E}$ high, the outputs remain in the high impedance state.

DEVICE OPERATION (IMS1421)

The operation of the IMS1421 is similar to the operation of the IMS1420 except that the Chip Enable ($\overline{E}$) function on the IMS1420 is replaced by a high speed Chip Select ($\overline{S}$) for the IMS1421. The $\overline{S}$ function controls chip selection but there is no power down function on the IMS1421. The IMS1421 is designed to allow even higher system performance than is possible with the IMS1420 by removing the Chip Select decoder delay from the critical access delay path.

With $\overline{S}$ high, the device is deselected and the outputs are disabled.

READ CYCLE

A read cycle is defined as $\overline{W} \geq V_{IH}$ min. with $\overline{S} \leq V_{IL}$ max. Read access time is measured from either $\overline{S}$ going low or from valid address. If $\overline{S}$ goes low within 10ns of address valid, access time is equal to address access time. If $\overline{S}$ goes low later than 10ns after address valid, then access time is equal to Chip Select access time.

WRITE CYCLE

A write cycle is initiated by the latter of $\overline{W}$ or $\overline{S}$ going low and is terminated by $\overline{W}$ (WRITE CYCLE 1) or $\overline{S}$ (WRITE CYCLE 2) going high. During a write cycle, the outputs are floated and the data on the inputs are written into the addressed memory cells.

If a write cycle is initiated by $\overline{W}$ going low, the address must be stable for the specified WRITE CYCLE 1 set-up time. If a write cycle is initiated by $\overline{S}$ going low, the address must be stable for the specified WRITE CYCLE 2 set-up time. WRITE CYCLE 1 waveform on page 4 shows a write cycle terminated by $\overline{W}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{W}$. With $\overline{W}$ high and $\overline{S}$ low, the outputs become active.

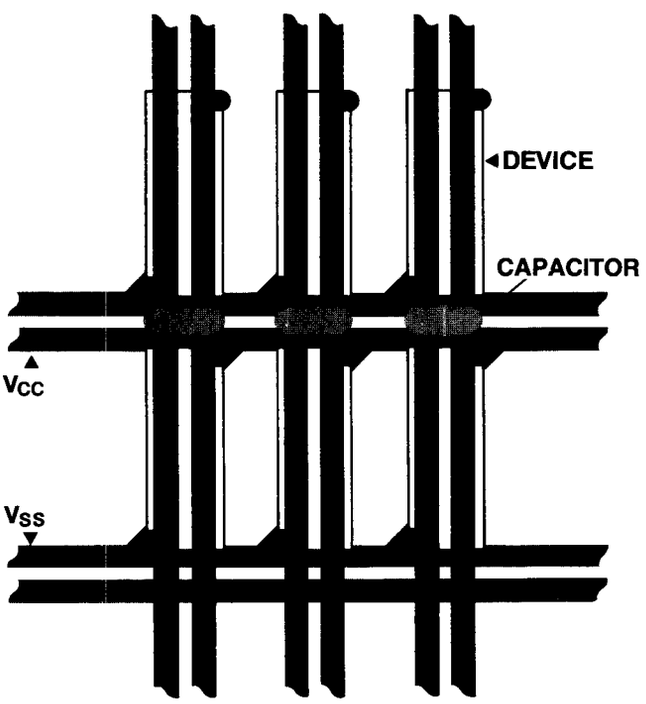
WRITE CYCLE 2 on page 5 shows a write cycle terminated by the rising edge of $\overline{S}$. Data set-up and hold times are referenced to the rising edge of $\overline{S}$, and the outputs remain in the high impedance state.

APPLICATION

Fundamental rules in regard to memory board layout should be followed to ensure maximum benefit from the features offered by the IMS1420/21 Static RAM.

Power Distribution: The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1420/21. The impedance in the decoupling path from the power pin (20) through the decoupling capacitor to the ground pin (10) should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Since the current transients associated with the operation of the high speed IMS1420/21 are high frequency, the line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor acts as a low impedance power supply located near the memory device. The high frequency decoupling capacitor should have a value of 0.1μF, and be placed between the rows of memory devices in the array (see drawing). A larger tantalum capacitor with a value between 22μF and 47μF should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.



V_{CC}, V_{SS} GRID SHOWING DECOUPLING CAPACITORS

The ground grid of the memory array should extend to the TTL driver periphery circuit. This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

Termination: Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

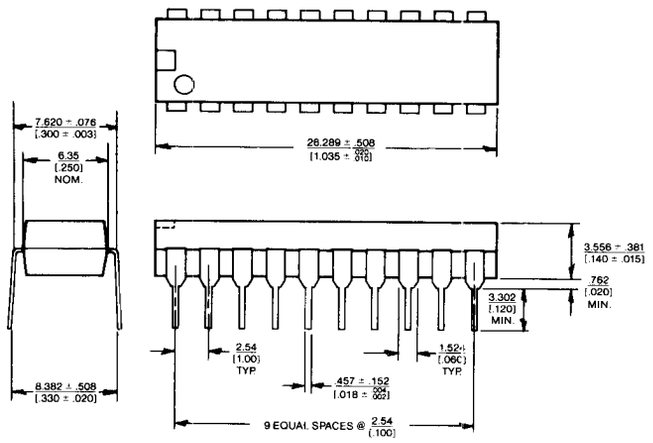
The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The line should be kept short by placing the driver-termination combination close to the memory array.

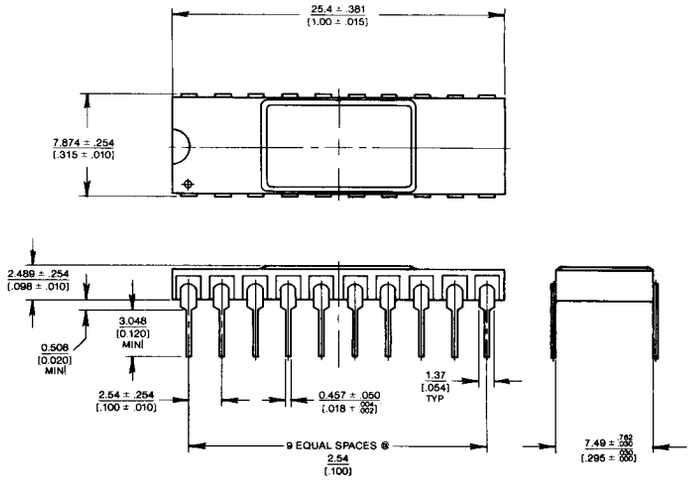
Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10Ω to 30Ω range will be required.

Proper power distribution techniques, including adequate use of decoupling capacitors, and proper termination of TTL drive outputs are some of the most important yet basic guidelines that need to be followed when designing and building a memory board. The guidelines are intended to maintain the operating margins of all devices on the memory board by providing a quiet environment free of noise spikes and signal reflections.

IMS1420/21

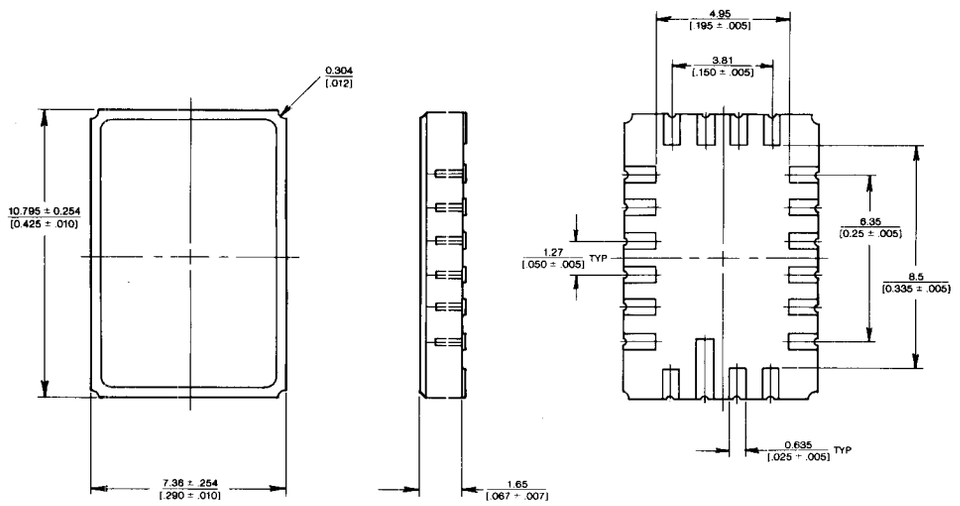
20 PIN PLASTIC DUAL-IN-LINE





20 PIN CERAMIC DUAL-IN-LINE

20 PIN CHIP CARRIER



DIMENSION NOTE:
Top Number in Millimeters
Bottom Number in Inches

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS1420	45ns	PLASTIC DIP	IMS1420P-45
	45ns	CERAMIC DIP	IMS1420S-45
	45ns	CHIP CARRIER	IMS1420W-45
	55ns	PLASTIC DIP	IMS1420P-55
	55ns	CERAMIC DIP	IMS1420S-55
	55ns	CHIP CARRIER	IMS1420W-55
IMS1421	40ns	CERAMIC DIP	IMS1421S-40
	40ns	CHIP CARRIER	IMS1421W-40
	50ns	CERAMIC DIP	IMS1421S-50
	50ns	CHIP CARRIER	IMS1421W-50

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