



GUARANTEED LOW SKEW CMOS CLOCK DRIVER/BUFFER

QS532807

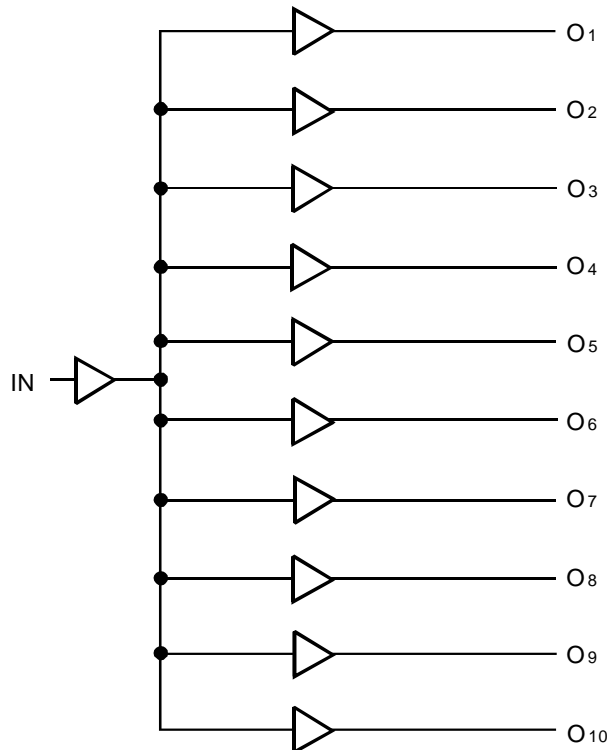
FEATURES:

- JEDEC compatible LVTTTL level
- 10 low skew clock outputs
- Clock input is 5V tolerant
- Pinout and function compatible with QS5807
- 25Ω on-chip resistors available for low noise
- Input hysteresis for better noise margin
- Guaranteed low skew < 0.5ns (max.) between outputs:
- Available in QSOP and SOIC packages

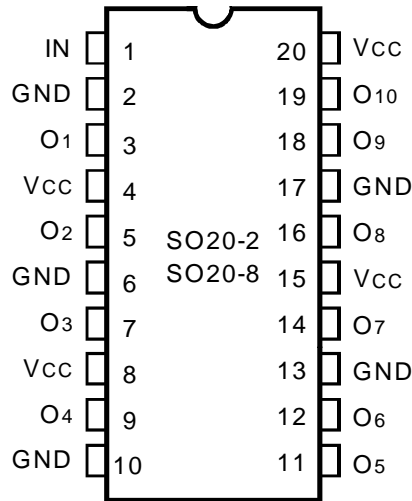
DESCRIPTION:

The QS532807 clock driver/buffer circuit can be used for clock buffering schemes where low skew is a key parameter. The QS532807 offers ten non-inverting outputs. Designed in IDT's proprietary QCMOS process, these devices provide low propagation delay buffering with less than 0.5ns on-chip skew. The QS532807 has on-chip series termination resistors for lower noise clock signals. The QS532807 series resistor version is recommended for driving unterminated lines with capacitive loading and other noise sensitive clock distribution circuits. These clock buffer products are designed for use in high-performance workstations, embedded and personal computing systems. Several devices can be used in parallel or scattered throughout a system for guaranteed low skew, system-wide clock distribution networks.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



QSOP/ SOIC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
V _{TERM} (2)	Supply Voltage to Ground	- 0.5 to +4.6	V
	DC Output Voltage V _{OUT}	- 0.5 to V _{CC} +0.5	V
V _{TERM} (3)	DC Input Voltage V _{IN}	- 0.5 to +7	V
V _{AC}	AC Input Voltage (pulse width ≤20ns)	-3	V
I _{OUT}	DC Output Current V _{IN} < 0	-20	mA
	DC Output Current Max. Sink Current/Pin	120	mA
T _{STG}	Storage Temperature	- 65 to +150	°C
T _J	Junction Temperature	150	°C

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} Terminals.
3. All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz, V_{IN} = 0V)

Pins	QSOP		SOIC		Unit
	Typ.	Max. (1)	Typ.	Max. (1)	
C _{IN}	3	6	5	7	pF

NOTE:

1. This parameter is guaranteed but not production tested.

PIN DESCRIPTION

Pin Names	I/O	Description
IN	I	Clock Input
Ox	O	Clock Outputs

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$

Symbol	Parameter	Test Conditions	Min.	Typ. ⁽¹⁾	Max.	Unit
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for All Inputs	2	1.7	5.5	V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW for All Inputs	-0.5	—	0.8	V
V _{IC}	Clamp Diode Voltage ⁽³⁾	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$	—	-0.7	-1.2	V
V _{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -100\mu\text{A}$	$V_{CC} - 0.2$	—	—	V
		$V_{CC} = \text{Min.}, I_{OH} = -8\text{mA}$	2.4	—	—	
V _{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 100\mu\text{A}$	—	—	0.2	V
		$V_{CC} = \text{Min.}, I_{OL} = 6\text{mA}$	—	—	0.4	
		$V_{CC} = \text{Min.}, I_{OL} = 8\text{mA}$	—	—	0.5	
I _{IN}	Input Leakage Current	$V_{CC} = \text{Max.}, V_{IN} = V_{CC}$ or GND	—	—	±1	μA
I _{OFF}	Input Power Off Leakage	$V_{CC} = 0\text{V}, V_{IN} = V_{CC}$ or GND	—	—	±1	μA
I _{OS}	Short Circuit Current ^(2,3)	$V_{CC} = \text{Max.}, V_{OUT} = \text{GND}$	-60	-195	—	mA
I _{ODH}	Output HIGH Current	$V_{CC} = 3.3\text{V}, V_{IN} = V_{IH}$ or $V_{IL}, V_O = 1.5\text{V}$	-50	-80	-200	mA
I _{ODL}	Output LOW Current	$V_{CC} = 3.3\text{V}, V_{IN} = V_{IH}$ or $V_{IL}, V_O = 1.5\text{V}$	50	112	200	mA
ΔV _T	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
R _{OUT}	Output Resistance ⁽⁴⁾	$V_{CC} = \text{Min.}, I_{OL} = 12\text{mA}$	—	28	—	Ω

NOTES:

1. Typical values are at $V_{CC} = 3.3\text{V}, T_A = 25^{\circ}\text{C}$.
2. Not more than one output should be used to test this high power condition. Duration is less than one second.
3. Guaranteed by design but not tested.
4. Output resistance represents the total output impedance of the logic device and includes added series termination resistance.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions	Typ. ⁽²⁾	Max.	Unit	
I _{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND}$ or V_{CC}	0.01	100	μA	
ΔI _{CC}	Supply Current per Input HIGH	$V_{CC} = \text{Max.}, V_{IN} = 3\text{V}$ Input toggling at 50% duty cycle	0.1	30	μA	
I _{CCD}	Dynamic Power Supply Current per Output ⁽¹⁾	$V_{CC} = \text{Max.},$ outputs Enabled	60	90	μA/MHz	
I _C	Total Power Supply Current Examples ^(1,3)	$V_{CC} = \text{Max.},$ Input at 50% duty cycle $f_i = 10\text{MHz}$	$V_{IN} = \text{GND}$ or V_{CC}	6	10	mA
		$V_{CC} = \text{Max.},$ Input at 50% duty cycle $f_i = 2.5\text{MHz}$	$V_{IN} = \text{GND}$ or V_{CC}	1.5	3	

NOTES:

1. Guaranteed by design but not tested. $C_L = 0\text{pF}$.
2. Typical values are for reference only. Conditions are $V_{CC} = 3.3\text{V}, T_A = 25^{\circ}\text{C}$.
3. $I_C = I_{CC} + (\Delta I_{CC})(D_H)(N_T) + I_{CCD}(f_o)(N_o)$
where:
D_H = Input Duty Cycle
N_T = Number of TTL HIGH inputs at D_H (one)
f_o = Output Frequency
N_o = Number of outputs at f_o (ten)

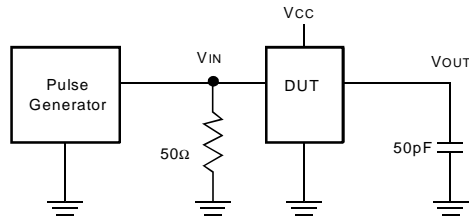
SWITCHING CHARACTERISTICS OVER OPERATING RANGET_A = -40°C to +85°C, V_{CC} = 3.3V ± 0.3VC_{LOAD} = 50pF (no resistor)

Symbol	Parameter ⁽¹⁾	Min.	Max.	Unit
tsk(01)	Skew between all outputs, same transition	—	0.5	ns
tsk(P)	Pulse Skew; skew between opposite transitions of the same output (t _{PHL} - t _{PLH})	—	0.5	ns
tsk(T)	Part-to-part skew ⁽²⁾	—	1	ns
t _{PLH} t _{PHL}	Propagation Delay ⁽³⁾ IN to O _x	1.5	5.2	ns
t _R	Output Rise Time, 0.8V to 2V	—	2	ns
t _F	Output Fall Time, 2V to 0.8V	—	2	ns

NOTES:

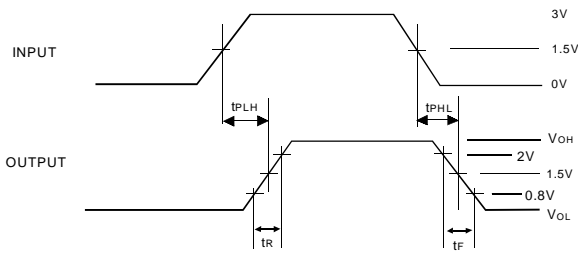
1. Skew parameters are guaranteed across temperature range, but not tested.
2. tsk(T) only applies to devices of the same transition, part type, temperature, power supply voltage, loading, and package.
3. The propagation delay range indicated by Min. and Max. specifications results from process and environmental variables. These propagation delays do not imply limit skew.

TEST CIRCUITS AND WAVEFORMS

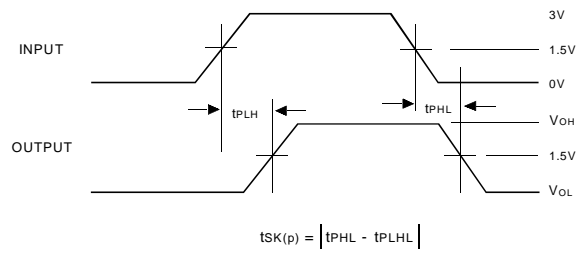


Pulse generator for all pulses: $f \leq 1.0\text{MHz}$; $t_F \leq 2.5\text{ns}$; $t_R \leq 2.5\text{ns}$

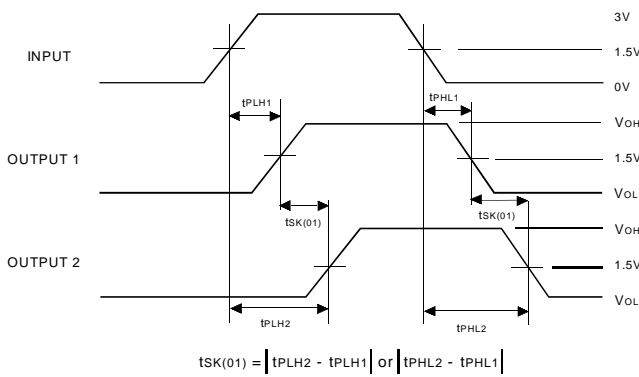
PROPAGATION DELAY



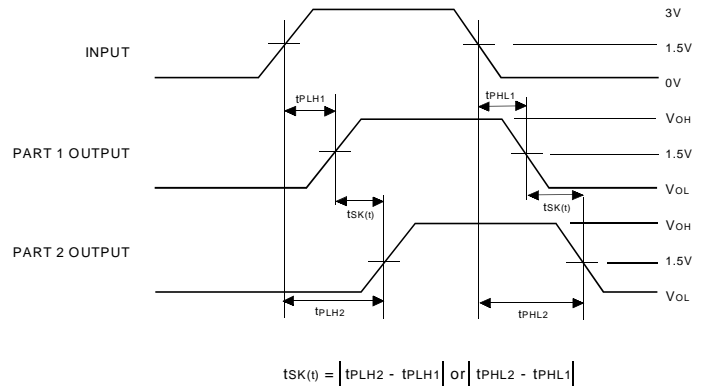
PULSE SKEW — $t_{SK(P)}$



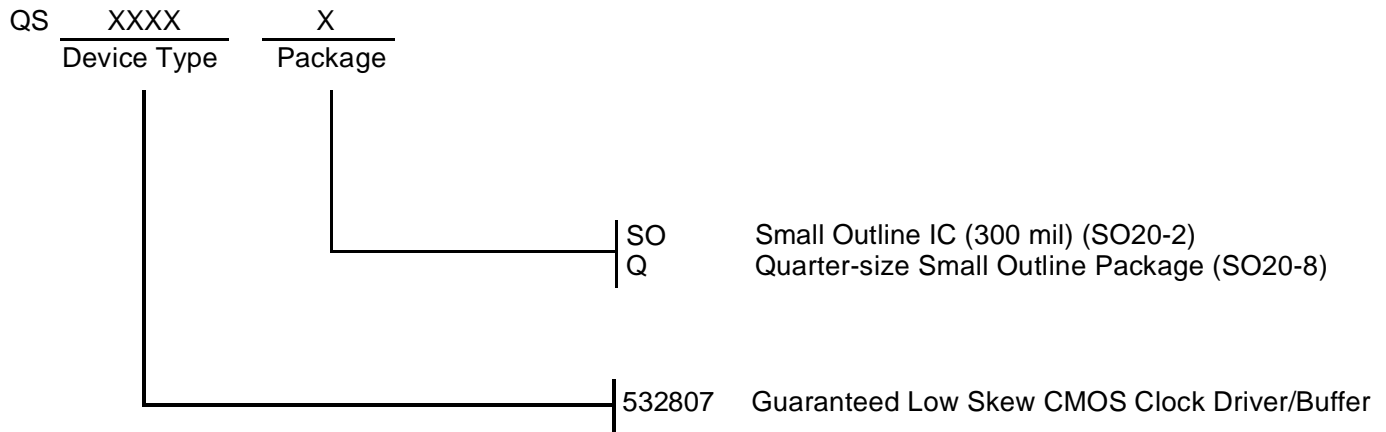
OUTPUT SKEW — $t_{SK(O1)}$



PART-TO-PART SKEW — $t_{SK(T)}$



ORDERING INFORMATION



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