



**FEATURES:**

- Bus switches provide zero delay paths
- Extended commercial range of -40°C to +85°C
- Low switch on-resistance: FST3xxx - 5Ω
- TTL-compatible input and output levels
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Available in PDIP, SOIC, QSOP, and TSSOP Packages
- Pin-compatible with FCT245

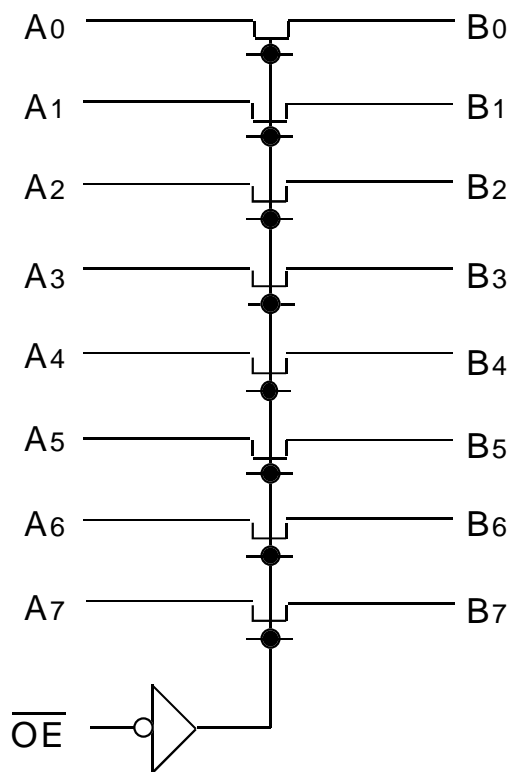
**DESCRIPTION:**

The FST3245 belongs to IDT's family of Bus switches. Bus switch devices perform the function of connecting or isolating two ports without providing any inherent current sink or source capability. Thus they generate little or no noise of their own while providing a low resistance path for an external driver. These devices connect input and output ports through an n-channel FET. When the gate-to-source junction of this FET is adequately forward-biased the device conducts or the resistance between input and output ports is small. Without adequate bias on the gate-to-source junction of the FET, the FET is turned off, therefore with no Vcc applied, the device has hot insertion capability.

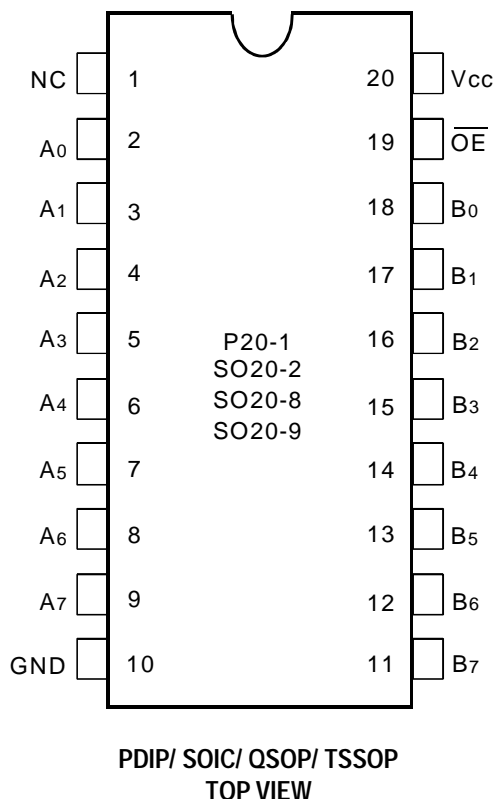
The low on-resistance and simplicity of the connection between input and output ports reduces the delay in this path to close to zero.

The FST3245 is an octal TTL-compatible bus switch. The  $\overline{OE}$  pin provides output enable control for all 8 bits. The direction control pin (DIR) of the FCT245 is replaced with a "No connect" (NC) in the FST3245. Bus switch devices provide an inherently bidirectional connection between ports, thus eliminating the purpose of the direction control pin.

**FUNCTIONAL BLOCK DIAGRAM**



**PIN CONFIGURATION**



### ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Max.	Unit
VTERM(2)	Terminal Voltage with Respect to GND	-0.5 to +7	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	Maximum Continuous Channel Current	128	mA

FST LINK

#### NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc, Control, and Switch terminals.

### CAPACITANCE (1)

Symbol	Parameter	Conditions(2)	Typ.	Unit
CIN	Control Input Capacitance		4	pF
CIO	Switch Input/Output Capacitance	Switch Off		pF

#### NOTES:

1. Capacitance is characterized but not tested.
2. TA = 25°C, f = 1MHz, VIN = 0V, VOUT = 0V

### DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Conditions: TA = -40°C to +85°C, Vcc = 5.0V ±5%

Symbol	Parameter	Test Conditions(1)	Min.	Typ.(2)	Max.	Unit
VIH	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs	2	—	—	V
VIL	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs	—	—	0.8	V
IiH	Input HIGH Current	Vcc = Max. Vi = Vcc Vi = GND	—	—	±1	µA
IiL	Input LOW Current		—	—	±1	
IoZH	High Impedance Output Current (3-State Output Pins)	Vcc = Max. Vo = Vcc Vo = GND	—	—	±1	µA
IoZL			—	—	±1	
Ios	Short Circuit Current	Vcc = Max., Vo = GND(3)	—	300	—	mA
VIK	Clamp Diode Voltage	Vcc = Min., IIN = -18mA	—	-0.7	-1.2	V
RON	Switch On Resistance(4)	Vcc = Max., Vo = 0V, ION = 30mA	—	5	7	Ω
		Vcc = Max., Vo = 2.4V, ION = 15mA	—	10	15	
Ioff	Input/Output Power Off Leakage	Vcc = 0V, VIN or Vo ≤ 4.5V	—	—	±1	µA
Icc	Quiescent Power Supply Current	Vcc = Max., Vi = GND or Vcc	—	0.1	3	µA

#### NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. Measured by voltage drop between ports at indicated current through the switch.

### PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$	Output Enable Input (Active LOW)
NC	No connect
A0-A7	A Port Bits
B0-B7	B Port Bits

### FUNCTION TABLE(1)

$\overline{OE}$	B0-7	Description
H	X	Disconnect
L	A0-7	Connect

#### NOTE:

1. H = HIGH  
L = LOW  
X = Don't Care

## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	1.5	mA
$I_{CCD}$	Dynamic Power Supply Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$ Outputs Open Enable Pin Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	30	40	$\mu A/$ MHz/ Switch
$I_C$	Total Power Supply Current <sup>(6)</sup>	$V_{CC} = \text{Max.}$ Outputs Open Enable Pin Toggling (8 Switches Toggling) $f_i = 10\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	2.4	3.2	mA
			$V_{IN} = 3.4$ $V_{IN} = \text{GND}$	—	2.7	4	

### NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0V$ ,  $+25^\circ\text{C}$  ambient.
- Per TTL driven input ( $V_{IN} = 3.4V$ ). All other inputs at  $V_{CC}$  or  $\text{GND}$ .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$   
 $I_C = I_{CC} + \Delta I_{CC} D_{HT} + I_{CCD} (f_i N)$   
 $I_{CC}$  = Quiescent Current  
 $\Delta I_{CC}$  = Power Supply Current for a TTL High Input ( $V_{IN} = 3.4V$ )  
 $D_{HT}$  = Duty Cycle for TTL Inputs High  
 $N_T$  = Number of TTL Inputs at  $D_H$   
 $I_{CCD}$  = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)  
 $f_i$  = Input Frequency  
 $N$  = Number of Switches Toggling at  $f_i$   
 All currents are in milliamps and all frequencies are in megahertz.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial:  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 5.0V \pm 5\%$

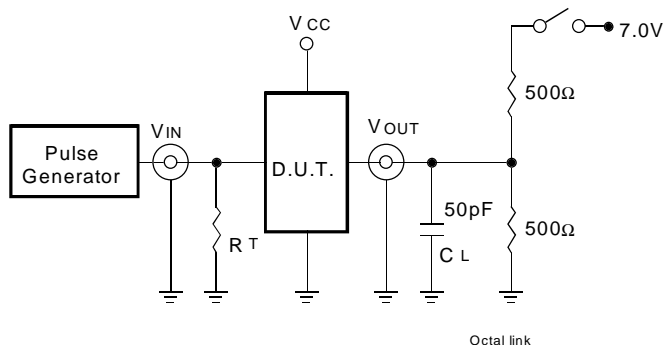
Symbol	Description	Condition <sup>(1)</sup>	Min. <sup>(2)</sup>	Typ.	Max.	Unit
$t_{PLH}$	Data Propagation Delay $A_i$ to $B_i$ , $B_i$ to $A_i^{(3,4)}$	$C_L = 50\text{pF}$ $R_L = 500\Omega$	—	—	0.25	ns
$t_{PZH}$	Switch Turn on Delay $\overline{OE}$ to $A_i$ , $B_i$		1.5	—	6.5	ns
$t_{PHZ}$	Switch Turn off Delay $\overline{OE}$ to $A_i$ , $B_i^{(3)}$		1.5	—	5.5	ns
$t_{PLZ}$						
$ Q_{CI} $	Charge Injection <sup>(5,6)</sup>		—	1.5	—	pC

### NOTES:

- See test circuit and waveforms.
- Minimum limits guaranteed but not tested.
- This parameter is guaranteed by design but not tested.
- The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 50 pF load. Since this time is constant and much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
- Measured at switch turn off, load = 50 pF in parallel with 10 M $\Omega$  scope probe,  $V_{IN} = 0$  volts.
- Characterized parameter. Not 100% tested.

## TEST CIRCUITS AND WAVEFORMS

### TEST CIRCUITS FOR ALL OUTPUTS



### SWITCH POSITION

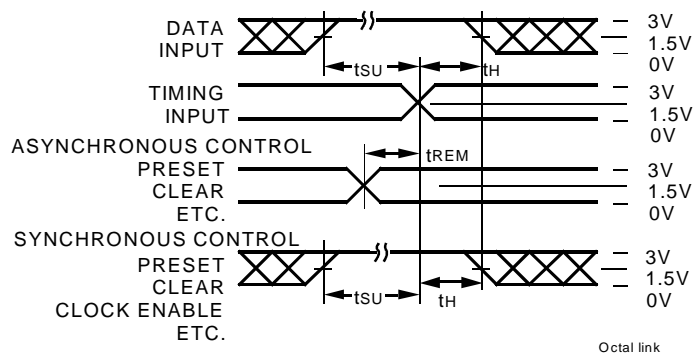
Test	Switch
Open Drain	Closed
Disable Low	
Enable Low	
All Other Tests	Open

FCT LINK

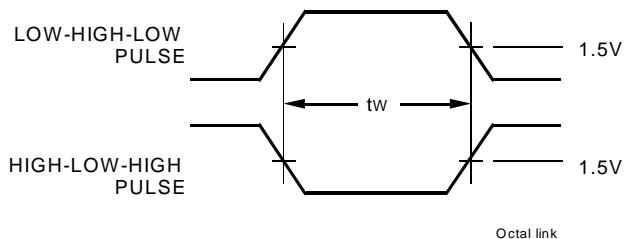
#### DEFINITIONS:

C<sub>L</sub> = Load capacitance: includes jig and probe capacitance.  
R<sub>T</sub> = Termination resistance: should be equal to Z<sub>OUT</sub> of the Pulse Generator.

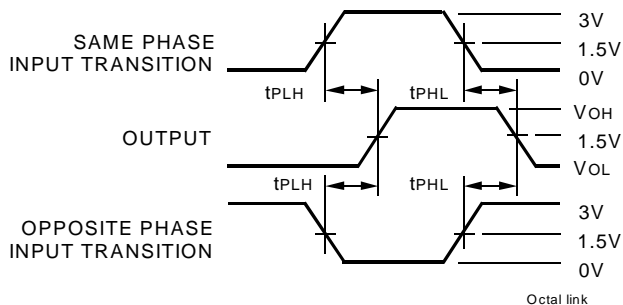
### SET-UP, HOLD, AND RELEASE TIMES



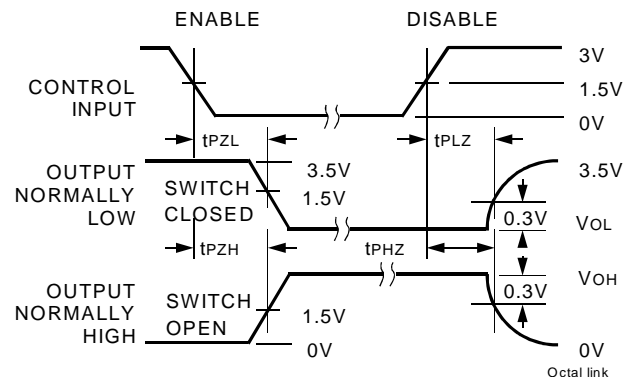
### PULSE WIDTH



### PROPAGATION DELAY



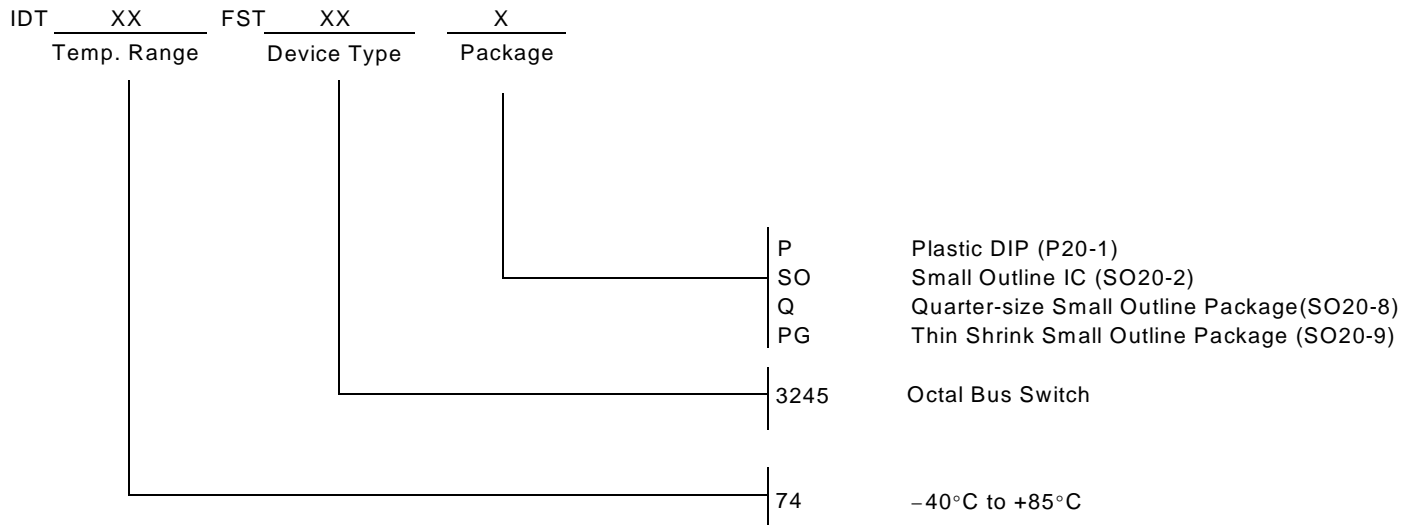
### ENABLE AND DISABLE TIMES



#### NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
- Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t<sub>r</sub> ≤ 2.5ns; t<sub>f</sub> ≤ 2.5ns

## ORDERING INFORMATION



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