FAST CMOS 16-BIT BIDIRECTIONAL TRANSCEIVER

IDT74FCT166245T/AT

FEATURES:
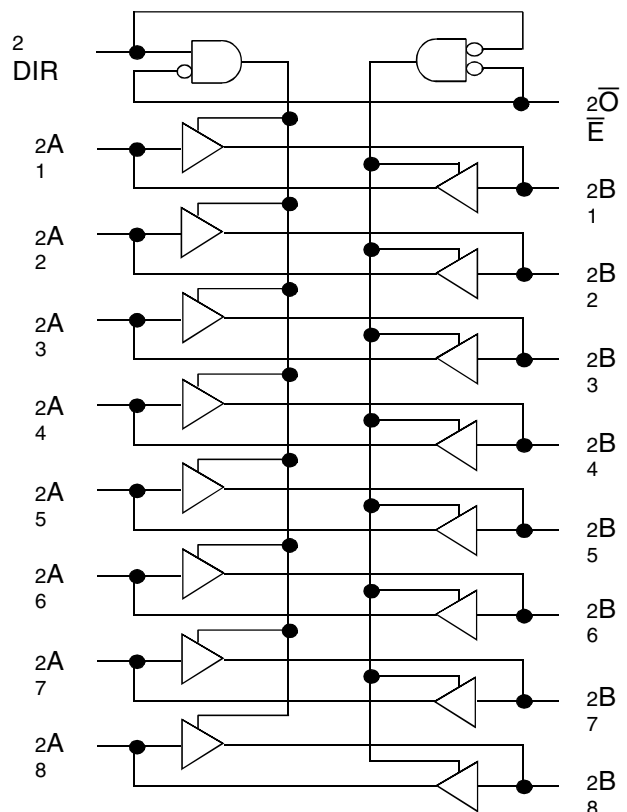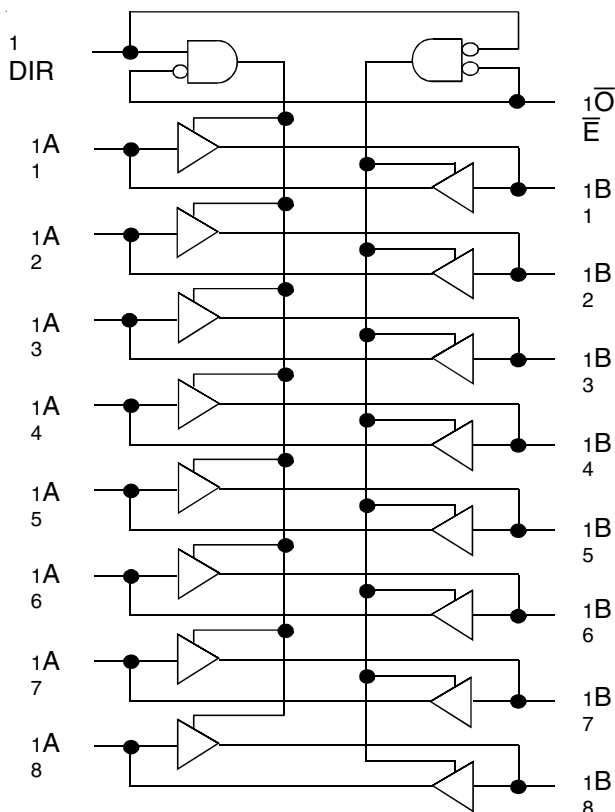
- 0.5 MICRON CMOS Technology
- High-speed, low-power CMOS replacement for ABT functions
- Typical $t_{SK(o)}$ (Output Skew) < 250ps
- Low input and output leakage ≤1µA (max.)
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Light drive A port: ±8mA
- High drive B port: +64mA, -32mA
- Minimal system switching noise
- Typical V_{OLP} (Output Ground Bounce) < 0.25V at V_{CC} = 5V, T_A = 25°C (A port switching)
- Power off disable outputs permit "live insertion"
- Available in SSOP and TSSOP packages

DESCRIPTION:

The FCT166245T 16-bit transceiver is built using advanced dual metal CMOS technology. These high-speed, low-power transceivers are ideal for synchronous communication between two buses (A and B). The Direction and Output Enable controls operate these devices as either two independent 8-bit transceivers or one 16-bit transceiver. The direction control pin (xDIR) controls the direction of data flow. The output enable pin (x$\overline{OE}$) overrides the direction control and disables both ports. All inputs are designed with hysteresis for improved noise margin.

The FCT166245T is suited for very low noise, point-to-point driving where there is a single receiver, or a light lumped load (<100pF). The buffers are designed to limit the output current to levels which will avoid noise and ringing on the signal lines without using external series terminating resistors. These parts have a ±8mA driver on the "A" Port and a +64/−32mA driver on the "B" Port, making them ideal for interfacing noisy system busses to noise sensitive interfaces.
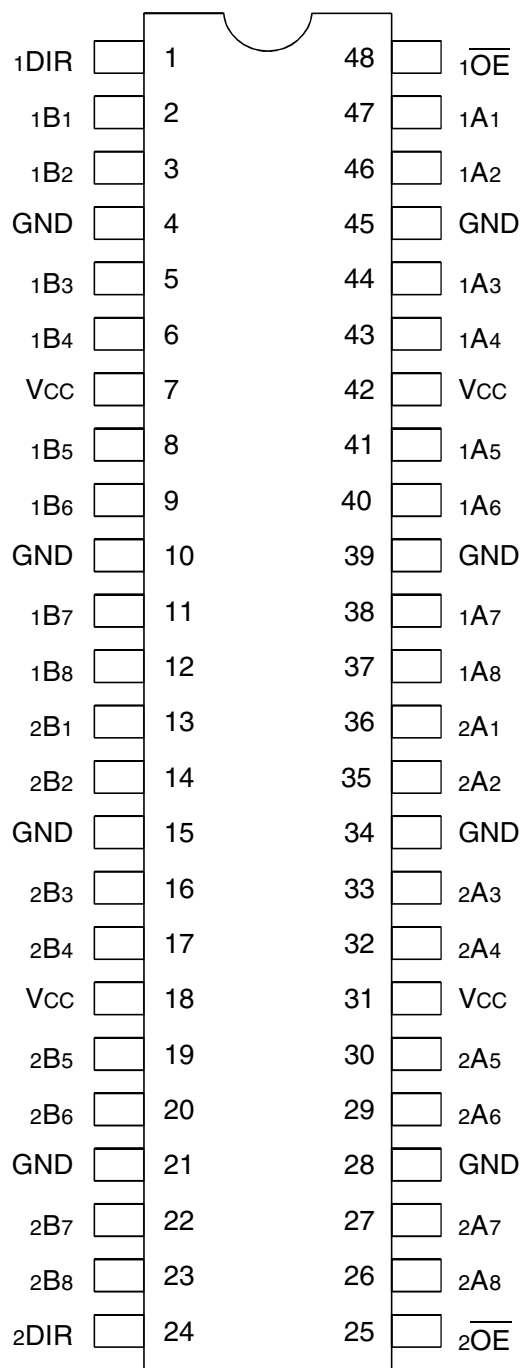
FUNCTIONAL BLOCK DIAGRAM

INDUSTRIAL TEMPERATURE RANGE

MAY 2001

DSC-5458/1

PIN CONFIGURATION

1DIR	1		48	1$\overline{OE}$
1B1	2		47	1A1
1B2	3		46	1A2
GND	4		45	GND
1B3	5		44	1A3
1B4	6		43	1A4
VCC	7		42	VCC
1B5	8		41	1A5
1B6	9		40	1A6
GND	10		39	GND
1B7	11		38	1A7
1B8	12		37	1A8
2B1	13		36	2A1
2B2	14		35	2A2
GND	15		34	GND
2B3	16		33	2A3
2B4	17		32	2A4
VCC	18		31	VCC
2B5	19		30	2A5
2B6	20		29	2A6
GND	21		28	GND
2B7	22		27	2A7
2B8	23		26	2A8
2DIR	24		25	2$\overline{OE}$

SSOP/ TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Description	Max	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	−0.5 to +7	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	−0.5 to V_{CC}+0.5	V
T_{STG}	Storage Temperature	−65 to +150	°C
I_{OUT}	DC Output Current	−60 to +120	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except FCT162XXX and FCT166XXXT(A port) Output and I/O terminals.
3. Output and I/O terminals for FCT162XXX and FCT166XXXT(A port).

CAPACITANCE (T$_A$ = +25°C, F = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	3.5	8	pF

NOTE:
1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
x$\overline{OE}$	3-State Output Enable Inputs (Active LOW)
xDIR	Direction Control Input
x A x	Side A Inputs or 3-State Outputs[1]
x B x	Side A Inputs or 3-State Outputs[2]

NOTES:
1. This is the ±8mA port.
2. This is the +64/-32mA port.

FUNCTION TABLE[1]

Inputs		Outputs
x$\overline{OE}$	DIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Z

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = –40°C to +85°C, V_{CC} = 5.0V ±10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[5]	V_{CC} = Max.	V_I = V_{CC}	—	—	±1	µA
	Input HIGH Current (I/O pins)[5]			—	—	±1	
I_{IL}	Input LOW Current (Input pins)[5]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[5]			—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State Output pins)[5]		V_O = 0.5V	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–80	–140	–250	mA
V_H	Input Hysteresis	—		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	5	500	µA

OUTPUT DRIVE CHARACTERISTICS (A-PORT)

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		16	48	96	mA
I_{ODL}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–16	–48	–96	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –8mA	2.4	3.3	—	V
V_{OH}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8mA	—	0.3	0.55	V

OUTPUT DRIVE CHARACTERISTICS (B-PORT)

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.5V[3]		–50	—	–180	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3mA	2.5	3.5	—	V
			I_{OH} = –15mA	2.4	3.5	—	
			I_{OH} = –32mA[4]	2	3	—	
V_{OH}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage	V_{CC} = 0V, V_{IN} or V_O ≤ 4.5V		—	—	±1	µA

NOTES:
1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. Duration of the condition can not exceed one second.
5. The test limit for this parameter is ±5µA at T_A = -55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open x$\overline{OE}$ = xDIR = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz	V_{IN} = V_{CC} V_{IN} = GND	—	0.6	1.5	mA
		50% Duty Cycle x$\overline{OE}$ = xDIR = GND One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	0.9	2.3	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz	V_{IN} = V_{CC} V_{IN} = GND	—	2.4	4.5[5]	
		50% Duty Cycle x$\overline{OE}$ = xDIR = GND Sixteen Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	6.4	16.5[5]	

NOTES:
1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

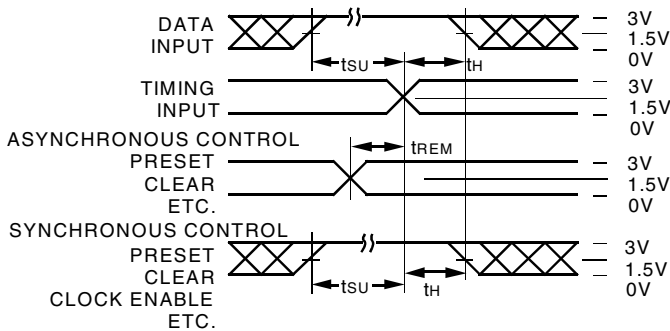| Symbol	Parameter	Condition[1]	FCT166245T		FCT166245AT		Unit
			Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay A to B	$C_L = 50pF$ $R_L = 500\Omega$	1.5	4.6	1.5	4.1	ns
t_{PLH} t_{PHL}	Propagation Delay B to A		1.5	7	1.5	4.6	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OE}$ to B		1.5	6.2	1.5	5.8	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OE}$ to A		1.5	9.5	1.5	6.2	ns
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{OE}$ to B		1.5	5	1.5	4.8	ns
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{OE}$ to A		1.5	7.5	1.5	5	ns
t_{PZH} t_{PZL}	Output Enable Time DIR to B[3]		1.5	6.2	1.5	5.8	ns
t_{PZH} t_{PZL}	Output Enable Time DIR to A[3]		1.5	9.5	1.5	6.2	ns
t_{PHZ} t_{PLZ}	Output Disable Time DIR to B[3]		1.5	5	1.5	4.8	ns
t_{PHZ} t_{PLZ}	Output Disable Time DIR to A[3]		1.5	7.5	1.5	5	ns
$t_{SK(o)}$	Output Skew[4]		—	0.5	—	0.5	ns

NOTES:
1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.
4. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
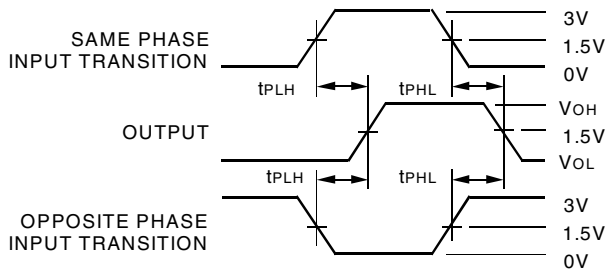
TEST CIRCUITS AND WAVEFORMS
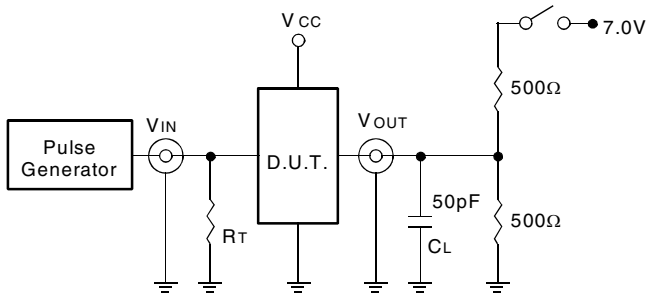
Test Circuits for All Outputs

SWITCH POSITION

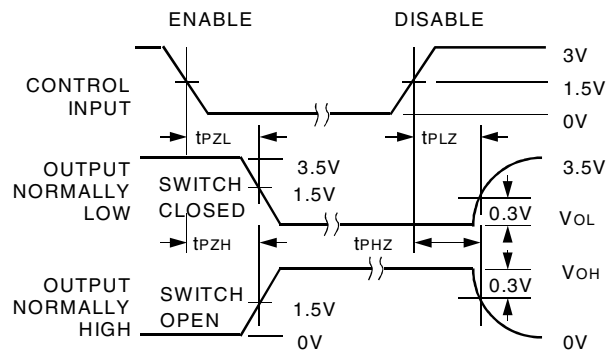| Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

Set-up, Hold, and Release Times

Pulse Width
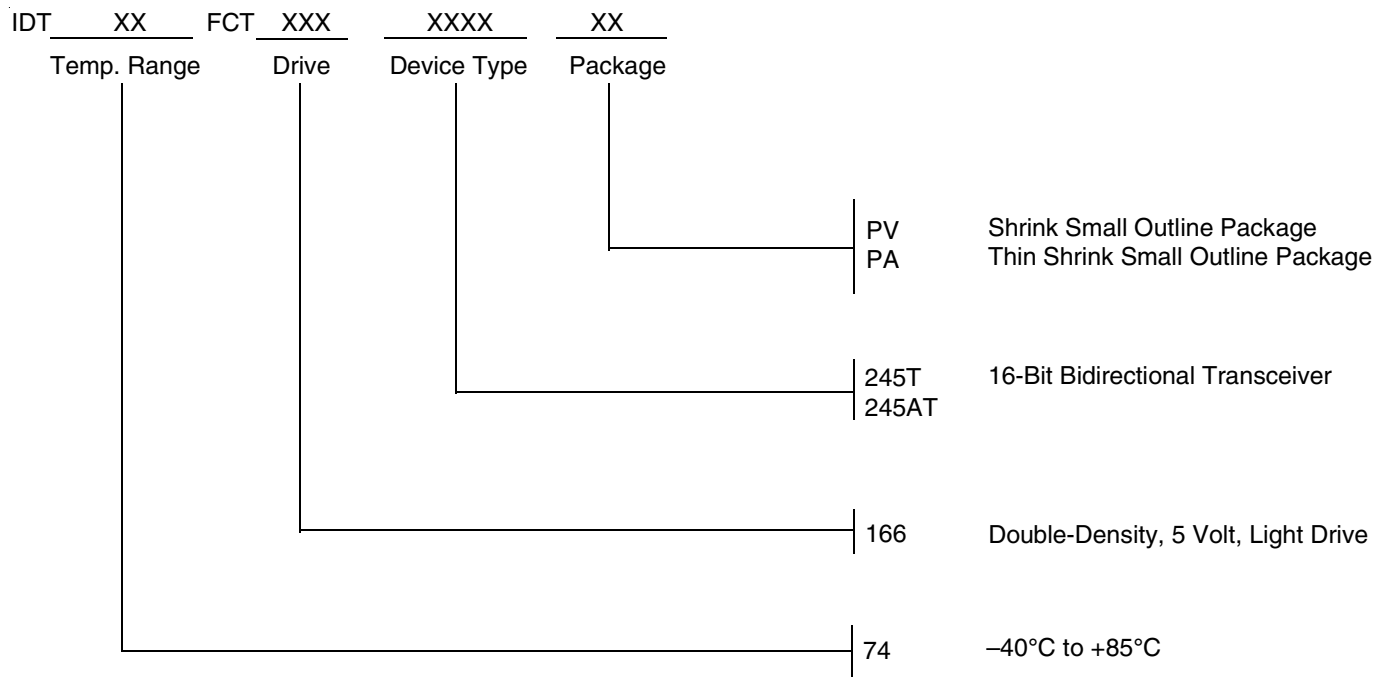

Propagation Delay
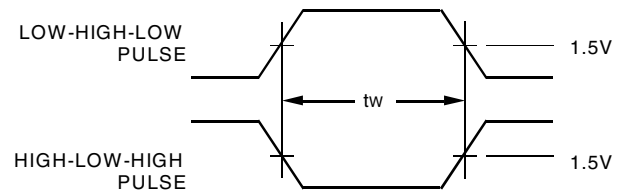
Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION

IDT <u>XX</u> FCT <u>XXX</u> <u>XXXX</u> <u>XX</u>
Temp. Range   Drive   Device Type   Package

PV	Shrink Small Outline Package
PA	Thin Shrink Small Outline Package
245T	16-Bit Bidirectional Transceiver
245AT	
166	Double-Density, 5 Volt, Light Drive
74	−40°C to +85°C