



Integrated Device Technology, Inc.

# CMOS STATIC RAM 16K (4K x 4-BIT)

IDT6168SA  
IDT6168LA

## FEATURES:

- High-speed (equal access and cycle time)
  - Military: 15/20/25/35/45/55/70/85/100ns (max.)
  - Commercial: 15/20/25/35ns (max.)
- Low power consumption
- Battery backup operation—2V data retention voltage (IDT6168LA only)
- Available in high-density 20-pin ceramic or plastic DIP, 20-pin SOIC, 20-pin CERPACK and 20-pin leadless chip carrier
- Produced with advanced CMOS high-performance technology
- CMOS process virtually eliminates alpha particle soft-error rates
- Bidirectional data input and output
- Military product compliant to MIL-STD-883, Class B

## DESCRIPTION:

The IDT6168 is a 16,384-bit high-speed static RAM organized as 4K x 4. It is fabricated using IDT's high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques,

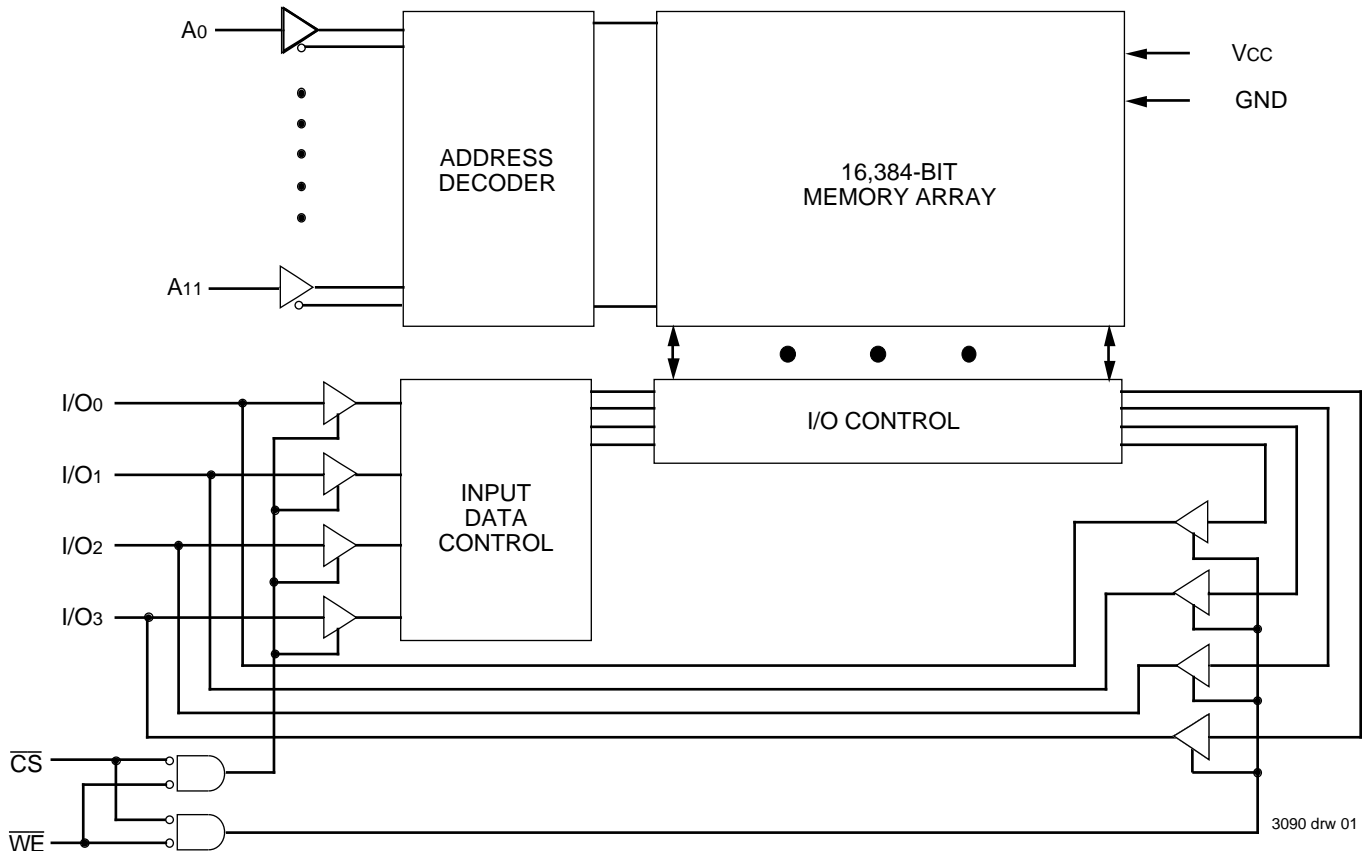
provides a cost-effective approach for high-speed memory applications.

Access times as fast 15ns are available. The circuit also offers a reduced power standby mode. When  $\overline{CS}$  goes HIGH, the circuit will automatically go to, and remain in, a standby mode as long as  $\overline{CS}$  remains HIGH. This capability provides significant system-level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1 $\mu$ W operating off a 2V battery. All inputs and outputs of the IDT6168 are TTL-compatible and operate from a single 5V supply.

The IDT6168 is packaged in either a space saving 20-pin, 300-mil ceramic or plastic DIP, 20-pin CERPACK, 20-pin SOIC, or 20-pin leadless chip carrier, providing high board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

## FUNCTIONAL BLOCK DIAGRAM



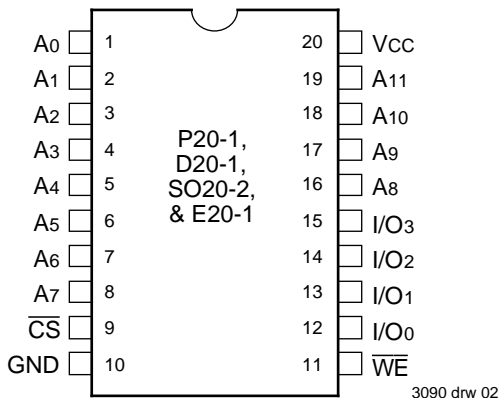
3090 drw 01

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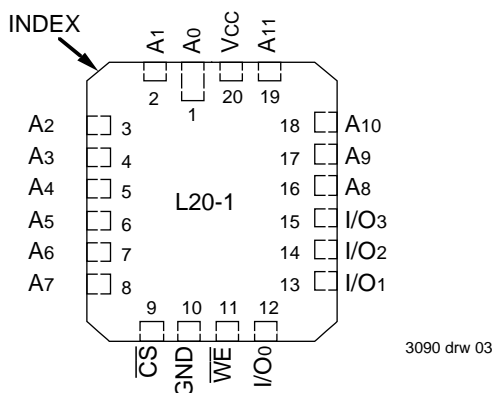
**MILITARY AND COMMERCIAL TEMPERATURE RANGE**

**MAY 1994**

## PIN CONFIGURATIONS



### DIP/SOIC/SOJ/CERPACK TOP VIEW



### LCC TOP VIEW

## PIN DESCRIPTIONS

Name	Description
A0-A11	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
I/O0-3	Data Input/Output
V <sub>CC</sub>	Power
GND	Ground

3090 tbl 01

## CAPACITANCE (T<sub>A</sub> = +25°C, F = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	7	pF
C <sub>I/O</sub>	I/O Capacitance	V <sub>OUT</sub> = 0V	7	pF

**NOTE:**  
1. This parameter is determined by device characterization, but is not production tested.

3090 tbl 02

## TRUTH TABLE<sup>(1)</sup>

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High-Z	Standby
Read	L	H	DOUT	Active
Write	L	L	DIN	Active

**NOTE:**

1. H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = Don't Care

3090 tbl 03

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Rating	Com'l.	Mil.	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T <sub>A</sub>	Operating Temperature	0 to +70	-55 to +125	°C
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	-65 to +135	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
I <sub>OUT</sub>	DC Output Current	50	50	mA

**NOTE:**

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

3090 tbl 04

## RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V <sub>IH</sub>	Input High Voltage	2.2	—	6.0	V
V <sub>IL</sub>	Input Low Voltage	-0.5 <sup>(1)</sup>	—	0.8	V

**NOTE:**

1. V<sub>IL</sub> (min.) = -3.0V for pulse width less than 20ns, once per cycle.

3090 tbl 05

## RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	VCC
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

3090 tbl 06

### DC ELECTRICAL CHARACTERISTICS<sup>(1)</sup>

(V<sub>CC</sub> = 5.0V ± 10%, V<sub>LC</sub> = 0.2V, V<sub>HC</sub> = V<sub>CC</sub> - 0.2V)

Symbol	Parameter	Power	6168SA15		6168SA20 6168LA20		Unit
			Com'l.	Mil.	Com'l.	Mil.	
ICC1	Operating Power Supply Current $\overline{CS} \leq V_{IL}$ , Outputs Open, V <sub>CC</sub> = Max., f = 0 <sup>(3)</sup>	SA	110	120	90	100	mA
		LA	—	—	70	80	
ICC2	Dynamic Operating Current $\overline{CS} \leq V_{IL}$ , Outputs Open, V <sub>CC</sub> = Max., f = f <sub>MAX</sub> <sup>(3)</sup>	SA	145	165	120	120	mA
		LA	—	—	100	110	
ISB	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$ , V <sub>CC</sub> = Max., Outputs Open, f = f <sub>MAX</sub> <sup>(3)</sup>	SA	55	60	45	45	mA
		LA	—	—	30	35	
ISB1	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$ , V <sub>CC</sub> = Max., V <sub>IN</sub> ≥ V <sub>HC</sub> or V <sub>IN</sub> ≤ V <sub>LC</sub> , f = 0 <sup>(3)</sup>	SA	20	20	20	20	mA
		LA	—	—	0.5	5	

3090 tbl 07

### DC ELECTRICAL CHARACTERISTICS (CONTINUED)<sup>(1)</sup>

(V<sub>CC</sub> = 5.0V ± 10%, V<sub>LC</sub> = 0.2V, V<sub>HC</sub> = V<sub>CC</sub> - 0.2V)

Symbol	Parameter	Power	6168SA25 6168LA25		6168SA35 6168LA35		6168SA45/55 6168LA45/55		6168SA70 <sup>(2)</sup> 6168LA70 <sup>(2)</sup>		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
ICC1	Operating Power Supply Current $\overline{CS} \leq V_{IL}$ , Outputs Open, V <sub>CC</sub> = Max., f = 0 <sup>(3)</sup>	SA	90	100	90	100	—	100	—	100	mA
		LA	70	80	70	80	—	80	—	80	
ICC2	Dynamic Operating Current $\overline{CS} \leq V_{IL}$ , Outputs Open, V <sub>CC</sub> = Max., f = f <sub>MAX</sub> <sup>(3)</sup>	SA	110	120	100	110	—	110	—	110	mA
		LA	90	100	80	90	—	80	—	80	
ISB	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$ , V <sub>CC</sub> = Max., Outputs Open, f = f <sub>MAX</sub> <sup>(3)</sup>	SA	35	45	30	35	—	35	—	35	mA
		LA	25	30	20	25	—	25/20	—	20	
ISB1	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$ , V <sub>CC</sub> = Max., V <sub>IN</sub> ≥ V <sub>HC</sub> or V <sub>IN</sub> ≤ V <sub>LC</sub> , f = 0 <sup>(3)</sup>	SA	3	10	3	10	—	10	—	10	mA
		LA	0.5	0.3	0.5	0.3	—	0.3	—	0.3	

**NOTES:**

1. All values are maximum guaranteed values.
2. Also available 85 and 100ns military devices.
3. f<sub>MAX</sub> = 1/t<sub>RC</sub>, only address inputs are cycling at f<sub>MAX</sub>. f = 0 means no address inputs are changing.

3090 tbl 08

### DC ELECTRICAL CHARACTERISTICS V<sub>CC</sub> = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT6168SA		IDT6168LA		Unit	
			Min.	Max.	Min.	Max.		
I <sub>LI</sub>	Input Leakage Current	V <sub>CC</sub> = Max., V <sub>IN</sub> = GND to V <sub>CC</sub>	MIL	—	10	—	5	μA
			COM'L	—	2	—	2	
I <sub>LO</sub>	Output Leakage Current	V <sub>CC</sub> = Max., $\overline{CS} = V_{IH}$ , V <sub>OUT</sub> = GND to V <sub>CC</sub>	MIL	—	10	—	5	μA
			COM'L	—	2	—	2	
V <sub>OL</sub>	Output LOW Voltage	IoL = 10mA, V <sub>CC</sub> = Min.	—	0.5	—	0.5	V	
		IoL = 8mA, V <sub>CC</sub> = Min.	—	0.4	—	0.4		
V <sub>OH</sub>	Output HIGH Voltage	IoH = -4mA, V <sub>CC</sub> = Min.	2.4	—	2.4	—	V	

3090 tbl 09

### DATA RETENTION CHARACTERISTICS (LA Version Only)

$V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V$

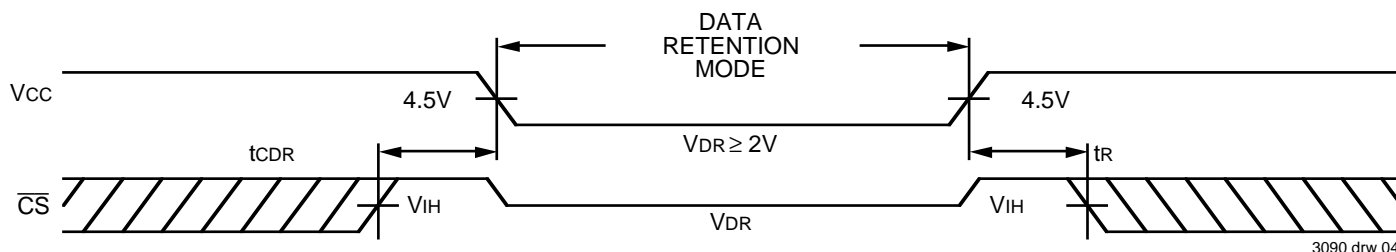
Symbol	Parameter	Test Condition	IDT6168LA			Unit	
			Min.	Typ. <sup>(1)</sup>	Max.		
VDR	V <sub>CC</sub> for Data Retention	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	2.0	—	—	V	
I <sub>CCDR</sub>	Data Retention Current		MIL.	—	0.5 <sup>(2)</sup>	100 <sup>(2)</sup>	μA
			COM'L.	—	1.0 <sup>(3)</sup>	150 <sup>(3)</sup>	μA
t <sub>CDR</sub> <sup>(5)</sup>	Chip Deselect to Data Retention Time		0	—	—	ns	
t <sub>R</sub> <sup>(5)</sup>	Operation Recovery Time		t <sub>RC</sub> <sup>(2)</sup>	—	—	ns	

**NOTES:**

1. T<sub>A</sub> = +25°C.
2. at V<sub>CC</sub> = 2V
3. at V<sub>CC</sub> = 3V
4. t<sub>RC</sub> = Read Cycle Time.
5. This parameter is guaranteed by device characterization, but is not production tested.

3090 tbl 10

### LOW V<sub>CC</sub> DATA RETENTION WAVEFORM

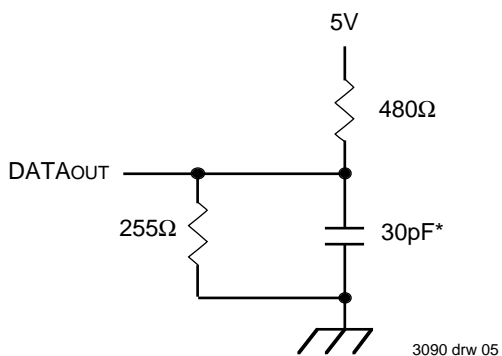


3090 drw 04

### AC TEST CONDITIONS

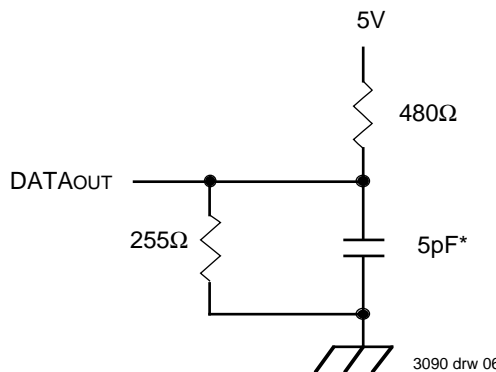
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

3090 tbl 11



3090 drw 05

Figure 1. AC Test Load



3090 drw 06

Figure 2. AC Test Load  
(for t<sub>CHZ</sub>, t<sub>CLZ</sub>, t<sub>WHZ</sub> and t<sub>OW</sub>)

\*Includes scope and jig capacitances

**AC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5.0V \pm 10\%$ , All Temperature Ranges)

Symbol	Parameter	6168SA15		6168SA20/25 6168LA20/25		Unit
		Min.	Max.	Min.	Max.	
<b>Read Cycle</b>						
t <sub>RC</sub>	Read Cycle Time	15	—	20/25	—	ns
t <sub>AA</sub>	Address Access Time	—	15	—	20/25	ns
t <sub>ACS</sub>	Chip Select Access Time	—	15	—	20/25	ns
t <sub>CLZ</sub> <sup>(2)</sup>	Chip Select to Output in Low-Z	3	—	5	—	ns
t <sub>CHZ</sub> <sup>(2)</sup>	Chip Deselect to Output in High-Z	—	8	—	10	ns
t <sub>OH</sub>	Output Hold from Address Change	3	—	3	—	ns
t <sub>PU</sub> <sup>(2)</sup>	Chip Select to Power-Up Time	0	—	0	—	ns
t <sub>PD</sub> <sup>(2)</sup>	Chip Deselect to Power-Down Time	—	15	—	20/25	ns

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**AC ELECTRICAL CHARACTERISTICS (CONTINUED)** ( $V_{CC} = 5.0V \pm 10\%$ , All Temperature Ranges)

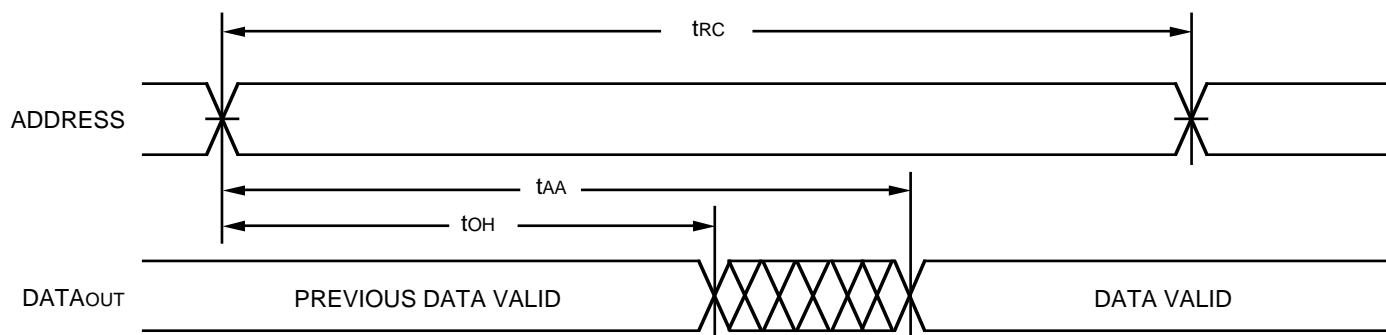
Symbol	Parameter	6168SA35 6168LA35		6168SA45 <sup>(1)</sup> 6168LA45 <sup>(1)</sup>		6168SA55 <sup>(1)</sup> 6168LA55 <sup>(1)</sup>		6168SA70 <sup>(1)</sup> 6168LA70 <sup>(1)</sup>		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>										
t <sub>RC</sub>	Read Cycle Time	35	—	45	—	55	—	70	—	ns
t <sub>AA</sub>	Address Access Time	—	35	—	45	—	55	—	70	ns
t <sub>ACS</sub>	Chip Select Access Time	—	35	—	45	—	55	—	70	ns
t <sub>CLZ</sub> <sup>(2)</sup>	Chip Select to Output in Low-Z	5	—	5	—	5	—	5	—	ns
t <sub>CHZ</sub> <sup>(2)</sup>	Chip Deselect to Output in High-Z	—	15	—	25	—	25	—	30	ns
t <sub>OH</sub>	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
t <sub>PU</sub> <sup>(2)</sup>	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	ns
t <sub>PD</sub> <sup>(2)</sup>	Chip Deselect to Power-Down Time	—	35	—	40	—	50	—	60	ns

**NOTES:**

1. -55°C to +125°C temperature range only. Also available 85ns and 100ns devices.
2. This parameter is guaranteed with AC Test load (Figure 2) by device characterization, but is not production tested.

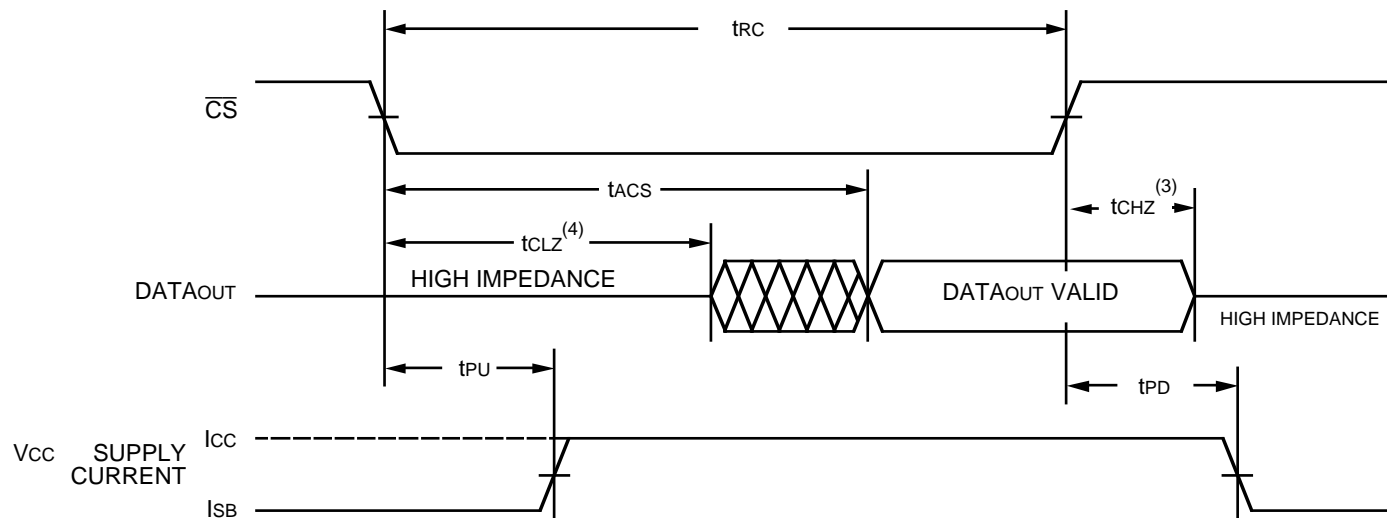
3090 tbl 13

**TIMING WAVEFORM OF READ CYCLE NO. 1<sup>(1, 2)</sup>**



3090 drw 07

### TIMING WAVEFORM OF READ CYCLE NO. 2<sup>(1, 3)</sup>



3090 drw 08

**NOTES:**

1. WE is HIGH for Read cycle.
2. CS is LOW for Read cycle.
3. Device is continuously selected, CS is LOW.
3. Address valid prior to or coincident with CS transition LOW.
4. Transition is measured ±200mV from steady state.

### AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6168SA15		6168SA20/25 6168LA20/25		Unit
		Min.	Max.	Min.	Max.	
<b>Write Cycle</b>						
tWC	Write Cycle Time	15	—	20	—	ns
tCW	Chip Select to End-of-Write	15	—	20	—	ns
tAW	Address Valid to End-of-Write	15	—	20	—	ns
tAS	Address Set-up Time	0	—	0	—	ns
tWP	Write Pulse Width	15	—	20	—	ns
tWR	Write Recovery Time	0	—	0	—	ns
tdW	Data Valid to End-of-Write	9	—	10	—	ns
tdH	Data Hold Time	0	—	0	—	ns
tWHZ <sup>(3)</sup>	Write Enable to Output in High-Z	—	6	—	7	ns
tOW <sup>(3)</sup>	Output Active from End-of-Write	0	—	0	—	ns

3090 tbl 14

**AC ELECTRICAL CHARACTERISTICS (CONTINUED)** ( $V_{CC} = 5.0V \pm 10\%$ , All Temperature Ranges)

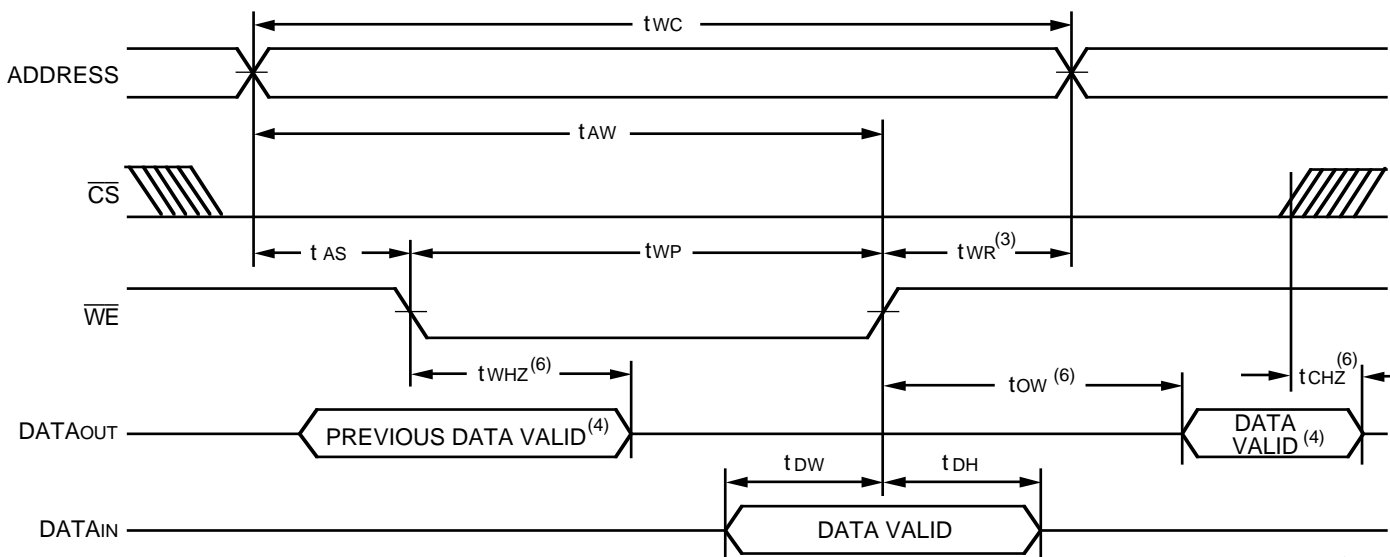
Symbol	Parameter	6168SA35 6168LA35		6168SA45 <sup>(2)</sup> 6168LA45 <sup>(2)</sup>		6168SA55 <sup>(2)</sup> 6168LA55 <sup>(2)</sup>		6168SA70 <sup>(2)</sup> 6168LA70 <sup>(2)</sup>		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
		<b>Write Cycle</b>								
t <sub>WC</sub>	Write Cycle Time	30	—	40	—	50	—	60	—	ns
t <sub>CW</sub>	Chip Select to End-of-Write	30	—	40	—	50	—	60	—	ns
t <sub>AW</sub>	Address Valid to End-of-Write	30	—	40	—	50	—	60	—	ns
t <sub>AS</sub>	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t <sub>WP</sub>	Write Pulse Width	30	—	40	—	50	—	60	—	ns
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t <sub>DW</sub>	DataValid to End-of-Write	15	—	20	—	20	—	25	—	ns
t <sub>DH</sub>	Data Hold Time	0	—	3	—	3	—	3	—	ns
t <sub>WHZ</sub> <sup>(3)</sup>	Write Enable to Output in High-Z	—	13	—	20	—	25	—	30	ns
t <sub>OW</sub> <sup>(3)</sup>	Output Active from End-of-Write	0	—	0	—	0	—	0	—	ns

**NOTES:**

1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only. Also available 85ns and 100ns devices.
3. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

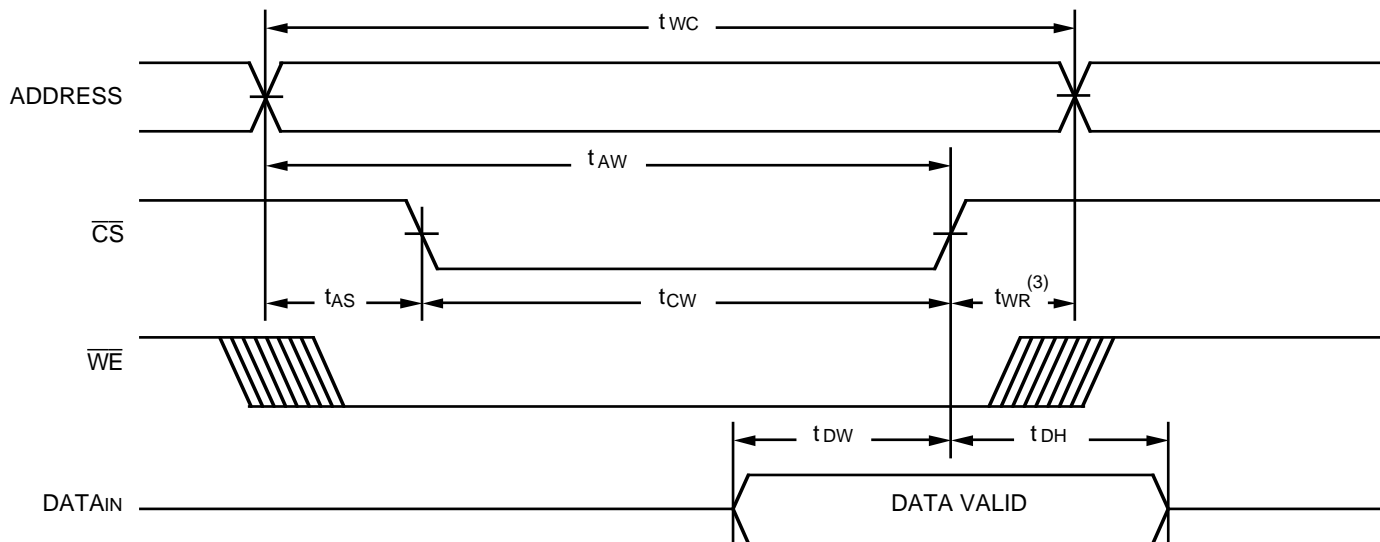
3090 tbl 15

**TIMING WAVEFORM OF WRITE CYCLE NO. 1 ( $\overline{WE}$  CONTROLLED TIMING)**<sup>(1, 2, 5)</sup>



3090 drw 09

**TIMING WAVEFORM OF WRITE CYCLE NO. 2 ( $\overline{CS}$  CONTROLLED TIMING)<sup>(1, 2, 5)</sup>**



3090 drw 10

**NOTES:**

1.  $\overline{WE}$  or  $\overline{CS}$  must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW  $\overline{CS}$  and a LOW  $\overline{WE}$ .
3.  $t_{WR}$  is measured from the earlier of  $\overline{CS}$  or  $\overline{WE}$  going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals should not be applied.
5. If the  $\overline{CS}$  LOW transition occurs simultaneously with or after the  $\overline{WE}$  LOW transition, the outputs remain in the high impedance state.
6. Transition is measured  $\pm 200\text{mV}$  from steady state.

**ORDERING INFORMATION**

IDT	6168	XX	XXX	XX	X	
	Device Type	Power	Speed	Package	Process/ Temperature Range	
					Blank B	Commercial (0°C to +70°C) Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B
					P D L SO E	300mil Plastic DIP (P20-1) 300mil Ceramic DIP (D20-1) Leadless Chip Carrier (L20-1) 300mil Small Outline IC, Gull Wing (SO20-2) 300mil CERPACK (E20-1)
					15 20 25 35 45 55 70 85 100	} Speed in nanoseconds
					SA LA	

3090 drw 11