HD64610

Calendar Clock IC

Description

The HD64610 is a calendar clock IC providing calendar clock functions and an 8-bit static-RAM interface. The HD64610 incorporates a crystal oscillator circuit dedicated to 32 kHz and a voltage clamp circuit enabling low current dissipation and battery back-up.

Features

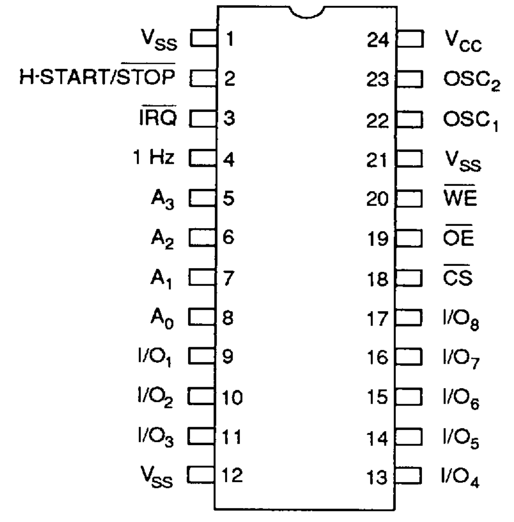
- 8-bit data bus (static-RAM interface); high-speed static-RAM timing equivalent to HM62256
- Oscillator circuit (Rf, Rd) incorporated
- Timer and calendar functions (BCD based); second, minute, hour, date, day of week, month, and year counters.
- 1 Hz to 64 Hz timer (binary based)
- START/STOP function
- 30-second ADJUST function
- Alarm interrupt and carry interrupt
- 1 Hz output
- Leap year automatic adjustment
- Battery backup (low power operation capability)

Type of Products

Type No.	Package
HD64610P	24 pin plastic DIP (DP-24)
HD64610FP	24 pin plastic SOP (FP-24D)

Note: WTR; Wide temperature range (–40 to +85°C) version is available. Please consult the Hitachi's sales office.

Pin Arrangement



(Top view)

Pin Description

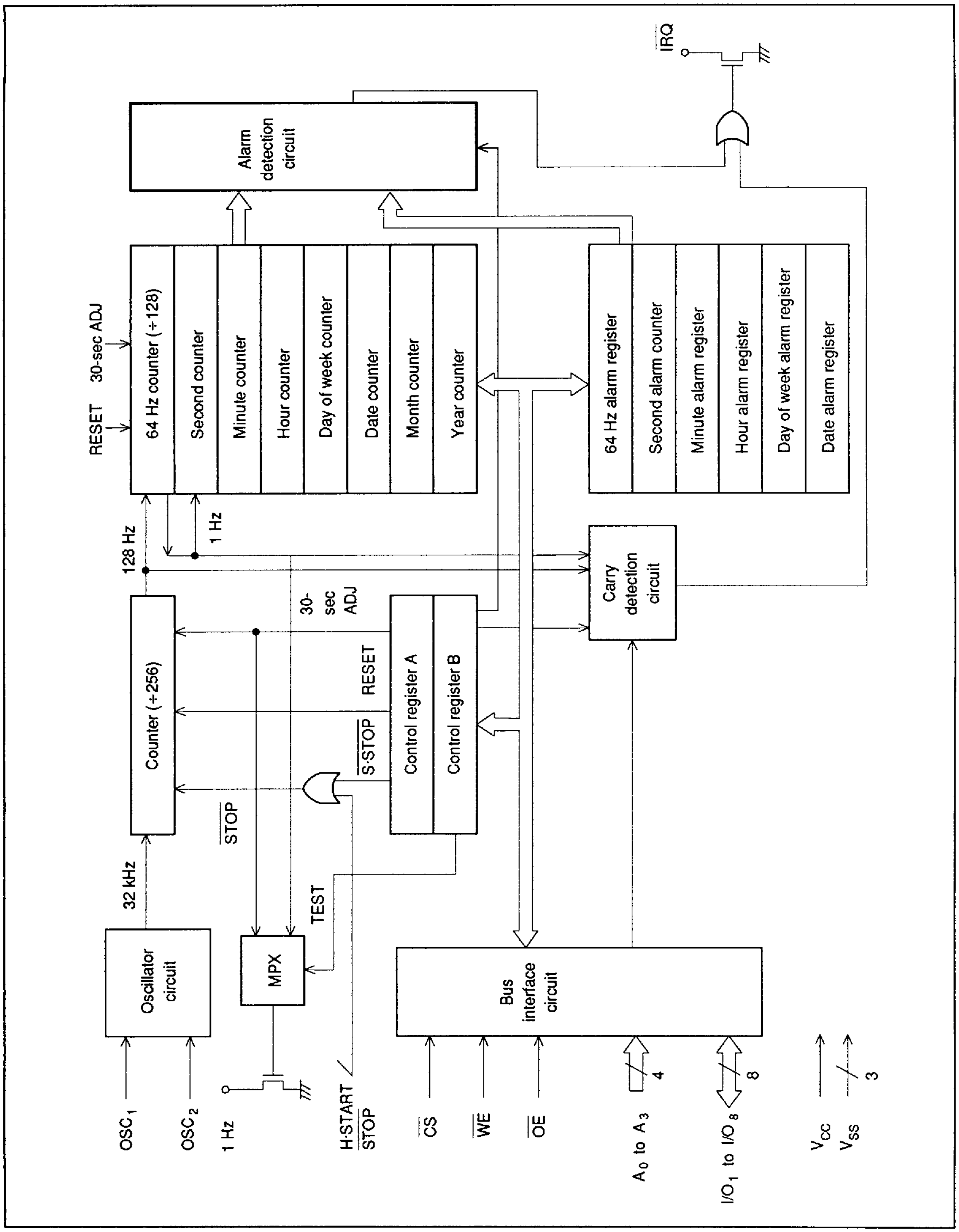
Function	Pin No.	Symbol	Pin Name	I/O	Description
Power supply	24	V_{CC}	V_{CC}	—	Connected to power supply. Supplies a voltage of 5 V ± 10% at power-on and bus access. Supplies 2 V or more during battery backup.
	1, 12, 21	V_{SS}	V_{SS}	—	Connected to ground (GND). As pin 1 and 12 are used independently within the HD64610, both connected to GND. Careful consideration must be taken in printed circuit board design to prevent a potential difference from being generated between these two pins at board mounting. Especially, pin 1 must supply a stable voltage since it supplies the basic voltage for the oscillator. Pin 21 is connected to GND to prevent the cross-talk noise from other signal (note) circuit.
Clock	22, 23	OSC_1 OSC_2	OSC_1 OSC_2	Input	Connects to a crystal resonator having a frequency of 32.768 kHz. (Refer to figure 7 for crystal resonator connection.)
MPU bus interface	5 – 8	$A_3 - A_0$	Address bus	Input	Inputs address information to access an internal register.
	9 – 11, 13 – 17	$I/O_1 - I/O_8$	Data bus	I/O	8-bit bi-directional data bus. These pins consist of three-state output buffers, and are placed in high impedance state except when both $\overline{CS}$ and $\overline{OE}$ are low and WE high (read accessing).
	18	$\overline{CS}$	Chip select	Input	Selects the HD64610. The MPU can access the HD64610 when CS is low.
	19	$\overline{OE}$	Output enable	Input	Asserted low when the MPU reads data from a register. If both OE and WE are asserted low, WE has priority over OE.
	20	$\overline{WE}$	Write enable	Input	Asserted low when the MPU writes data to a register.
	3	$\overline{IRQ}$	Interrupt request	Output	Requests an interrupt to the MPU. Asserted low when a carry or alarm interrupt occurs. IRQ can be reset by having the MPU write a 0 to the corresponding interrupt flag or enable bit of control register A. IRQ is an open drain pin and is placed in high impedance state if no interrupt is being requested. Connect pull-up resistors to IRQ with other interrupt request signals.

Pin Description (cont)

Function	Pin No.	Symbol	Pin Name	I/O	Description
Clock control	2	H·START/$\overline{\text{STOP}}$	Hardware start/stop	Input	Controls start/stop for clock and counter functions. This function is valid when S·START/$\overline{\text{STOP}}$ bit of control register B is 0. When S·START/$\overline{\text{STOP}}$ bit is 1, the HD64610 continues count operations regardless of this pin's status.
	4	1 Hz	1 Hz	Output	Monitors the 1 Hz internal basic clock. To monitor this 1 Hz signal, clear bit 3 of control register B to 0 and set bit 0 to 1 after power on. 1 Hz is an open drain pin.

Note: Pin 21 is not connected to an internal die. Therefore, this pin is open in DC measurement electrically. However this pin is very important to prevent the cross-talk noise from close signals in a high-frequency AC characteristics. Pin 21 must be connected to GND.

Block Diagram



System Configuration

The HD64610 generates a 1 Hz basic signal through a crystal oscillator (32.768 kHz) and a divider circuit. A divider circuits provides a detail clock data ranging from 64 Hz to 1 Hz, which can be read through the 64 Hz counter. A carry occurs and the clock data is updated on every 1 Hz interval in the second, minute, hour, day of week, date, month, and year counters. It is thus necessary to confirm that no carry has occurred during counter reading since the counter value is undefined when a carry occurs. Whether or not a carry has occurred can be checked by carry flag or interrupt.

An alarm can be generated any time under the control of the 64 Hz, second, minute, hour, day of week, and date alarm registers. Alarm time can be specified by setting the appropriate enable (ENB) bits and time bits of alarm registers. Whether or not an alarm has occurred can be confirmed by reading the alarm flag in control register A or by interrupt. Start/stop, reset, and 30-second adjustment of the divider circuit are also provided for clock counter control.

Table 1 Internal Registers

I/O Address	Register Name	Symbol	Read/ Write	Bits b7	b6	b5	b4	b3	b2	b1	b0
$ 0	64 Hz counter	64CNT	R	—	1 Hz	2 Hz	4 Hz	8 Hz	16 Hz	32 Hz	64 Hz
$ 1	Second counter	SECCNT	R/W	—	10 seconds			1 second			
$ 2	Minute counter	MINCNT	R/W	—	10 minutes			1 minute			
$ 3	Hour counter	HRCNT	R/W	—	—	10 hours		1 hour			
$ 4	Day of week counter	WKCNT	R/W	—	—	—	—	—	day of week		
$ 5	Date counter	DAYCNT	R/W	—	—	10 days		1 day			
$ 6	Month counter	MONCNT	R/W	—	—	—	10 months	1 month			
$ 7	Year counter	YRCNT	R/W	10 years				1 year			
$ 8	64 Hz alarm register	64AR	R/W	ENB	1 Hz	2 Hz	4 Hz	8 Hz	16 Hz	32 Hz	64 Hz
$ 9	Second alarm register	SECAR	R/W	ENB	10 seconds			1 second			
$ A	Minute alarm register	MINAR	R/W	ENB	10 minutes			1 minute			
$ B	Hour alarm register	HRAR	R/W	ENB	—	10 hours		1 hour			
$ C	Day of week alarm register	WKAR	R/W	ENB	—	—	—	—	day of week		
$ D	Date alarm register	DAYAR	R/W	ENB	—	10 days		1 day			
$ E	Control register A	CRA	R/W*	CF	—	—	CIE	AIE	—	—	AF
$ F	Control register B	CRB	R/W	RAM7	RAM6	RAM5	RAM4	TEST	ADJ	Reset	S·START/ STOP

Notes:

1. Reserved bits in the counters, alarm registers, and control register A cannot be written to and are always read as 0.
2. Days of the week are defined as follows:
   0 = Sunday, 1 = Monday, 2 = Tuesday,
   3 = Wednesday, 4 = Thursday, 5 = Friday,
   6 = Saturday
3. The second, minute, hour, date, month, and year counters and alarm registers contain BCD data.
4. The 64 Hz counter and 64 Hz alarm register contain binary data.
5. The hour is defined on a 24-hour basis.
6. The 64 Hz counter is a read only register and cannot be written to.

* Interrupt enable bits (b4, b3) of control register A can be read from or written to. Interrupt flags (b7, b0) can be read, but may only be written to as 0.

Function

1. Calendar Clock Function

   The HD64610 features a 64 Hz counter, which counts time in cycles from 64 Hz to 1 Hz provided from the divider circuit, and second, minute, hour, day of week, date, month, and year counters for calendar clock function. These counters are constructed by a series of ripple counters.

   The 64 Hz counter directly reads counter output from the divider circuit (without any conversion).

   It can measure and display time at about 8 msec resolution. The second, minute, hour, day of week, date, month, and year counters count up every second.

   Control registers include reset (Reset) and 30-second adjustment (ADJ) functions for calendar clock time adjustment. When these functions are performed, the divider circuit is cleared to 0 to start counting from 0. In 30-second adjustment, second data is rounded up or down with respect to 30-second intervals.

2. Time Measuring Function

   The HD64610 employs the H·START/$\overline{\text{STOP}}$ pin (external pin) and S·START/$\overline{\text{STOP}}$ bit of control register B to control count operation start and stop. The counters can be started or stopped by either the H·START/$\overline{\text{STOP}}$ pin or S·START/$\overline{\text{STOP}}$ bit according to the user application system. This function is useful for controlling accumulated system operation time.

3. Alarm Detection Function

   The HD64610 has an alarm detection function. An alarm setting can be specified in the 64 Hz, second, minute, hour, day of week and date alarm registers. The alarm flag of control register A is set when a calendar clock counter matches the specified alarm time. Each alarm register has an enable bit (ENB) in bit 7. Set ENB bit to 1 to enable an alarm register. In addition, if the alarm flag is set while the alarm interrupt enable bit is set, an interrupt request signal is generated at the $\overline{\text{IRQ}}$ pin. Note that the alarm flag keeps this value for a specified alarm time. That is, clearing the alarm flag bit during the specified alarm time is invalid (due to set the alarm flag by the internal circuit at this time). This point must be kept in mind during software design.

4. 1 Hz Basic Cycle Generation

   The HD64610 has a 1 Hz pin outputting a basic cycle which may be used for frequency adjustment or as a basic signal. This pin is an open-drain pin and waveforms can be monitored by connecting a resistor between it and V_{CC}.

Internal Registers

1. 64 Hz counter (64 CNT)

The 64 Hz counter counts cycles from 64 Hz to 1 Hz provided from the divider circuit. This is a read-only register and can not be written to. If a carry from 128 Hz step occurs when this register is read, bit 7 (CF bit) of control register A is set to 1 to indicate that a carry and read have occurred at the same time. In this case, since the read data is invalid, the 64 Hz counter must be read again after bit 7 of control register A is cleared by writing a 0 to it. Reserved bit of the 64 Hz counter is always read as 0. The divider circuit is cleared to 0 by RESET or ADJ (of control register B).

2. Second, minute, hour, day of week, date, month, and year counters

These counters are used for setting and counting timer calendar functions. Note that since each bit of these counters is undefined during power-on, these counters must be specified after stopping timer operation by bringing H·START/STOP signal low and clearing S·START/STOP bit to 0. Timers can be started by either bringing H·START/STOP high or setting the S·START/STOP bit to 1. Reserved bits of these counters are always read as 0. These registers are not be affected by ADJ and RESET. They contain BCD data and the hour is defined on a 24-hour basis. Days of week are defined as follows.

0 - Sunday, 1 - Monday, 2 - Tuesday,
3 - Wednesday, 4 - Thursday, 5 - Friday,
6 - Saturday

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Cycle (Hz)	—	1	2	4	8	16	32	64
Read/Write	R	R	R	R	R	R	R	R
Reset, ADJ	—	0	0	0	0	0	0	0

Bit	b7	b6	b5	b4	b3	b2	b1	b0	Valid range (BCD)
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Second counter	—	10 seconds			1 second				00 – 59
Minute counter	—	10 minutes			1 minute				00 – 59
Hour counter	—	—	10 hours		1 hour				00 – 23
Day of week counter	—	—	—	—	—	day of week			00 – 06
Date counter	—	—	10 days		1 day				00 – 31
Month counter	—	—	—	10 months	1 month				00 – 12
Year counter	10 years				1 year				00 – 99

Notes: 1. Year counter indicates last 2 digits of the year (A.D).
2. Remainder 0 obtained by dividing the year counter value by 4 identifiers leap year.
3. Set these counters within the valid range. Counter operation can not be assured if the counter is set outside the valid range. Remember that date count setting varies according to month and leap year.

3. 64 Hz, second, minute, hour, day of week, and date alarm registers

These registers are used for alarm timers. Set all registers after power-on since each bit in these alarm registers is undefined after power-on. If alarm registers, whose ENB bits are set to 1, match their corresponding counters, the alarm flag (of control register A) is set to 1. These registers are not be affected by ADJ and RESET. The 64 Hz alarm register and the day of week alarm register contain binary data and the others contain BCD data. The hour is defined on a 24-hour basis. Days of week are defined as follows.

0 - Sunday, 1 - Monday, 2 - Tuesday,
3 - Wednesday, 4 - Thursday, 5 - Friday,
6 - Saturday

4. Control register A (CRA)

Control register A (CRA) indicates carry and alarm status and enables carry and alarm interrupts. Initialize the CRA register by writing a specified value to it since all bits are undefined after power-on reset. The flag bits in the CRA register are set by the clock circuit asynchronously. Note that they must be cleared by writing a 0 to them by software. In addition, a bit set instruction which performs read-modify-write operation and bit clear instruction cannot be used for CRA register handling since a flag bit may set after reading. Reserved bits are always read as 0. The CRA register is not affected by RESET.

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
64 Hz alarm register	ENB	1 Hz	2 Hz	4 Hz	8 Hz	16 Hz	32 Hz	64 Hz
Second alarm register	ENB	10 seconds			1 second			
Minute alarm register	ENB	10 minutes			1 minute			
Hour alarm register	ENB	—	10 hours		1 hour			
Day of week alarm register	ENB	—	—	—	—	day of week		
Date alarm register	ENB	—	10 days		1 day			

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Read/Write	R/W*1	—	—	R/W	R/W	—	—	R/W*1
Bit name	CF	—	—	CIE	AIE	—	—	AF

Carry flag (CF)
0: No carry and no 64 Hz counter read during a carry occurrence.
1: A carry or 64 Hz counter read during a carry occurrence.

Carry interrupt enable
0: Disabled 1: Enabled

Alarm interrupt enable
0: Disabled 1: Enabled

Alarm flag
0: Counter and alarm register do not match.
1: Counter and alarm register match.

Note: *1 When b7 and b0 are 1, they can be cleared by writing 0 to them; however, a 1 cannot be written to them when they are 0.

Bit 7 (carry flag): The carry flag is set to 1 by hardware under the following conditions.

1) A carry occurs
2) Count time of the 64 Hz counter and 64 Hz register read access occur simultaneously.

The carry flag bit cannot be set by writing a 1 to it. This bit is cleared by writing a 0 to it during a period other than the carry period. See Counter Read Procedure for details.

CF (carry flag)

0: After clearing b7 to 0, no carry occurs and no request to read 64 Hz counter occurs at the 64 Hz carry period.
1: After clearing b7 to 0, a carry or read during 64 Hz carry has occurred.

b6, b5, b2, and b1: These bits are reserved and are always read as 0.

Bit 4 (carry interrupt enable): When the carry interrupt enable bit is set to 1, the $\overline{IRQ}$ pin is asserted low if the carry flag is set due to a carry occurrence. Here, the $\overline{IRQ}$ pin may be negated high by clearing the carry flag to 0. (The $\overline{IRQ}$ pin must be pulled up since it is an open-drain output pin.) If this bit is cleared to 0, the $\overline{IRQ}$ pin is not affected by carry flag status.

CIE (carry interrupt enable)

0: The $\overline{IRQ}$ pin is negated high regardless of carry flag status (disable).
1: The $\overline{IRQ}$ pin is asserted low if the carry flag is 1 (enable).

Bit 3 (alarm interrupt enable): When the alarm interrupt enable bit is set to 1, the $\overline{IRQ}$ pin is asserted low if the alarm flag is set due to an alarm occurrence. Here, the $\overline{IRQ}$ pin may be negated high by clearing the alarm flag to 0. (The $\overline{IRQ}$ pin must be pulled up since it is an open-drain output pin.) If the alarm interrupt enable bit is cleared to 0, the $\overline{IRQ}$ pin is not affected by alarm flag status.

AIE (Alarm interrupt enable)

0: The $\overline{IRQ}$ pin is negated high regardless of alarm flag status (disabled).
1: The $\overline{IRQ}$ pin is asserted low if the alarm flag bit is 1 (enabled).

Bit 0 (alarm flag): When timer counters match the alarm time specified in alarm registers whose ENB bits are set to 1, the alarm flag is set to 1 by hardware. Note that the alarm flag cannot be set to 1 by writing a 1 to it. The alarm flag is cleared to 0 by writing a 0 to it during a period other than the alarm generation period.

AF (alarm flag)

0: Alarm registers and timer counters do not match after reset.
1: Alarm registers whose ENB bits are set to 1 and corresponding timer counter match.

5. Control register B (CRB)

   The control register B (CRB) must be initialized by writing data to it since all bits are undefined after power-on reset. The CRB register contains the ADJ bit for 30-second adjustment, the RESET bit for the divider circuit, S·START/$\overline{STOP}$ bit for start or stop, and 4 RAM bits. No bits are affected by RESET.

Bit 7 – bit 4 (RAM7 – RAM4): The RAM7 – RAM4 bits can be used as RAM or flags by writing 1 or 0.

Bit 3 (TEST): This bit must be cleared to 0.

Bit 2 (ADJ): The ADJ bit is used for 30-second adjustment (ADJ function). If the ADJ bit is set to 1, 30-second adjustment is performed: time less than 30 seconds is truncated to as 0 second and that greater or equal to 30 seconds is raised to 1 minute. The divider circuit is reset at this time. After 30-second adjustment, the ADJ bit is cleared to 0. If a 0 is written to this bit, the HD64610 is unaffected.

ADJ

0: Normal timer operation
1: 30-second adjustment

Bit 1 (Reset)

The reset bit is used to initialize the divider circuit. Even if a 0 is written to this bit, the HD64610 is unaffected. After reset operation, the reset bit is automatically cleared to 0 and subsequent writing becomes available.

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Read/Write	R/W	R/W	R/W	R/W	R/W[1]	R/W[2]	R/W[2]	R/W
Bit name	RAM7	RAM6	RAM5	RAM4	TEST	ADJ	Reset	S·START/$\overline{\text{STOP}}$

RAM 7 to 4

TEST
0: Normal operation mode
1: Test mode

ADJ
0: Normal operation mode
1: 30-second adjustment

Reset
0: Normal operation mode
1: Divider circuit reset

S·START/$\overline{\text{STOP}}$
0: Timer stops when H·START/$\overline{\text{STOP}}$ is low
1: Timer operation

Notes: 1. Always write a 0 to this bit.
2. If a 1 is written to these bits, it remains 1 for a certain period of function executed and then cleared to 0. While the bit is 1, a 0 cannot be write to it.

Reset

0: Normal timer operation
1: Divider circuit reset

Bit 0 (S·START/STOP): The S·START/STOP bit is used to control stop and restart of the counters. Stop and reset operation are controlled by the combination of H·START/STOP pin and S·START/STOP bit status. When the H·START/STOP pin is high, the counters always operate regardless of the S·START/STOP bit status.

On the other hand, when the H·START/STOP pin is low, counter operation is controlled by the S·START/STOP bit as follows:

1. If the S·START/STOP bit is cleared to 0, the counters stop operating.
2. If the S·START/STOP bit is set to 1, the counters continue operation.

Relationship between counter operation, the H·START/STOP) pin, and the S·START/STOP bit is shown below.

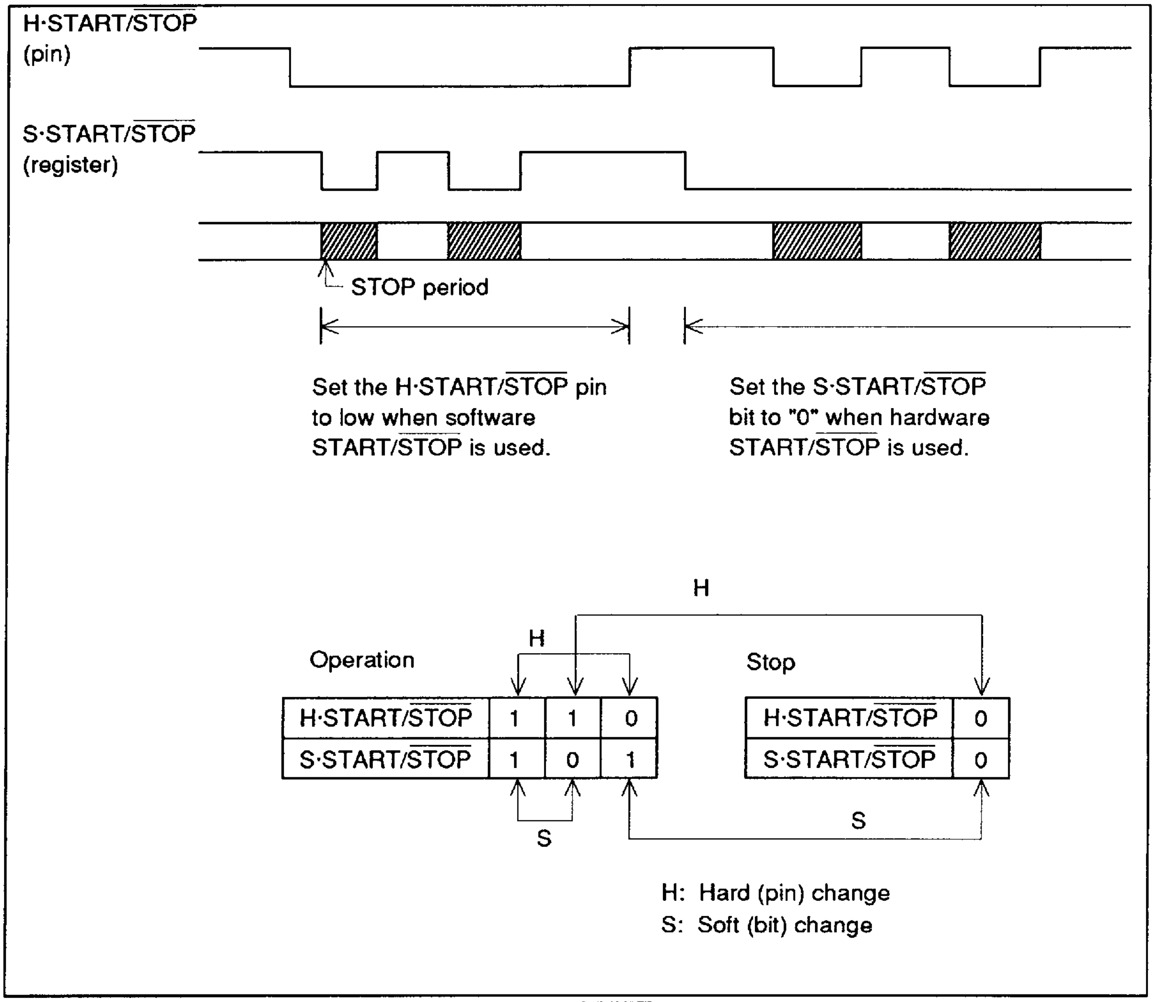


Figure 1 S·START/STOP Bit Function

S·START/$\overline{\text{STOP}}$

0: The timer stops operating when H·START/$\overline{\text{STOP}}$ = low, normal timer operation when H·START/$\overline{\text{STOP}}$ = high
1: Normal timer operation

Operational Description

1. Oscillator circuit startup at power on

   The HD64610 incorporates a crystal oscillator circuit. For a crystal oscillator circuit, oscillation startup characteristics at power-on is an important factor. The following describes oscillator circuit startup procedure.

   a) Power-on. (V_{CC} = 5 V ± 10%, T_a = –20 to +75°C)

   b) Bit 3 of the CRB register is cleared to 0 to specify normal operation mode.

   c) Wait until the crystal oscillator starts up. (t_{osc}).

   d) After registers are set, the HD64610 can be used as a timer calendar.

   The above procedure is used only at power on. If the system power supply is turned on or off (the battery backup power supply is used when system power supply is off), follow the specifications for the low voltage data retention waveform. The frequency of this crystal oscillator circuit can be checked by oscilloscope or frequency counter by connecting a pull-up resistor at the 1 Hz pin.

2. Initialization of registers after power on

   All HD64610 registers should be initialized after power on since the HD64610 has no pins for register reset. The following items should be noted before initializing.

   a) Undefined $\overline{\text{IRQ}}$ pin

   A carry or alarm interrupts may occur since the HD64610 registers are undefined after power on. A CPU must not accept the interrupt until all registers have been initialized by system software.

   b) Undefined calendar clock operation

   Bit 3 (TEST) of the CRB register is undefined after power on. Write 0 to the bit before utilizing timer functions since the HD64610 is in test mode (non-normal operation) when bit 3 is set to 1.

   c) Undefined counter START/$\overline{\text{STOP}}$

   Bit 0 (S·START/$\overline{\text{STOP}}$) of the CRB register is undefined after power on. Since counter start or stop is controlled by logical OR of bit 0 and the external pin H·START/$\overline{\text{STOP}}$, set a value accordingly.

3. Timer setting procedure

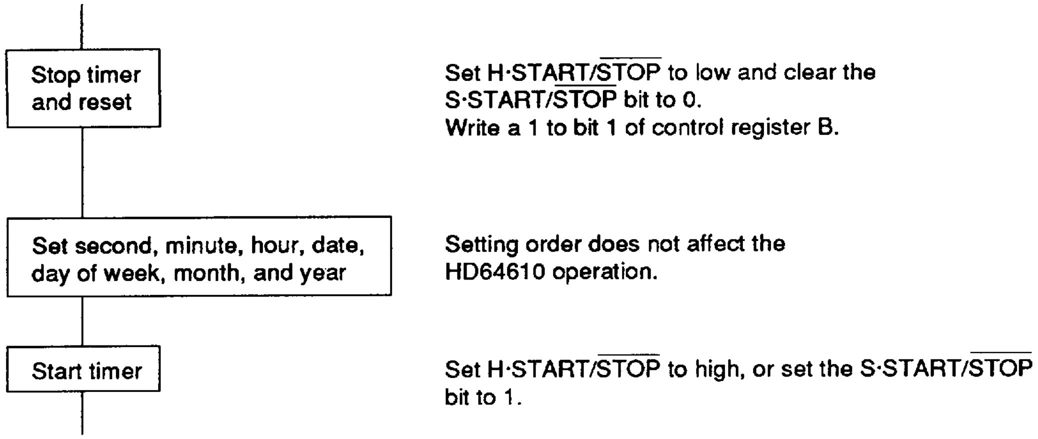
   Figure 2 shows a timer setting procedure.

   a) A procedure to set timers when stopped. This method is useful when all the calendar clocks are switched. It is easy to program timer settings with this method.

   b) A procedure to set timers during operation. This method is useful when only parts of the calendar clock function need to be switched (e.g. only seconds or hours are switched). In this case, the HD64610 shows the writing status with the carry flag.

   If a carry occurs during a write operation, write data is automatically updated, resulting in different specified data and write data. Accordingly, when a carry flag is set to 1, rewriting must be performed. An interrupt can also be used to check the carry flag status.

a) Setting counters after the divider has been reset



b) Setting counters (second, minute, hour, date, day of week, month, and year) during clock operation.

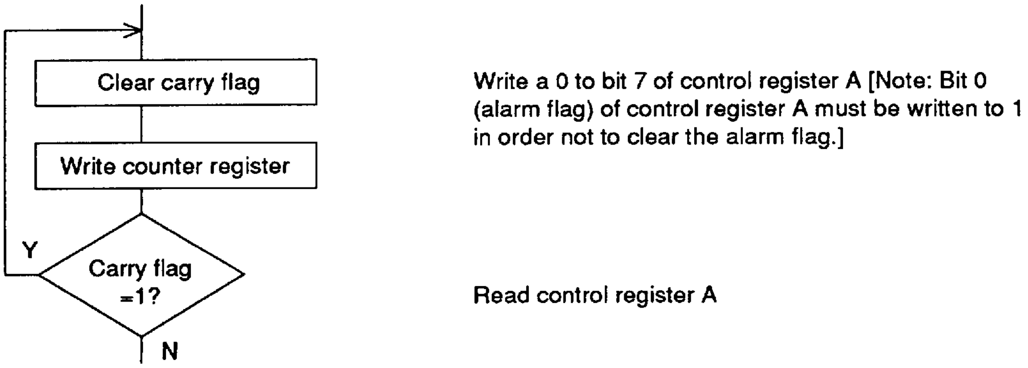


Figure 2 Timer Setting Procedure

Note: Carry of a second, minute, hour, day of week, month and year occurs during 125 μsec on every second. Therefore, if a carry is detected during a write operation, a correct write operation can be performed after a wait of at least 125 μsec. Note that the write should be completed before the next carry occurs.

4. Timer reading procedure

The timer reading procedure is shown in Figure 3. The timer cannot be read correctly if a carry occurs during timer reading and must be re-read. Figure a) shows a procedure which does not use an interrupt, and b) shows a procedure which uses an interrupt ($\overline{IRQ}$ pin). In general, a) is used because it is simple.

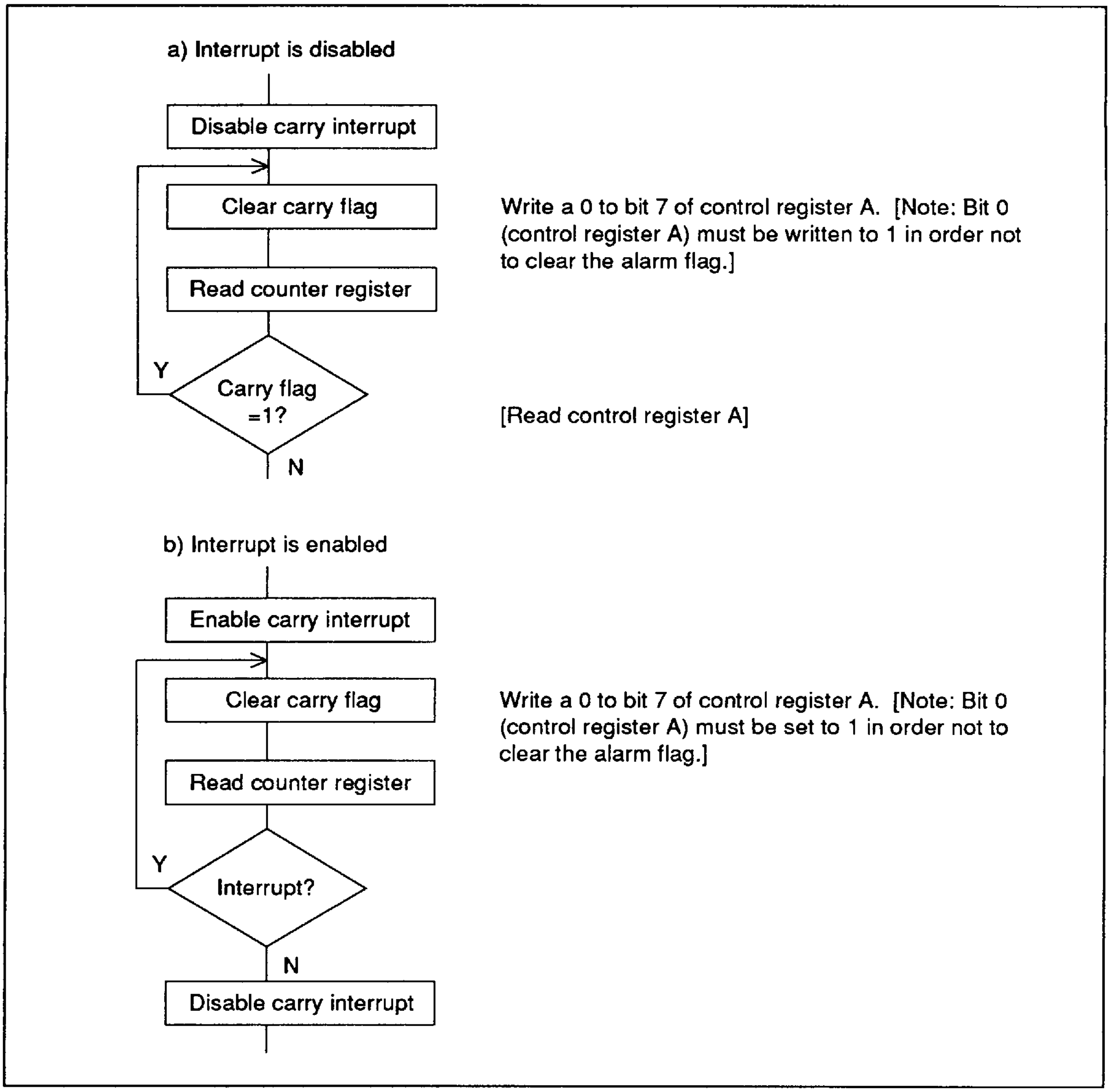


Figure 3 Timer Reading Procedure

Notes: 1. Carry of a second, minute, hour, day of week, month, and year occurs during 125 µsec on every second. Therefore, if a carry is detected during a read operation, a correct read operation can be performed after a wait of at least 125 µsec. Note that the read should be completed before the next carry occurs.

2. A carry occurs about every 8 msec and is performed during 125 µsec in the 64-Hz counter.

5. Alarm function

The alarm setting procedure is shown below.

An alarm is generated by setting the 64-Hz, second, minute, day of week, or date alarm register, or a combination of these registers.

To activate the alarm registers, set bit 7 (ENB) to 1, and to deactivate the registers, set bit 7 to 0.

If the timer and alarm time match, bit 0 (AF bit) of control register A is set to 1. The alarm can be detected by reading this bit, but in general, an interrupt is used for alarm detection. For instance, if an alarm interrupt is enabled by writing a 1 to bit 3 (AIE bit) of control register A, the $\overline{IRQ}$ pin is asserted low when the alarm is activated.

Accordingly, the alarm can be detected only by checking the $\overline{IRQ}$ pin.

Note that the alarm flag is automatically set to 1, even if it is cleared to 0 when the alarm is activated.

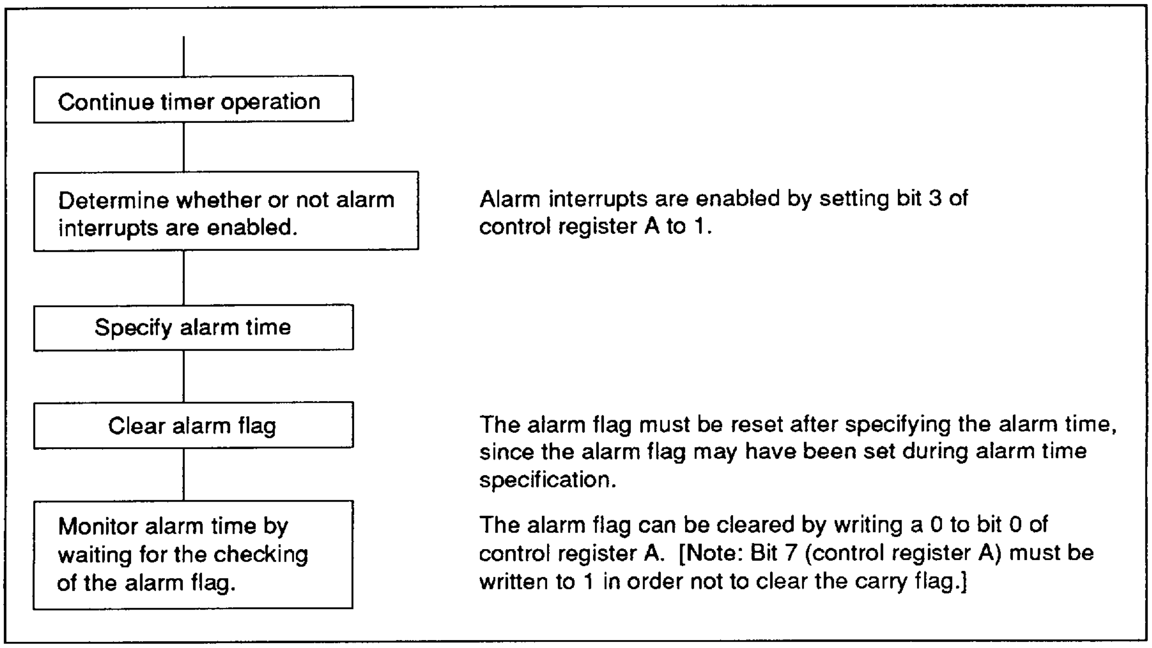


Figure 4 Alarm Function

6. Timer application

The HD64610 provides a counter START/STOP function. With this function, a timer can be used for long period measurement. Using the START/STOP function as a timer is shown below.

With this procedure, enabling the timer function requires that the year and month counters be specified since the usual calendar clock function is used. For example, if a timer is used without specifying the month counter, the 28th to 31st of the previous month cannot be identified.

The relation between the H·START/STOP pin and S·START/STOP bit is describe below.

The figure below shows the circuit diagram of the START/STOP operation.

The STOP signal is generated when H·START/STOP pin is low and the S·START/STOP bit is cleared. The STOP signal is latched by an 8-kHz clock to stop counting. To start counting, assert the H·START/STOP pin high or set the S·START/STOP bit to 1.

Stop timer	H·START/STOP is low. S·START/STOP is 0.
Reset	Write bit 1 (reset) of control register B to 1.
Set second, minute, hour, date, month, and year	Initial value of timer
Start timer	H·START/STOP is high or S·START/STOP is 1.

Figure 5 Timer Application

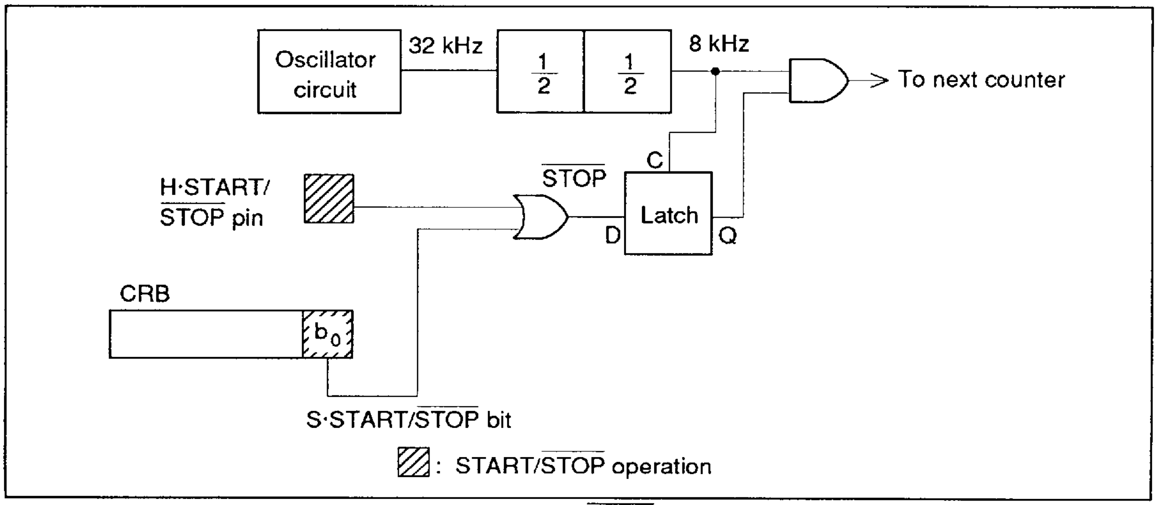


Figure 6 START/STOP Operation

Crystal Oscillator Circuit

The crystal oscillator circuit is shown in figure 7. Appropriate components should be selected according to the user application. Typical crystal oscillator circuit constants are shown below.

Table 2 Crystal Oscillator Circuit Constant (Recommended value)

f_{osc}	C_{in}	C_{out}	CI Note
32.768 kHz	10 to 20 pF	10 to 20 pF	35 kΩ (max)

Note: CI = Crystal impedance value
Drive level is 1 μW max

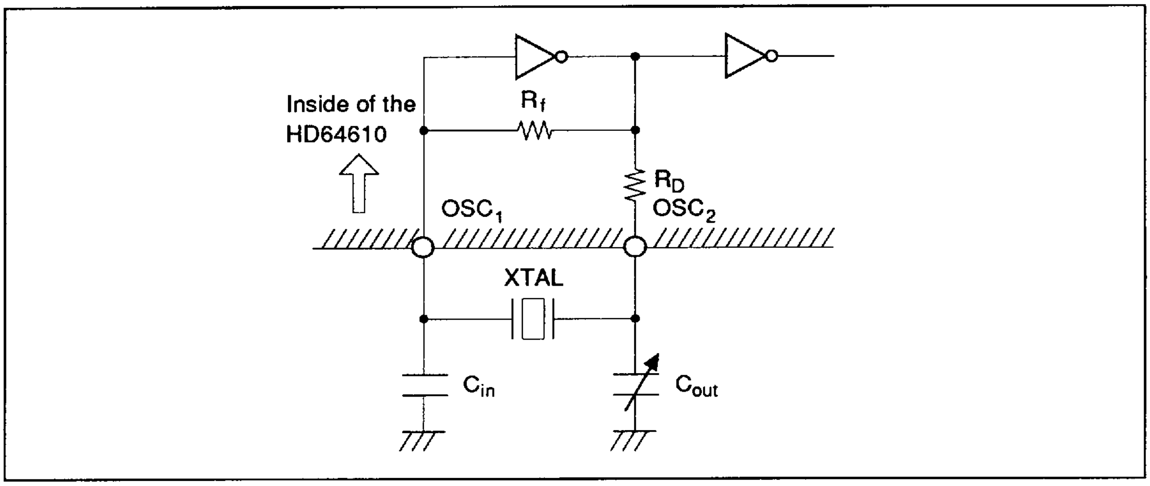
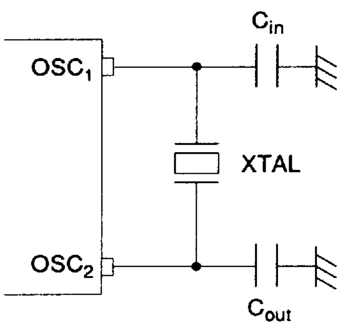


Figure 7 Crystal Oscillator Circuit Example

Notes:

1. Variable capacitor for frequency adjustment shall be connected to either C_{in} or C_{out} according to oscillation adjustment range or stabilizing degree.
2. Internal resistance: R_f (typ) = 10 MΩ, RD (typ) = 400 kΩ
3. C_{in} and C_{out} include floating capacitance in wiring. Accordingly, careful consideration must be taken when using ground patterns around C_{in} and C_{out}.
4. An oscillation start time of crystal oscillator is affected by the circuit constant, a stray capacitance, or the crystal resonator. Then, a detail investigation with the crystal vender is recommended.

(Example)



XTAL: 32.768 kwt
MU-206S (NDK)

C_{in} = 15 pF

C_{out} = 20 pF

When a crystal resonator is connected between the OSC_1 and OSC_2 pins to generate a system clock, the system clock may not be generated correctly depending on actual a crystal resonator installation conditions. Accordingly, board design must observe the following. In addition, oscillator circuit stabilization on the board must be checked.

1. To prevent induced noise on the crystal resonator and load capacitances, C_{in} and C_{out} must be connected as close to the LSI as possible. (Induced noise may prevent correct oscillation.)
2. The crystal resonator, OSC_1 and OSC_2 must be separated from power lines other than GND and signal lines as much as possible as shown in figure 8.
3. Signal lines and power lines must not run parallel to or cross the crystal oscillator circuit. An isolation resistance between OSC_1 or OSC_2 and adjacent signal lines must be 10 MΩ or more.
4. On a 32 kHz clock generator, more noise may be induced than other high frequency (ex. 4 MHz) due to high circuit impedance. Accordingly, noise occurrence and oscillation stabilization must be carefully checked.
5. On a laminated printed circuit, the crystal oscillator circuit may be shielded by a GND pattern to stabilize oscillation. In this case, careful consideration must be taken for large floating capacitance in oscillator circuit signal lines.
6. An example of board design is shown in figure 9.

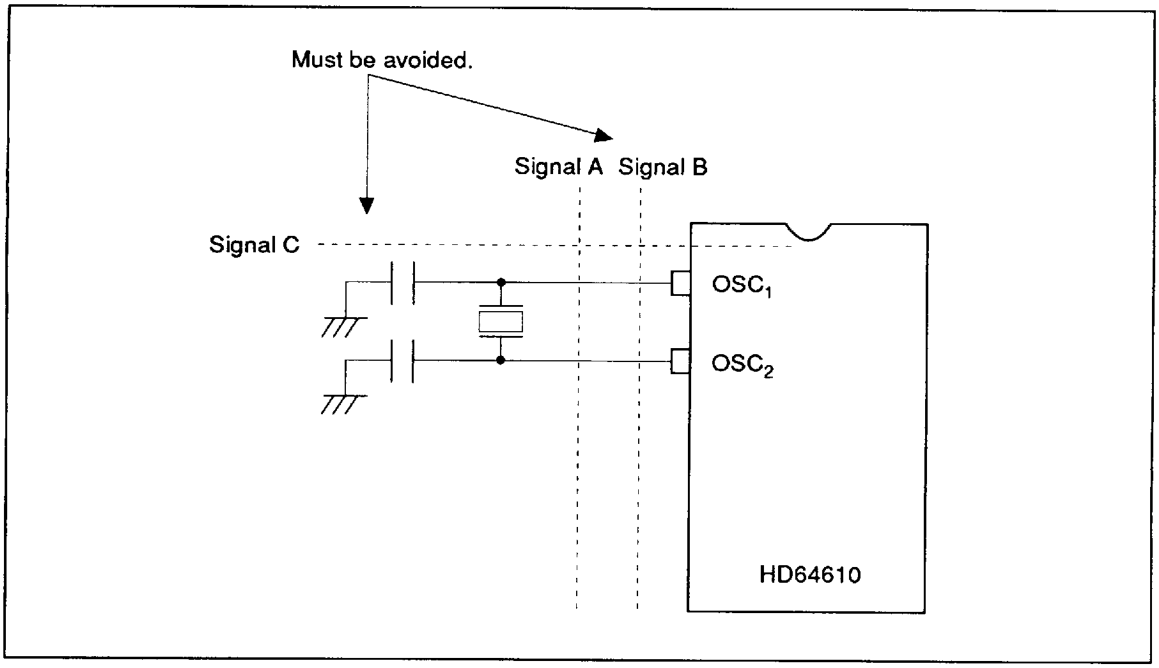


Figure 8 Signal Layout to be Avoided

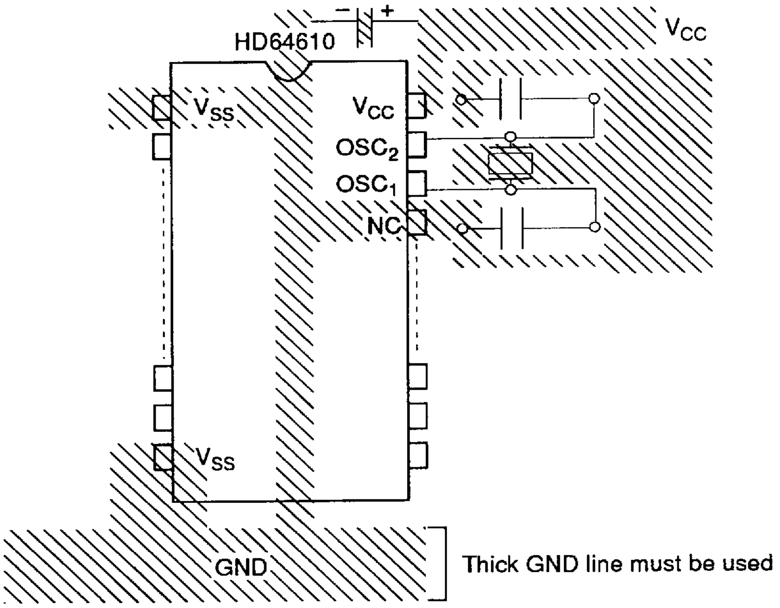


Figure 9 Board Design Example

HD64610 Operation Notes

Reinforcement of Power Lines

The HD64610 is a high-speed CMOS. Accordingly, a large peak current flows into the HD64610 at signal transition. This peak current must be carefully processed to prevent power voltage dropping and ground voltage increasing. Normally, this peak current is processed by connecting bypass capacitor to the HD64610. Bypass capacitor connection notes are shown below.

Notes:

1. A high frequency titanium, ceramic, or tantalum capacitor must be used as a bypass capacitor.
2. The bypass capacitor must be connected as close to the HD64610 V_{CC} power supply pin as possible. This can significantly reduce inductance elements from a V_{CC} pin to ground pin through the bypass capacitor.
3. Power line diameter on the printed circuit board must be as large as possible.

Electrical Characteristics

Maximum Ratings

Parameter	Symbol	Rating	Unit
Power supply voltage [1]	V_{CC}	–0.5 to +7.0	V
Input voltage [1]	V_{in}	–0.5 [2] to V_{CC} + 0.3	V
Allowable output current	$\|I_O\|$	5	mA
Total allowable output current	$\|\Sigma I_O\|$	50	mA
Operating ambient temperature	T_{opr}	Normal –20 to +75 WTR [4] –40 to +85	°C
Storage temperature	T_{stg}	–55 to +150	°C

Notes: 1. This value is in reference to V_{SS} = 0 V.
2. –3.0 V for 50 ns pulse width.
3. Stress greater than the above absolute maximum ratings may cause permanent damage to the HD64610. In addition, the following conditions must be observed to guarantee correct operation: $V_{SS} \leq V_{in}, V_{out} \leq V_{CC}$.
4. WTR: Wide temperature range version

DC Characteristics (V_{SS} = 0 V, T_a = –20 to +75 °C (Normal) unless otherwise specified. T_a = –40 to + 85°C (WTR) unless otherwise specified.)

		V_{CC} = 5 V ± 10%		V_{CC} = 2 V		Test	
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Condition**	**Unit**
Operation frequency	f_{osc}	32.768	32.768	32.768	32.768		kHz
Input high voltage	V_{iH}	2.2	V_{CC}	V_{CC} – 0.2	V_{CC}		V
Input low voltage	V_{iL}	–0.3	0.8	–0.3	0.2		V
Input leakage current	I_{iN}	—	±2	—	±2		µA
Three-state leakage current	I_{TSL}	—	±10	—	±10		µA
Output leakage current	I_{LOH}	—	±10	—	±10		µA
Output high voltage (All outputs other than 1 Hz, $\overline{IRQ}$, and OSC_2)	V_{OH}	2.4	—	—	—	I_{OH} = –1 mA	V
Output low voltage	V_{OL}	—	0.4	—	—	I_{OL} = 2.1 mA	V
Power consumption during bus accessing	I_{CC}	—	2.0	—	—	No-load, minimum cycle time	mA
Input capacity	C_{in}	—	12.5	—	—	V_{in} = 0 V, T_a = 25°C, f = 1.0 MHz	pF
Output capacity	C_{out}	—	12.5	—	—	V_{in} = 0 V, T_a = 25°C, f = 1.0 MHz	pF

**AC Characteristics (V_{CC} = 5 V ±10%, T_a = –20 to +75°C (Normal) unless otherwise specified.
T_a = –40 to + 85°C (WTR) unless otherwise specified.)**

Bus timing: Testing conditions for bus timing characteristics (Read cycle and write cycle) are shown below.

1. Input pulse level: 0.8 V to 2.4 V
2. Input rise and fall time: 5 ns
3. Input and output reference level: 1.5 V
4. Output load: 1 TTL gate and C_L (100 pF) (including scope and jig capacitance)

Read Cycle Timing

Parameter	Symbol	Min	Max	Unit
Read cycle time	t_{RC}	85	—	ns
Address access time	t_{AA}	—	85	ns
Chip select access time	t_{ACS}	—	85	ns
Output enable to output valid	t_{OE}	—	45	ns
Output hold from address change	t_{OH}	10	—	ns
Chip selection to output in low Z	t_{CLZ}	10	—	ns
Output enable to output in low Z	t_{OLZ}	5	—	ns
Chip deselection to output in high Z	t_{CHZ}	0	35	ns
Output disable to output in high Z	t_{OHZ}	0	35	ns

Note: Bus cannot be accessed during battery backup mode.

Write Cycle Timing

Parameter	Symbol	Min	Max	Unit
Write cycle time	t_{WC}	85	—	ns
Chip selection to end of write	t_{CW}	75	—	ns
Address valid to end of write	t_{AW}	75	—	ns
Address setup time	t_{AS}	0	—	ns
Write pulse width	t_{WP}	60	—	ns
Write recovery time	t_{WR}	10	—	ns
Write to output in high Z	t_{WHZ}	0	35	ns
Data to write time overlap	t_{DW}	40	—	ns
Data hold from write time	t_{DH}	0	—	ns
Output disable to output in high Z	t_{OHZ}	0	35	ns
Output active from end of write	t_{OW}	5	—	ns

Note: Bus cannot be accessed during battery backup mode.

Oscillator Characteristics and Control Signal Timings

Parameter	Symbol	Min	Typ	Max	Unit
Crystal oscillator startup time (32 kHz)	t_{OSC}	—	—	3.0	s
$\overline{IRQ}$ release time	t_{IR}	—	—	2.0	µs
H·START/$\overline{STOP}$ control delay time	t_{HSD}	—	—	125	µs

Parameter	Symbol	Min	Typ	Max	Unit
Reset delay time	t_{RD}	—	—	125	µs
Reset time	t_{RST}	—	122	125	µs
ADJ delay time	t_{AD}	—	—	125	µs
ADJ time	t_{ADJ}	—	122	185	µs

Note: Reset and ADJ must not be set during their operation cycles. They must be set after their operation cycles have been completed. Reset and ADJ can be set simultaneously.

Timing Charts

Bus Timings

Read Cycle Timing 1 (Note 1)

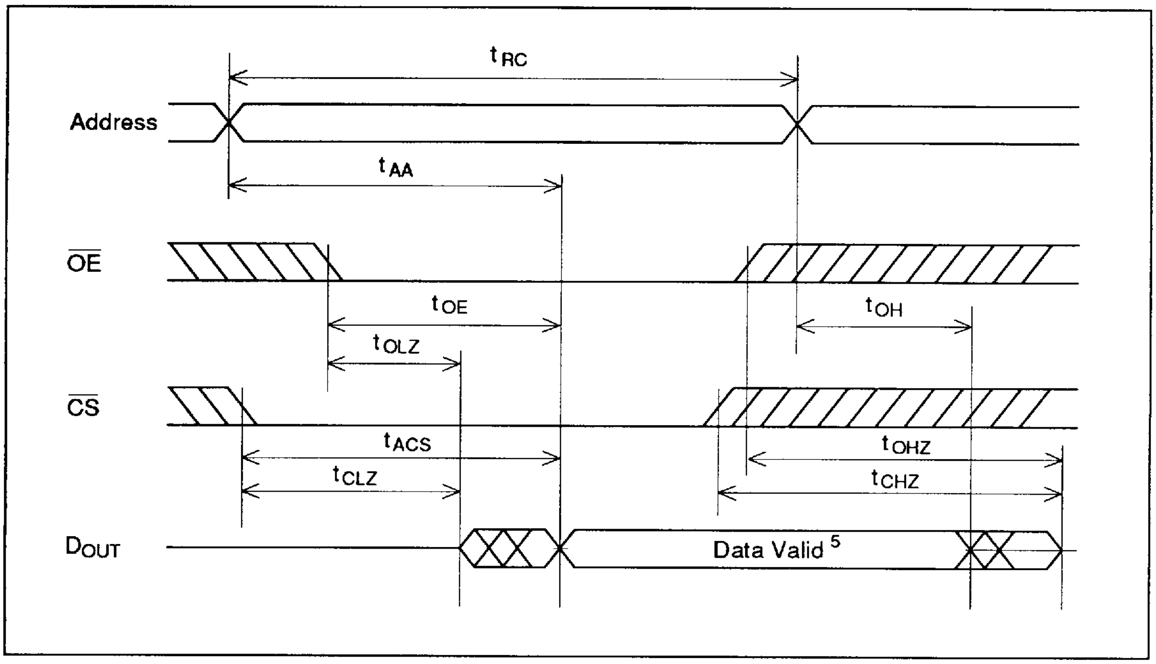


Figure 10 Read Cycle Timing 1

Read Cycle Timing 2 (Notes 1, 2, and 4)

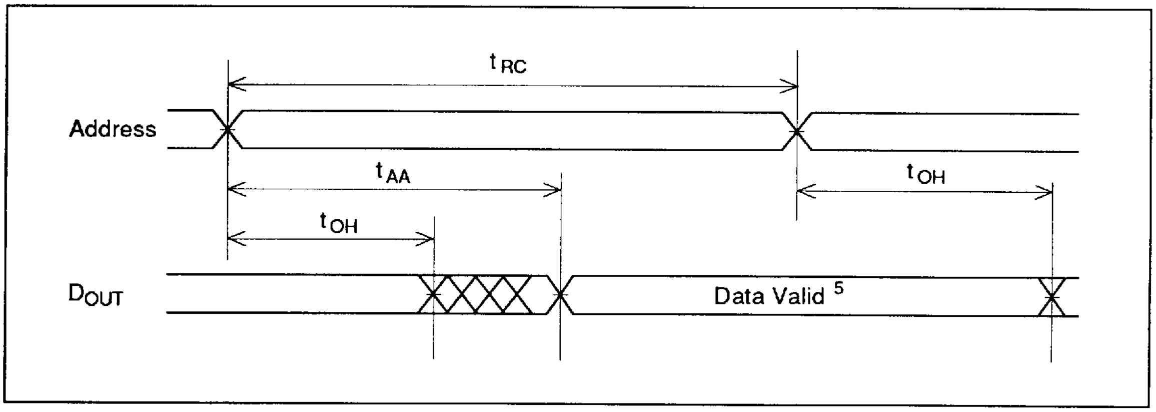


Figure 11 Read Cycle Timing 2

Read Cycle Timing 3 (Notes 1, 3, and 4)

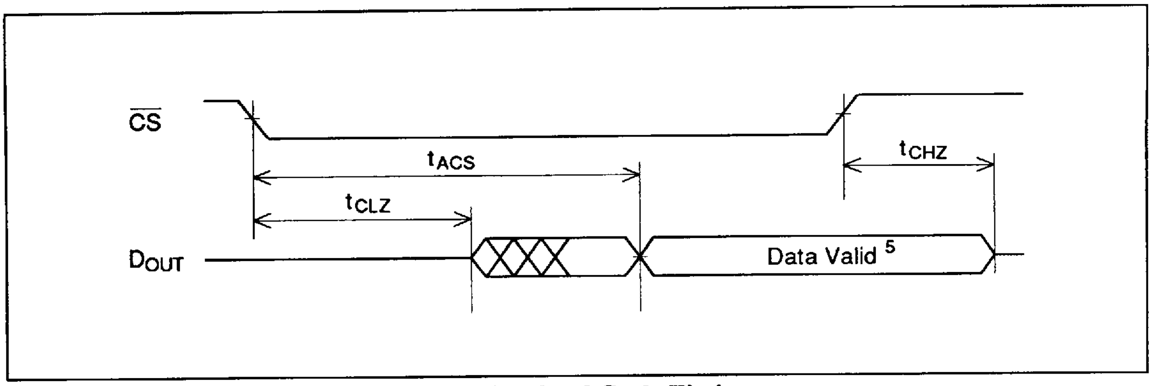


Figure 12 Read Cycle Timing

Notes: 1. $\overline{WE}$ must be negated high for read cycle.

2. A device is continuously selected with $\overline{CS} = V_{IL}$.

3. An address must be defined prior to or coincident with $\overline{CS}$ transition low.

4. $\overline{OE} = V_{IL}$

5. D_{OUT} changes if the contents of register change during read cycle.

Write Cycle Timing 1 ($\overline{OE}$ clock)

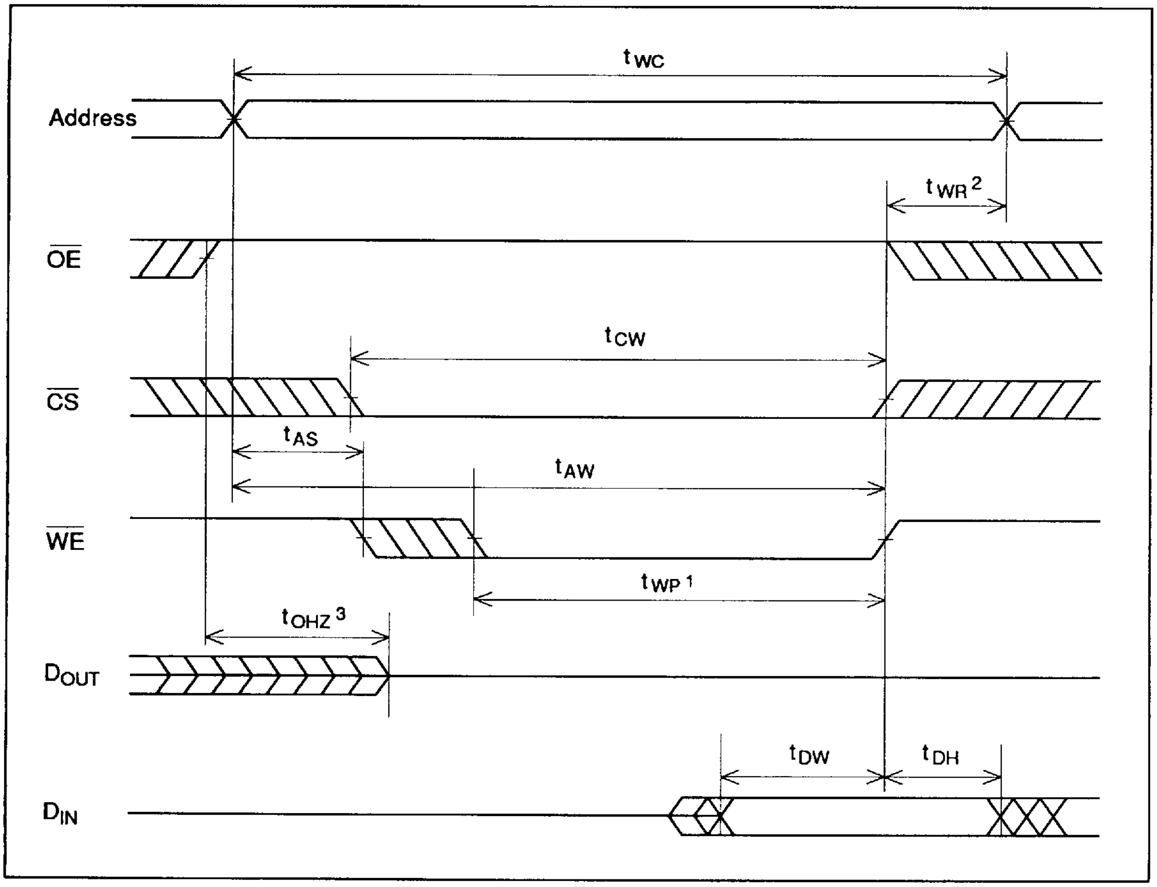


Figure 13 Write Cycle Timing 1

Notes: 1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.

2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

3. During this period, I/O pins are in the output state. The input signals out of phase must not be applied.

Write Cycle Timing 2 ($\overline{OE}$ [5] clock is fixed at low)

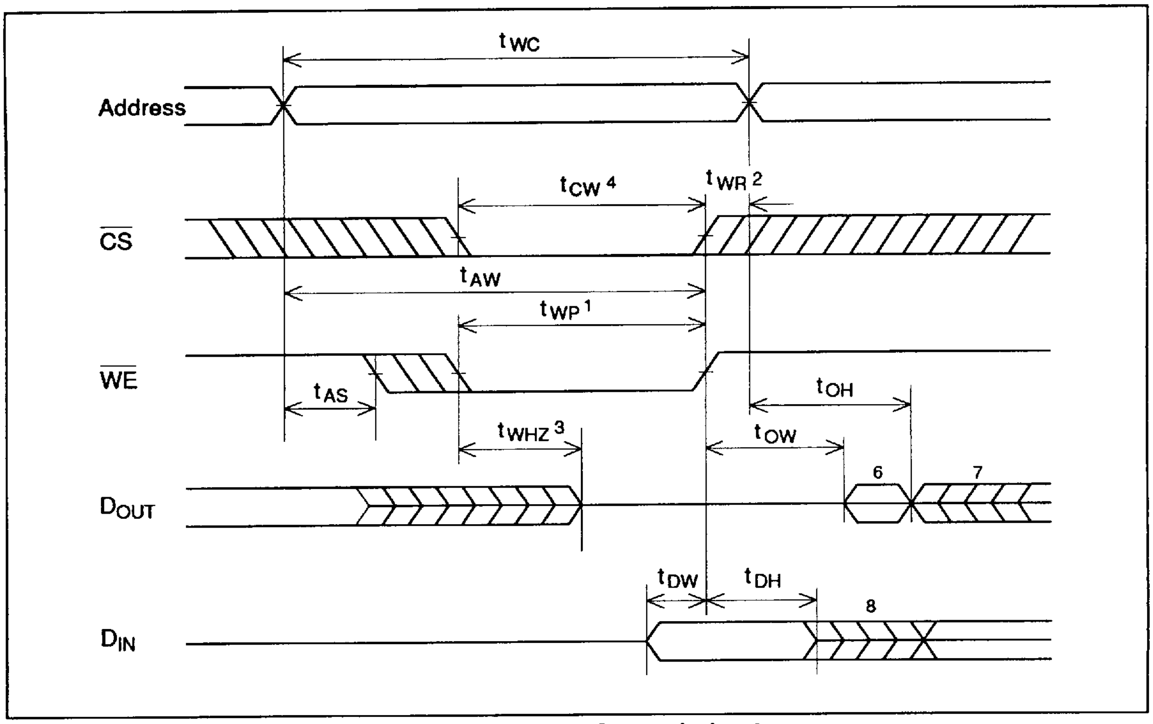


Figure 14 Write Cycle Timing 2

Notes: 1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.

2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

3. During this period, I/O pins are in the output state. The input signals out of phase must not be applied.

4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remains in a high impedance state.

5. $\overline{OE}$ is continuously low ($\overline{OE}$ = V_{IL})

6. D_{OUT} is in the same phase of written data of this write cycle.

7. D_{OUT} is the read data of next address.

8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. The input signals out of phase must not be applied to I/O pins.

Oscillator Timing

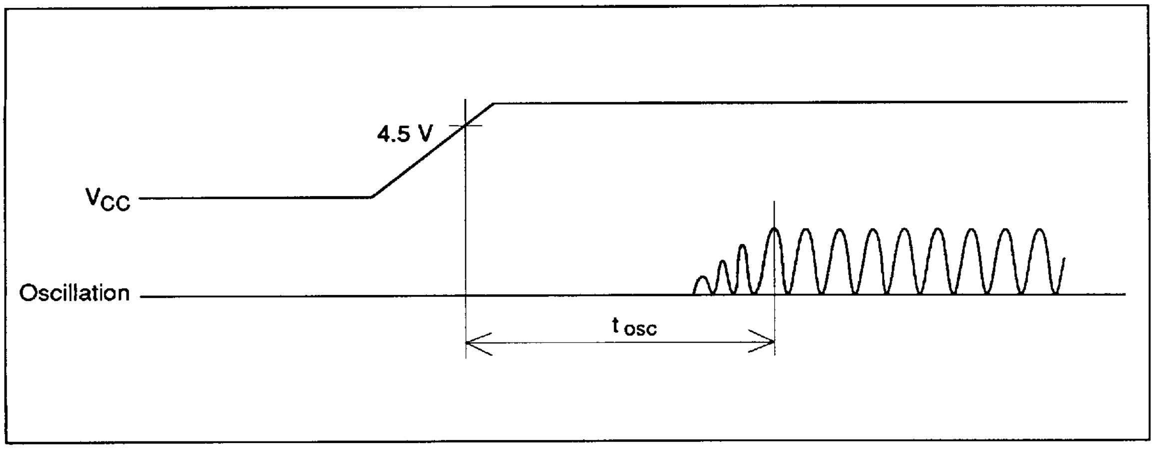


Figure 15 Oscillator Timing

Note: Crystal oscillator startup time (t_{OSC}) is defined for T_a = –20°C to ±75°C and V_{CC} = 5 V + 10%. Crystal oscillator startup time for $V_{CC} \leq$ 4.5 V is undefined. In addition, if the crystal oscillator is started up under the conditions which do not satisfy T_a ($T_a \neq$ –20°C to 75°C), an overtone oscillation error may occur in the oscillator.

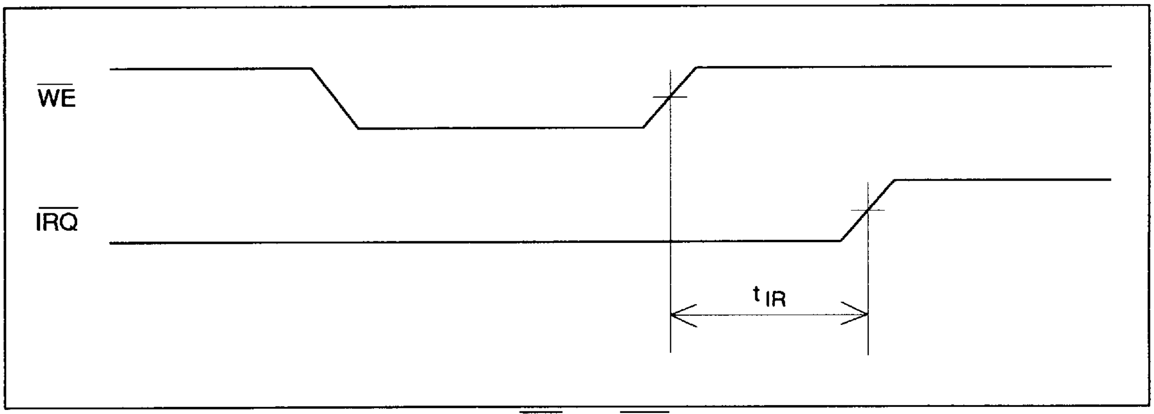


Figure 16 $\overline{WE}$ and $\overline{IRQ}$ Timing

Control Signal Timing

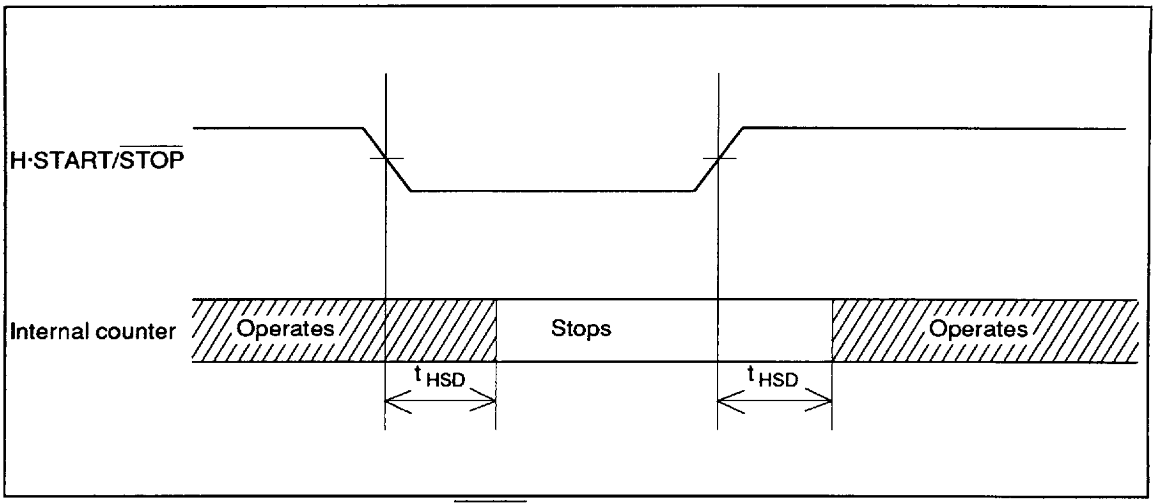


Figure 17 H·START/STOP Signal and Internal Counter Timing

Reset and ADJ Timings

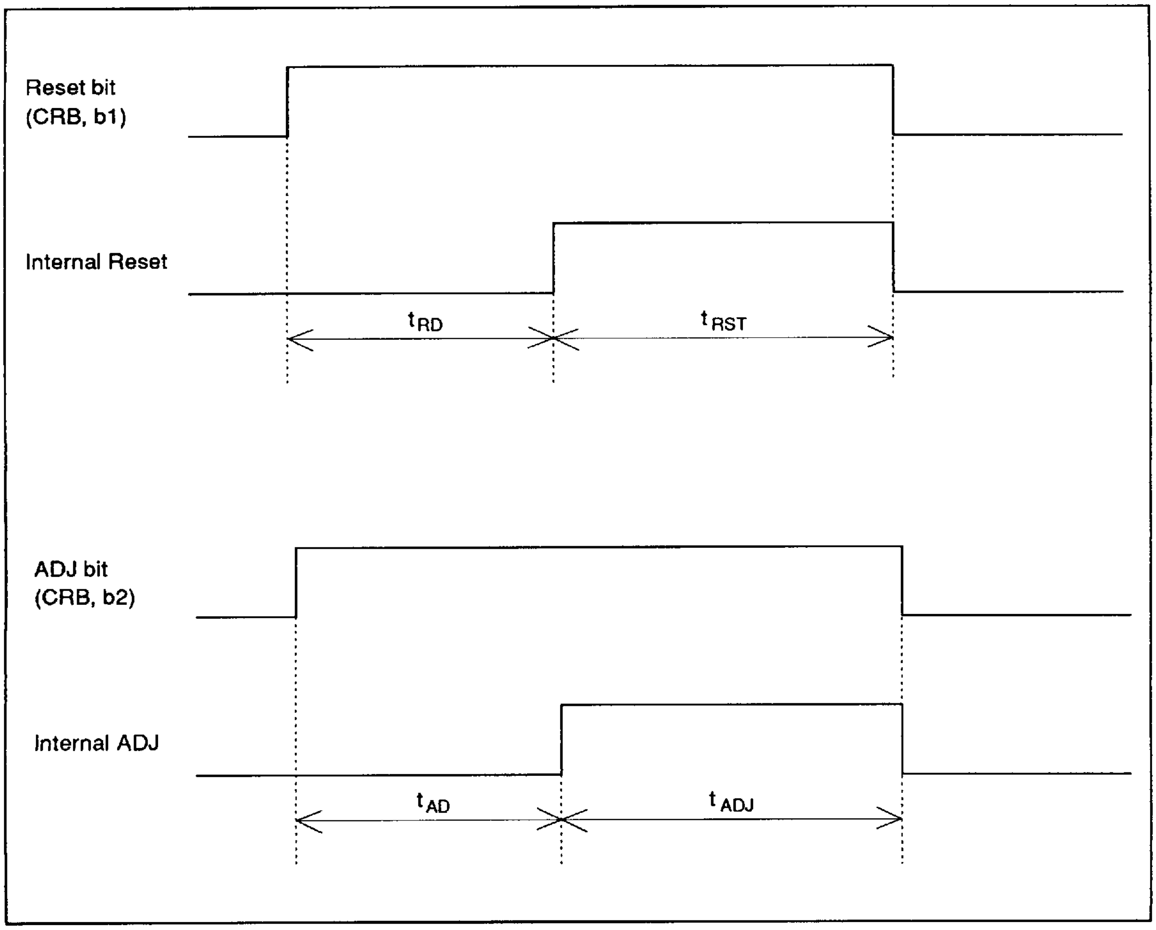


Figure 18 Reset and ADJ Timing

Battery Backup Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Data retention supply voltage	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2$ V	2.0	—	4.5	V
Supply current	I_{CCDR}	V_{CC} = 2.0 V, $\overline{CS} \geq 1.8$ V H·START/$\overline{STOP}$ ≥ 1.8 V, $\overline{IRQ}$, 1 Hz = open	—	0.8	2.0	µA
Chip select data retention time	t_{CDR}	Refer to the following figure.	0	—	—	ns
Operation recovery time	t_R	Refer to the following figure.	t_{RC}	—	—	ns

Note: t_{RC} = read cycle time

Battery Backup Timing

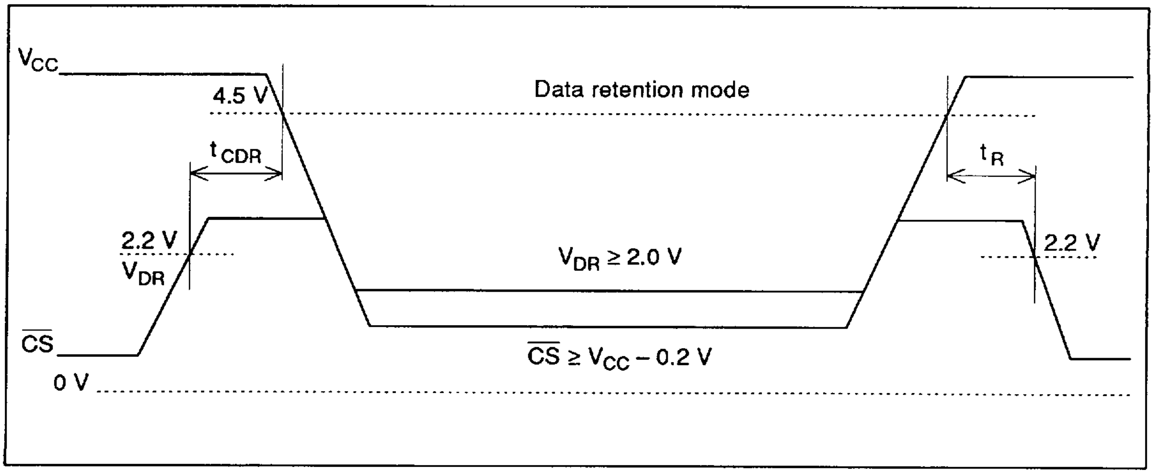


Figure 19 Battery Backup Timing

Note: $\overline{CS}$ controls address buffer, dat buffer, $\overline{WE}$ buffer, and $\overline{OE}$ buffer. During battery backup mode, address, data, $\overline{WE}$, and $\overline{OE}$ which can be placed in high impedance state.

Test Loads

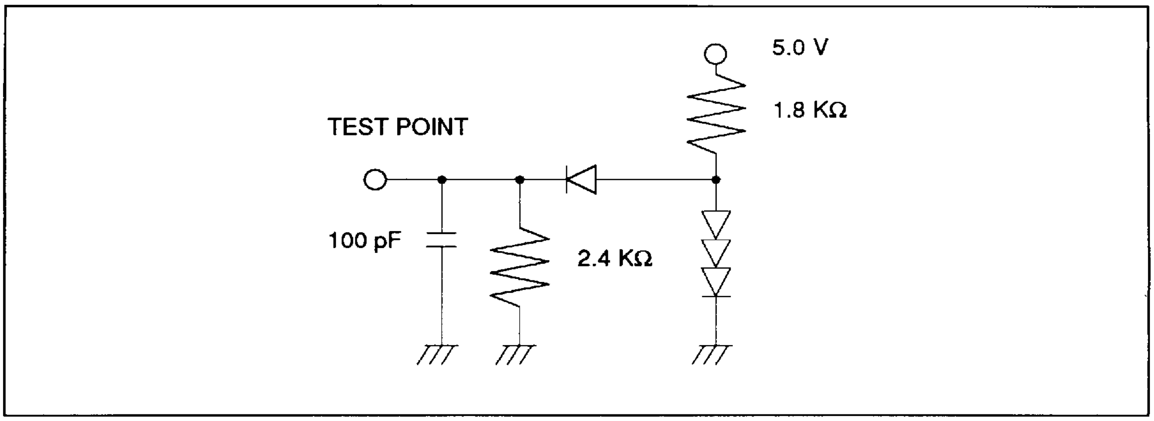


Figure 20 Load A (I/O_1 to I/O_8)

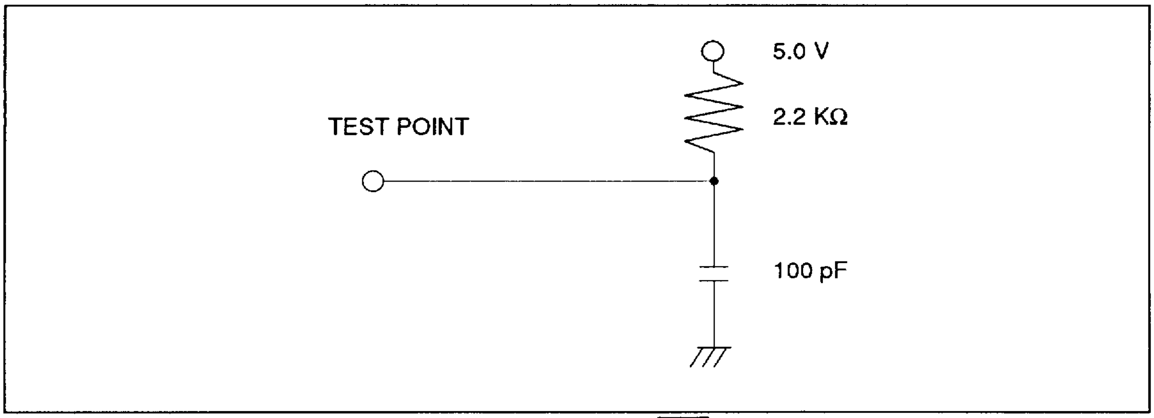


Figure 21 Load B ($\overline{IRQ}$)

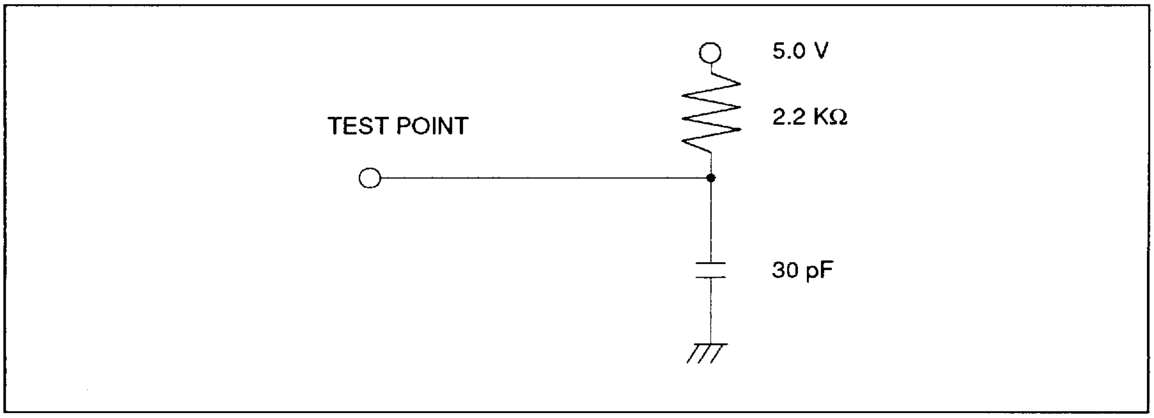


Figure 22 Load C (1 Hz)

References

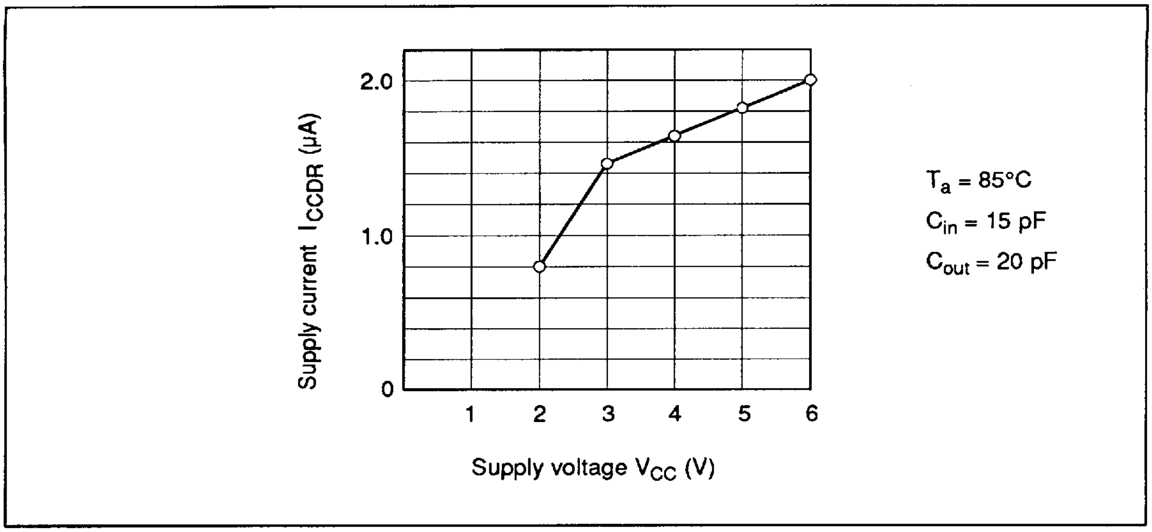


Figure 23 Supply Current vs. Supply Voltage

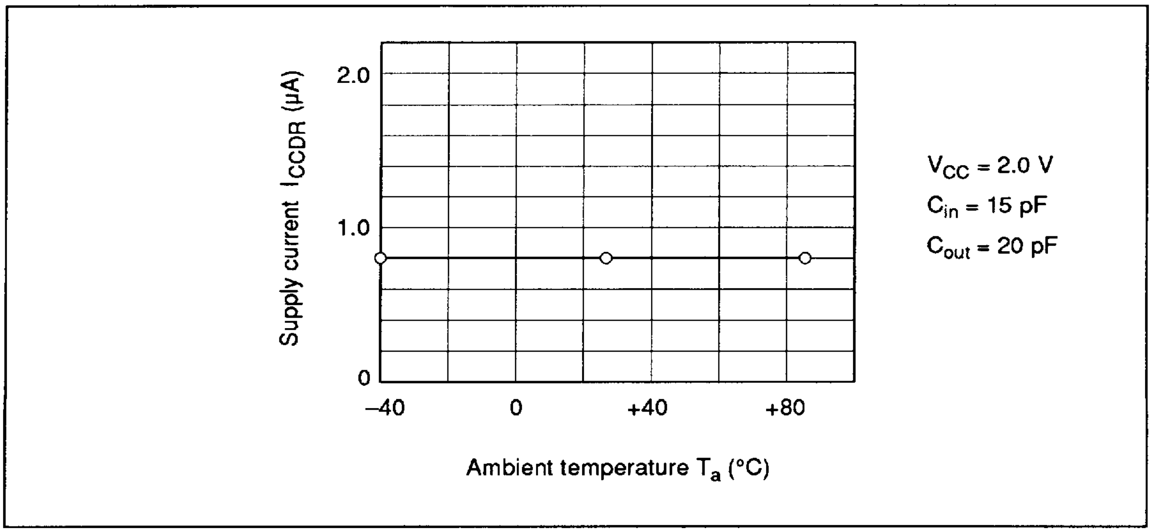


Figure 24 Supply Current vs. Ambient Temperature

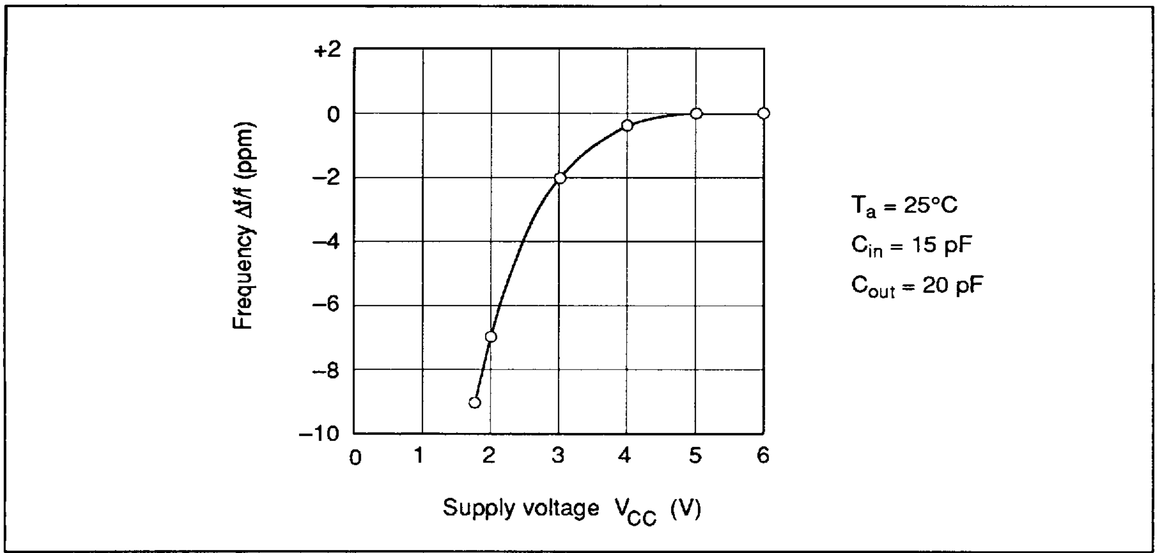


Figure 25 Frequency vs. Supply Voltage

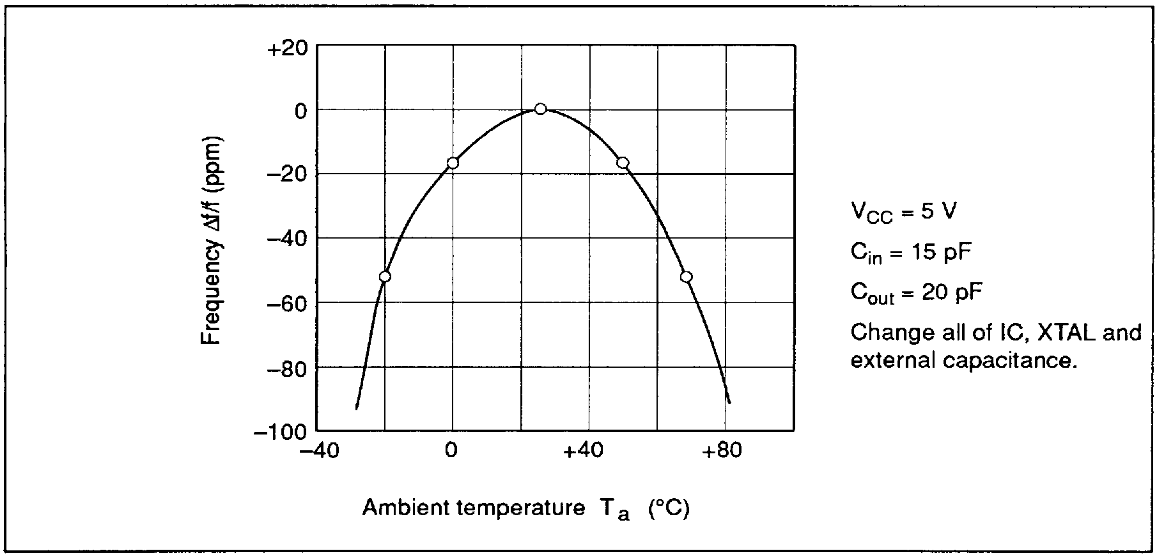


Figure 26 Frequency vs. Ambient Temperature

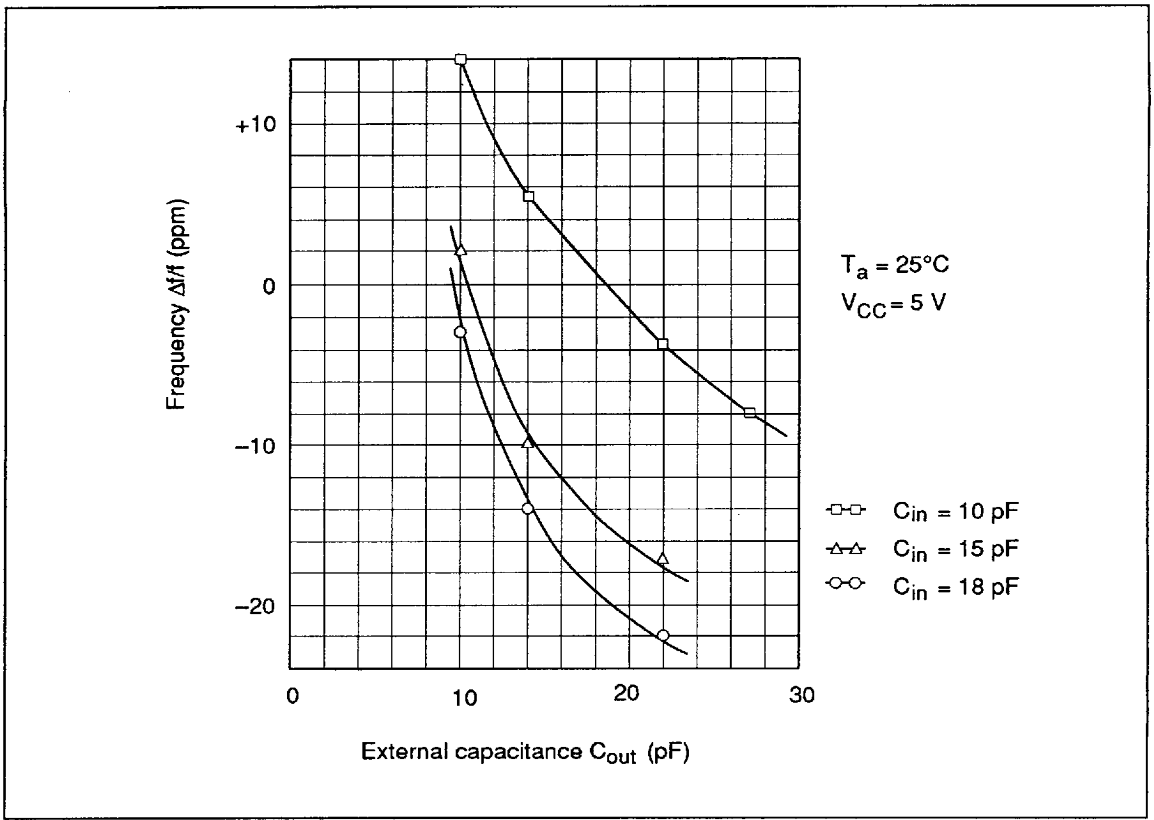


Figure 27 Frequency vs. External Capacitance