

## 14A, 50V, Avalanche Rated N-Channel Enhancement-Mode Power MOSFETs

December 1995

### Features

- 14A, 50V
- $r_{DS(ON)} = 0.100\Omega$
- *Temperature Compensating* PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- +175°C Operating Temperature

### Description

The RFD14N05, RFD14N05SM, and RFP14N05 N-channel power MOSFETs are manufactured using the MegaFET process. This process which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

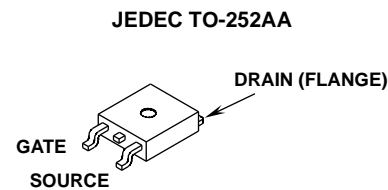
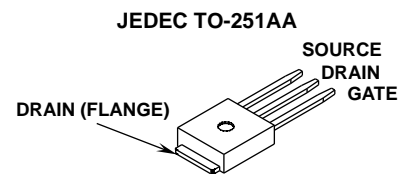
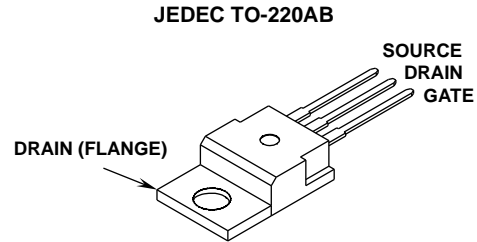
#### PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RFD14N05	TO-251AA	F14N05
RFD14N05SM	TO-252AA	F14N05
RFP14N05	TO-220AB	RFP14N05

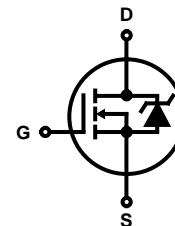
NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-252AA variant in the tape and reel, i.e., RFD14N05SM9A.

Formerly developmental type TA09770.

### Packaging



### Symbol



### Absolute Maximum Ratings $T_C = +25^\circ\text{C}$

	RFD14N05, RFD14N05SM, RFP14N05	UNITS
Drain-Source Voltage	50	V
Drain-Gate Voltage	50	V
Gate-Source Voltage	$\pm 20$	V
Drain Current		
RMS Continuous	14	A
Pulsed Drain Current	Refer to Peak Current Curve	
Pulsed Avalanche Rating	Refer to UIS Curve	
Power Dissipation		
$T_C = +25^\circ\text{C}$	48	W
Derate above +25°C	0.32	W/°C
Operating and Storage Temperature	-55 to +175	°C
Soldering Temperature of Leads for 10s	260	°C

## Specifications RFD14N05, RFD14N05SM, RFP14N05

### Electrical Specifications $T_C = +25^{\circ}\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
Drain-Source Breakdown Voltage	$V_{DSS}$	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$	50	-	-	V	
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$ , $I_D = 250\mu\text{A}$	2	-	4	V	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 50\text{V}$ , $V_{GS} = 0\text{V}$	$T_C = +25^{\circ}\text{C}$	-	-	1	$\mu\text{A}$
			$T_C = +150^{\circ}\text{C}$	-	-	50	$\mu\text{A}$
Gate-Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20\text{V}$	-	-	100	nA	
On Resistance	$r_{DS(ON)}$	$I_D = 14\text{A}$ , $V_{GS} = 10\text{V}$	-	-	0.100	$\Omega$	
Turn-On Time	$t_{ON}$	$V_{DD} = 25\text{V}$ , $I_D = 14\text{A}$ , $R_L = 3.57\Omega$ , $V_{GS} = 10\text{V}$ , $R_{GS} = 25\Omega$	-	-	60	ns	
Turn-On Delay Time	$t_{D(ON)}$		-	14	-	ns	
Rise Time	$t_R$		-	26	-	ns	
Turn-Off Delay Time	$t_{D(OFF)}$		-	45	-	ns	
Fall Time	$t_F$		-	17	-	ns	
Turn-Off Time	$t_{OFF}$		-	-	100	ns	
Total Gate Charge	$Q_{G(TOT)}$		$V_{GS} = 0\text{V to } 20\text{V}$	-	-	40	nC
Gate Charge at 10V	$Q_{G(10)}$		$V_{GS} = 0\text{V to } 10\text{V}$				
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 0\text{V to } 2\text{V}$					
Input Capacitance	$C_{ISS}$	$V_{DS} = 25\text{V}$ , $V_{GS} = 0\text{V}$ , $f = 1\text{MHz}$	-	570	-	pF	
Output Capacitance	$C_{OSS}$		-	185	-	pF	
Reverse Transfer Capacitance	$C_{RSS}$		-	50	-	pF	
Thermal Resistance Junction-to-Case	$R_{\theta JC}$		-	-	3.125	$^{\circ}\text{C/W}$	
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	TO-251 and TO-252	-	-	100	$^{\circ}\text{C/W}$	
		TO-220	-	-	80	$^{\circ}\text{C/W}$	

### Source-Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	$V_{SD}$	$I_{SD} = 14\text{A}$	-	-	1.5	V
Reverse Recovery Time	$t_{RR}$	$I_{SD} = 14\text{A}$ , $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	125	ns

Typical Performance Curves

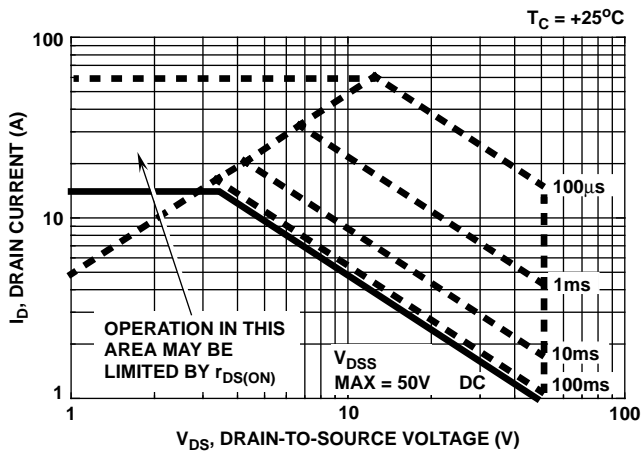


FIGURE 1. SAFE OPERATING AREA CURVE

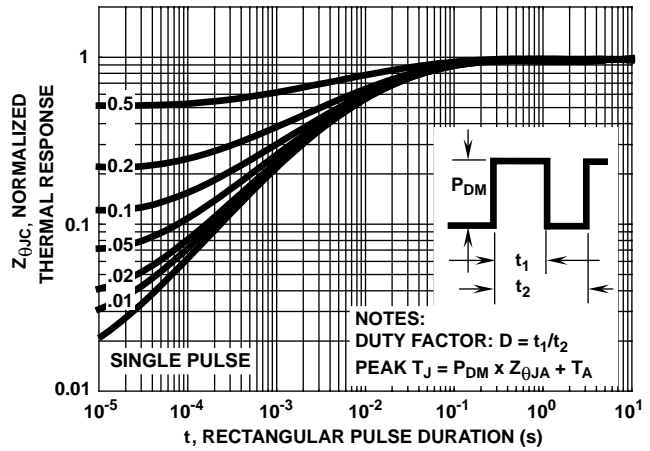


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

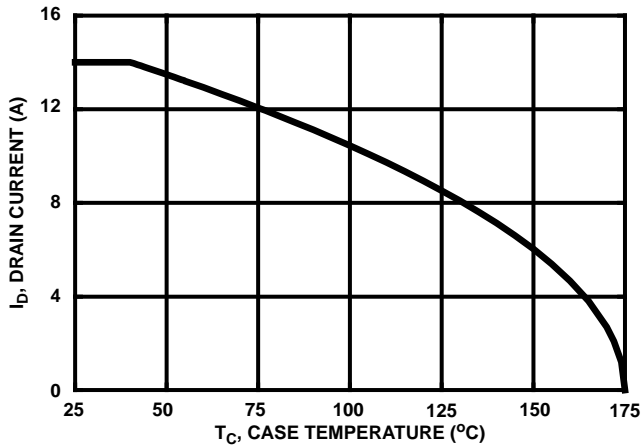


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

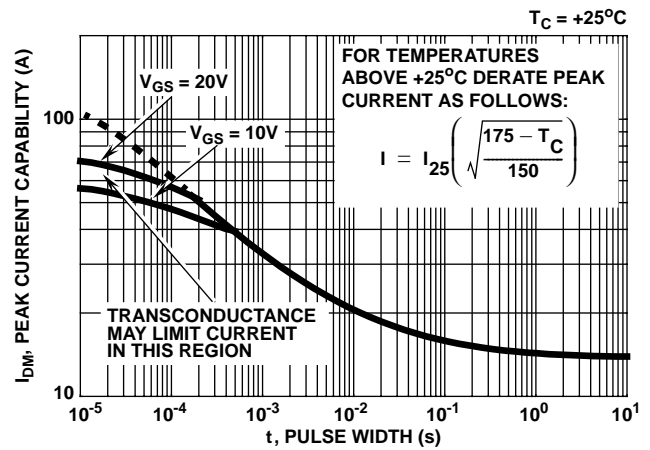


FIGURE 4. PEAK CURRENT CAPABILITY

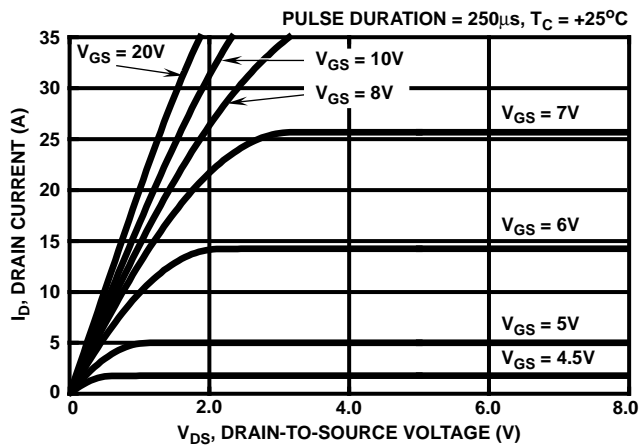


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

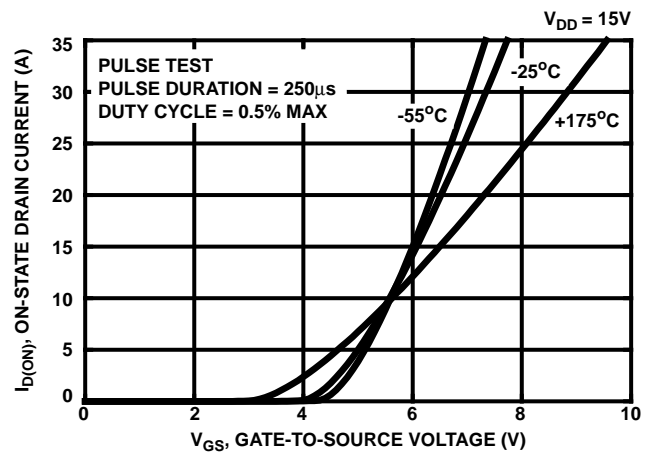


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

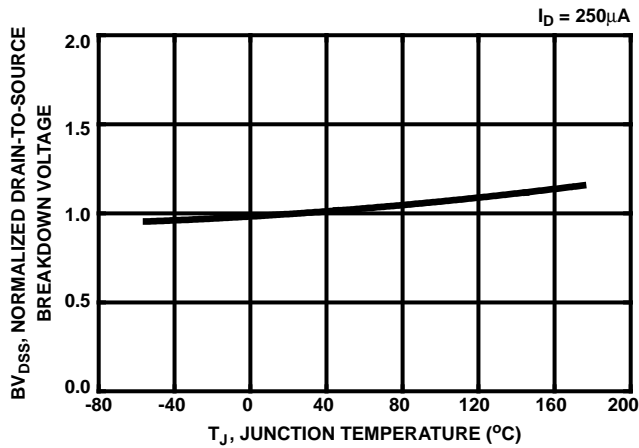


FIGURE 7. NORMALIZED DRAIN-SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

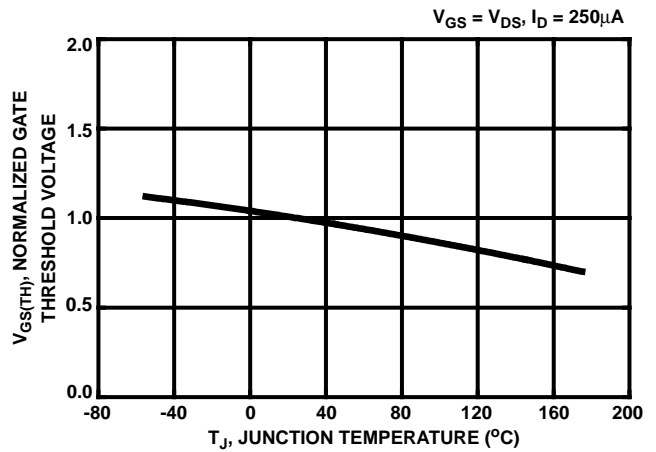


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

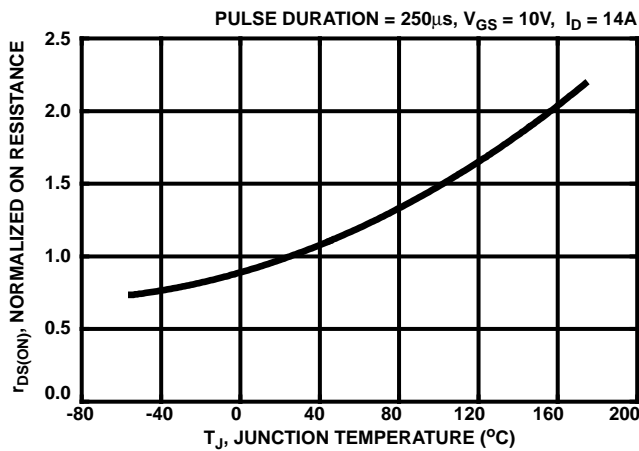


FIGURE 9. NORMALIZED  $r_{DS(ON)}$  vs JUNCTION TEMPERATURE

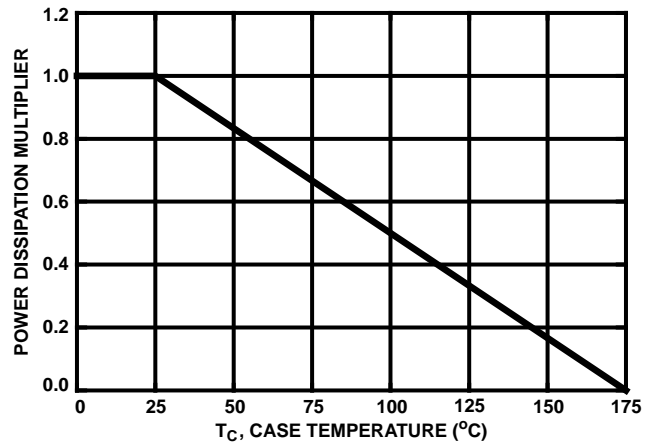


FIGURE 10. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

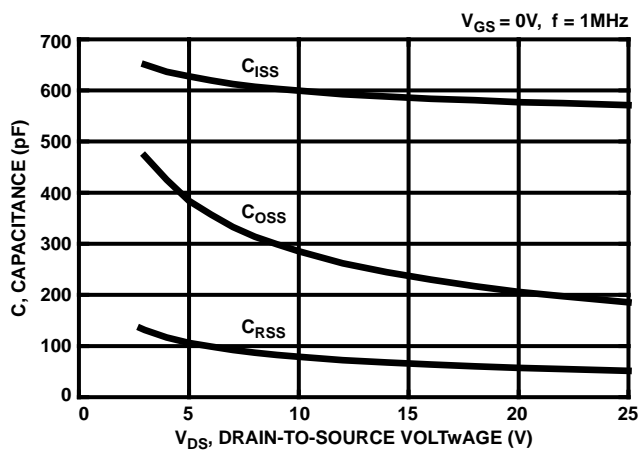


FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

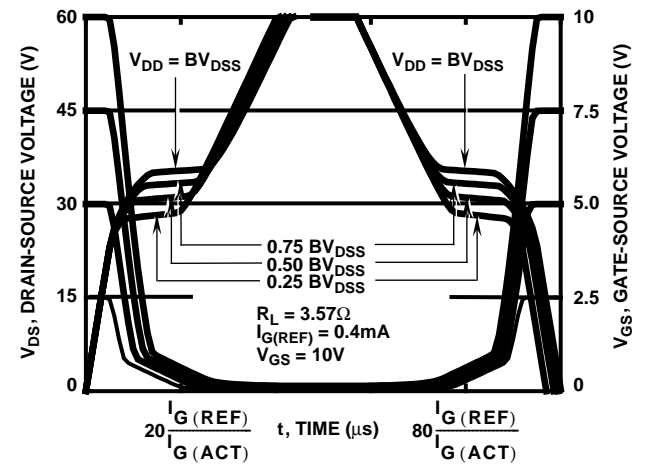


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

Typical Performance Curves (Continued)

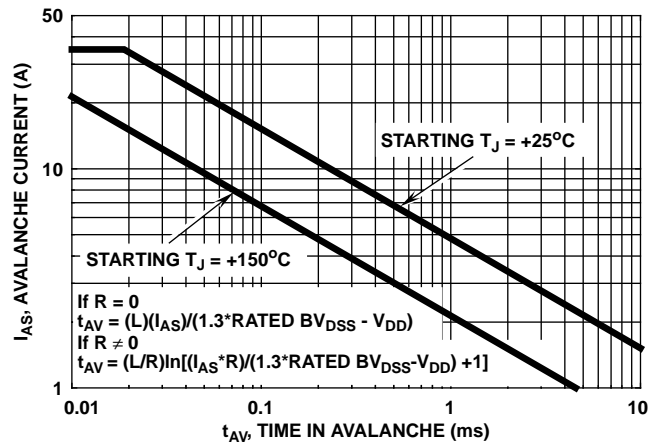


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING.  
 REFER TO HARRIS APPLICATION NOTES AN9321 AND AN9322

Test Circuits and Waveforms

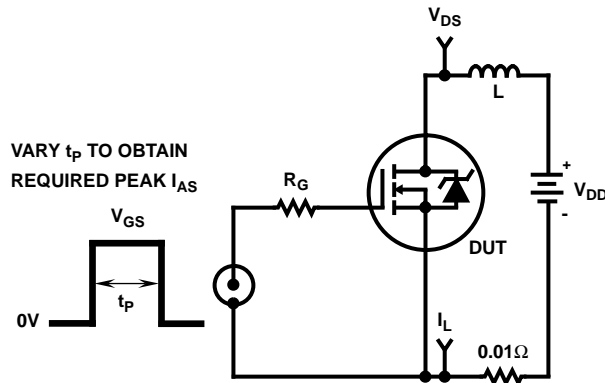


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

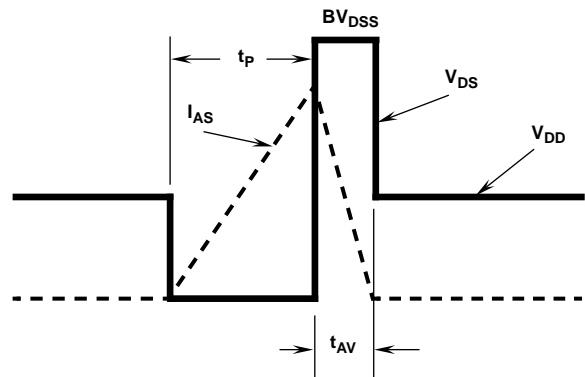


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

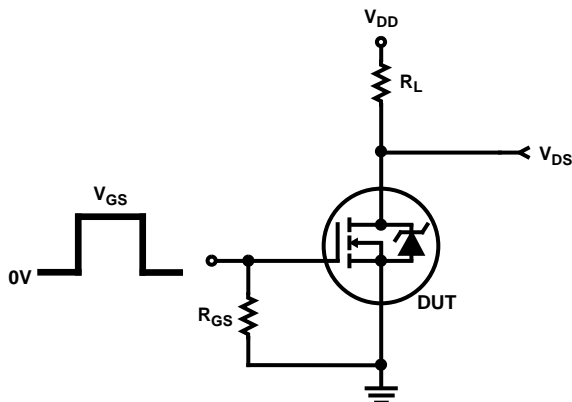


FIGURE 16. RESISTIVE SWITCHING TEST CIRCUIT

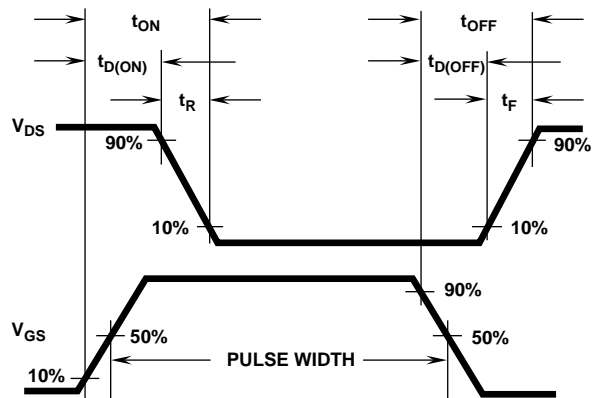


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

## RFD14N05, RFD14N05SM, RFP14N05

### Temperature Compensated PSPICE Model for the RFD14N05, RFD14N05SM, RFP14N05

.SUBCKT RFP14N05 2 1 3 ; rev 9/12/94

CA 12 8 8.84e-10  
 CB 15 14 9.34e-10  
 CIN 6 8 5.2e-10

DBODY 7 5 DBDMOD  
 DBREAK 5 11 DBKMOD  
 DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 62.87  
 EDS 14 8 5 8 1  
 EGS 13 8 6 8 1  
 ESG 6 10 6 8 1  
 EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1e-9  
 LGATE 1 9 4.34e-9  
 LSOURCE 3 7 3.79e-9

MOS1 16 6 8 8 MOSMOD M = 0.99  
 MOS2 16 21 8 8 MOSMOD M = 0.01

RBREAK 17 18 RBKMOD 1  
 RDRAIN 50 16 RDSMOD 2.2e-3  
 RGATE 9 20 5.64  
 RIN 6 8 1e9  
 RSCL1 5 51 RSCLMOD 1e-6  
 RSCL2 5 50 1e3  
 RSOURCE 8 7 RDSMOD 42.3e-3  
 RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD  
 S1B 13 12 13 8 S1BMOD  
 S2A 6 15 14 13 S2AMOD  
 S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1  
 VTO 21 6 0.82

ESCL 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))\*(PWR(V(5,51)\*1e6/50,6))}

.MODEL DBDMOD D (IS = 1.5e-13 RS = 10.9e-3 TRS1 = 2.3e-3 TRS2 = -1.75e-5 CJO = 6.84e-10 TT = 4.2e-8)  
 .MODEL DBKMOD D (RS = 4.15e-1 TRS1 = 3.73e-3 TRS2 = -3.21e-5)  
 .MODEL DPLCAPMOD D (CJO = 26.2e-11 IS = 1e-30 N = 10)  
 .MODEL MOSMOD NMOS (VTO = 3.91 KP = 12.68 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)  
 .MODEL RBKMOD RES (TC1 = 7.73e-4 TC2 = 2.12e-6)  
 .MODEL RDSMOD RES (TC1 = 5.0e-3 TC2 = 2.53e-5)  
 .MODEL RSCLMOD RES (TC1 = 2.05e-3 TC2 = 1.35e-5)  
 .MODEL RVTOMOD RES (TC1 = -4.44e-3 TC2 = -6.45e-6)  
 .MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -5.29 VOFF = -3.29)  
 .MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -3.29 VOFF = -5.29)  
 .MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.25 VOFF = 2.75)  
 .MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 2.75 VOFF = -2.25)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; written by William J. Hepp and C. Frank Wheatley.

