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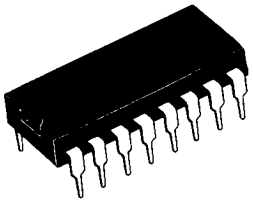
Linear Integrated Circuits

CA3242E

May 1990



16-Lead Dual-In-Line Plastic Package (E Suffix)

Quad-Gated Inverting Power Driver

For Interfacing Low-Level Logic to High Current Loads

Features:

- *Driven outputs capable of switching 600-mA load currents without spurious changes in output state*
- *Inputs compatible with TTL or 5-volt CMOS logic*
- *Suitable for resistive or inductive loads*
- *Output overload protection*
- *Power-Frame construction for good heat dissipation*

The RCA CA3242E quad-gated inverting power driver contains four gate switches for interfacing low-level logic to inductive and resistive loads such as: relays, solenoids, AC and DC motors, heaters, incandescent displays, and vacuum fluorescent displays.

Output overload protection is provided when the load current (approximately 1.2 A) causes the output V_{CE}(sat) to rise above 1.3 V. A built-in time delay, nominally 25 μs, is provided during output turn-on as output drops from V_{DD} to V_{SAT}. That output will be shut down by its protection network without affecting the other outputs. The corresponding Input or Enable must be toggled to reset the output protection circuit.

Steering diodes in the outputs in conjunction with external zener diodes protect the IC against voltage transients due to switching inductive loads.

To allow for maximum heat transfer from the chip, the two center leads are directly connected to the die mounting pad. In free air, junction-to-air thermal resistance ($R_{\theta JA}$) is 50° C/W* (typical). This coefficient can be lowered to 40° C/W (typical) by suitable design of the PC board to which the CA3242E is soldered.

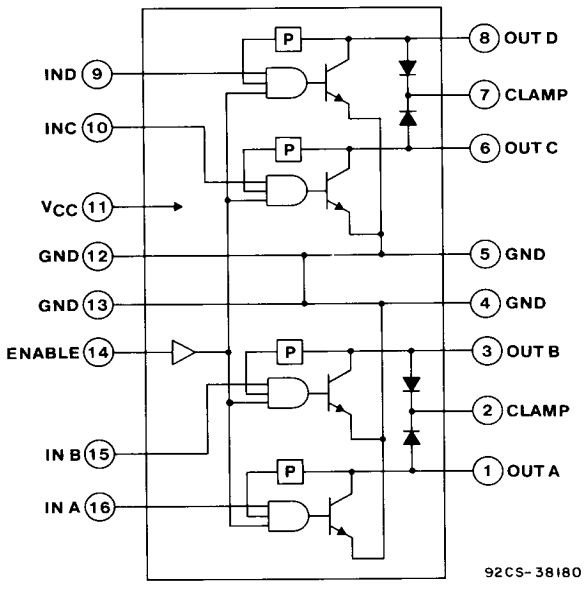


Fig. 1 - Block diagram for the CA3242E.

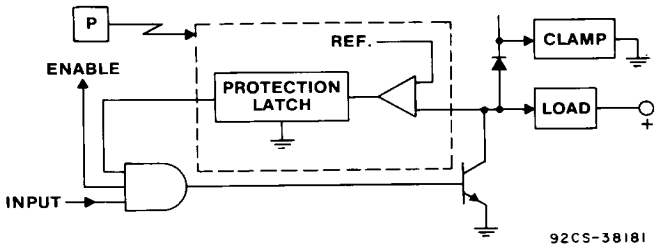


Fig. 2 - Logic diagram for each output.

TRUTH TABLE

ENABLE	IN	OUT
H	H	L
H	L	H
L	X	H

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25°C$*

LOGIC SUPPLY VOLTAGE (V_{CC}) ..... 7 V
LOGIC INPUT VOLTAGE (V_{IN}) ..... 15 V
OUTPUT VOLTAGE (V_{CEX}) ..... 50 V dc
OUTPUT SUSTAINING VOLTAGE (V_{CEsus}) ..... 35 V dc
OUTPUT CURRENT (I_O) ..... 1 A dc
POWER DISSIPATION (P_D):
- Up to 60°C ..... 1.5 W
- Above 60°C ..... Derate linearly at 16.6 mW/°C
- Up to 90°C with heat sink (PC Board) ..... 1.5 W
- Above 90°C with heat sink (PC Board) ..... Derate linearly at 25 mW/°C

AMBIENT TEMPERATURE RANGE:
- Operating ..... -40 to +105°C
- Storage ..... -55 to +150°C

MAXIMUM JUNCTION TEMPERATURE ($T_{\theta J}$) ..... +150°C
MAXIMUM THERMAL RESISTANCE:
- Junction-to-Air, θ_{J-A} ..... 60°C/W
- Junction-to-Case, θ_{J-C} to pins 4, 5, 12, 13 at seat ..... 12°C/W

LEAD TEMPERATURE (DURING SOLDERING):
- At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

ELECTRICAL CHARACTERISTICS at T_A = -40°C to +105°C, V_{CC} = 5 V Except as Noted

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Output Leakage Current (I_{CEX}) V_{CE} = 50 V V_{IN} = 0.8 V	—	100	μA
Output Sustaining Voltage $V_{CE(sus)}$ I_C = 100 mA V_{IN} = 0.8 V	30	—	V
Collector Emitter Saturation Voltage $V_{CE(sat)}$ I_C = 100 mA V_{IN} = 2.4 V	—	0.25	V
I_C = 400 mA V_{IN} = 2.4 V	—	0.6	V
I_C = 600 mA V_{IN} = 2.4 V	—	0.8	V
Input Low Voltage V_{IL}	—	0.8	V
Input Low Current I_{IL} V_{IN} = 0.8 V	—	±10	μA
Input High Voltage V_{IH} I_C = 600 mA	2	—	V
Input High Current I_{IH} I_C = 700 mA; V_{IN} = 4.5 V	—	10	μA
Supply Current - All Outputs ON, $I_{CC(ON)}$ I_C = 700 mA; $V_{CC} = V_{IH}$ = 5.5 V	—	80	mA
Supply Current - All Outputs OFF, $I_{CC(OFF)}$	—	5	mA
Clamp Diode Leakage Current I_R V_R = 50 V	—	100	μA
Clamp Diode Forward Voltage V_F IF = 1 A	—	1.8	V
IF = 1.5 A	—	2.5	V
Turn-On Delay t_{PHL} Turn-Off Delay t_{PLH}	—	20	μs

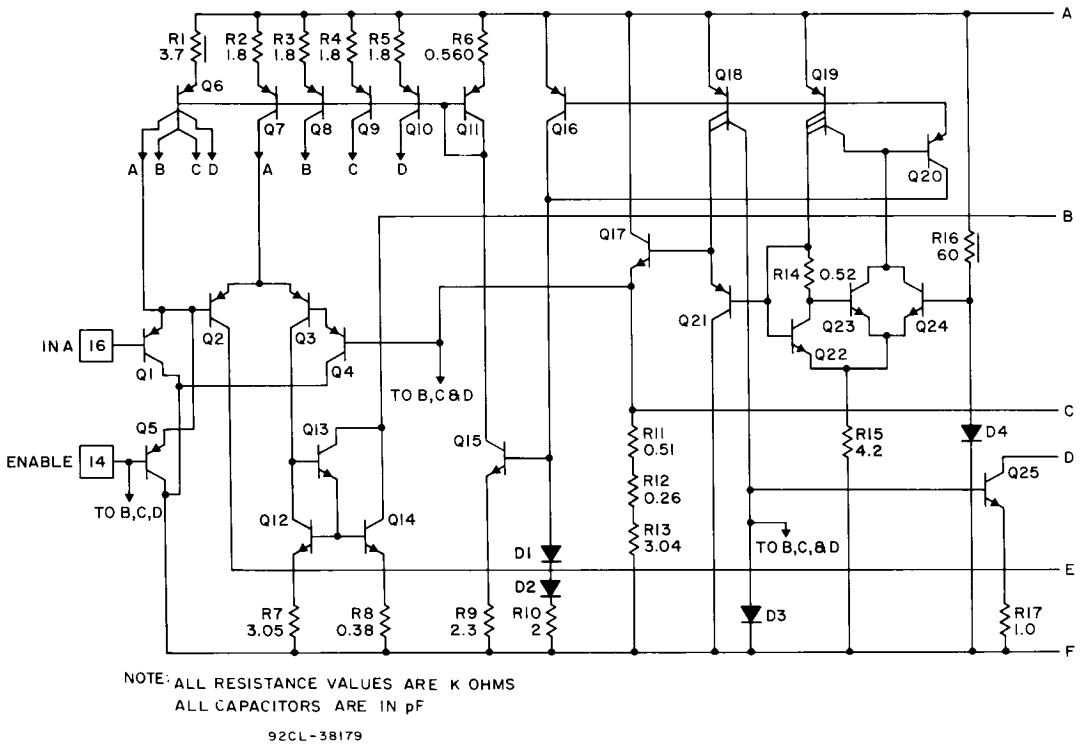


Fig. 3 - Schematic diagram of the CA3242E (Switch Section-A).
(Continued on next page).

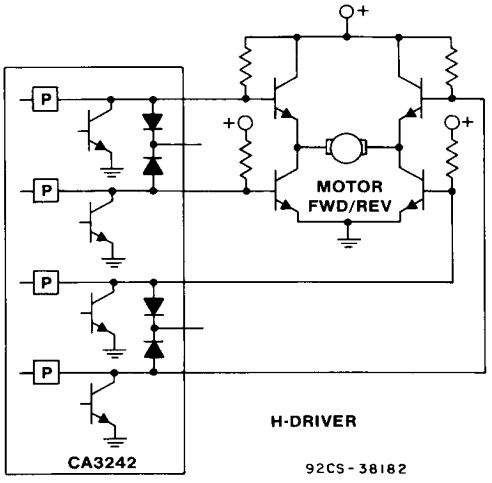


Fig. 4 - Typical applications for the RCA CA3242 Quad Driver.

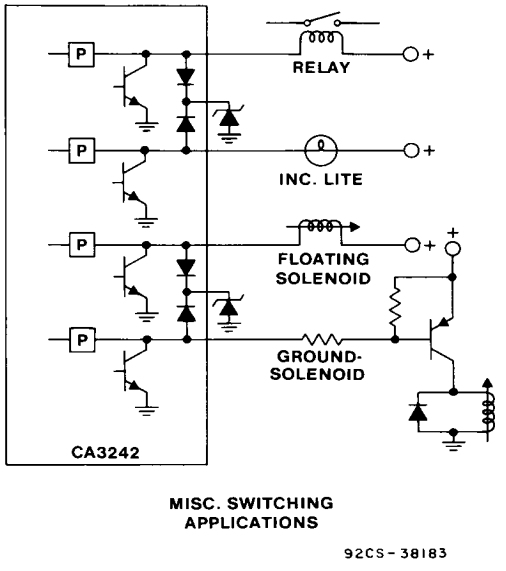


Fig. 5 - Typical applications for the RCA CA3242 Quad Driver.

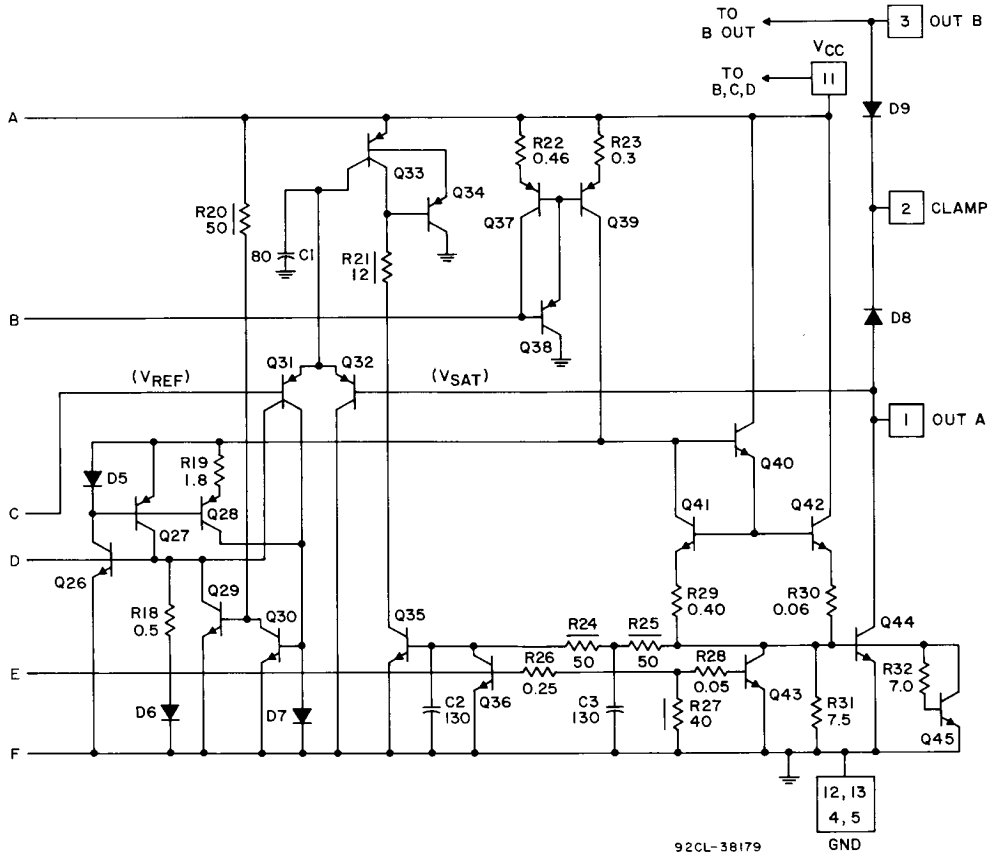


Fig. 3 - Schematic diagram of the CA3242E (Switch Section-A). (Continued from previous page).

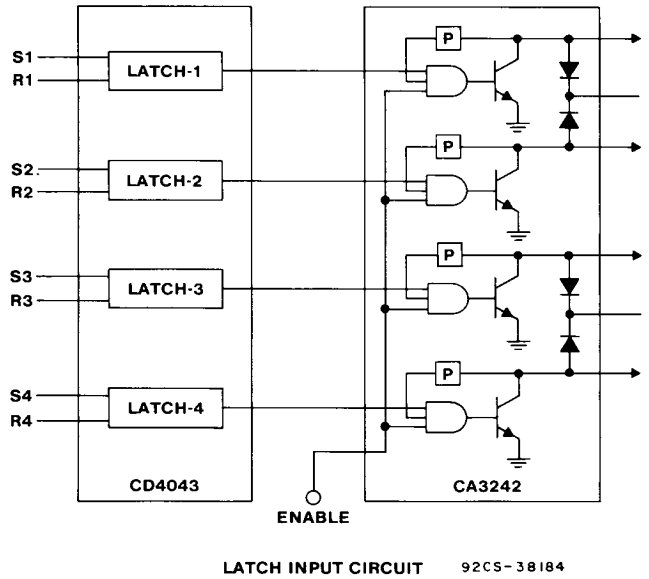
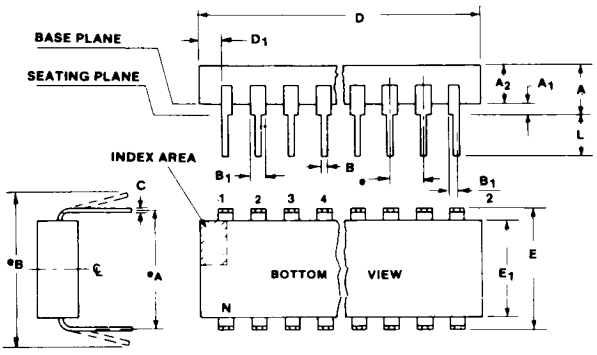


Fig. 6 - Typical applications for the RCA CA3242 Quad Driver.

DIMENSIONAL OUTLINE

E Suffix (JEDEC MS-001-AA)
16-Lead Dual-In-Line Plastic Package



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A_1	0.015	—	0.39	—	9
A_2	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.745	0.840	18.93	21.33	4
D_1	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	16		16		11

92CS-39900

Notes:

1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines, in Section 2.2.
2. Protrusions (flash) on the base plane surface shall not exceed 0.010 in. (0.25 mm).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions
   $1, N, \frac{N}{2}, \frac{N}{2}+1.$
4. Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 in. (0.25 mm).
5. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
6. Dimension E_1 does not include mold flash or protrusions.
7. Package body and leads shall be symmetrical around center line shown in end view.
8. Lead spacing e shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
9. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 in. (0.25 mm) diameter for dimension e_A.
10. e_B is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
11. N is the maximum number of lead positions.
12. Dimension D_1 at the left end of the package must equal dimension D_1 at the right end of the package within 0.030 in. (0.76 mm).
13. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

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