

# GD4022B

## 4-STAGE DIVIDE-BY-8 JOHNSON COUNTER

**DESCRIPTION** — The 4022B is a 4-Stage Divide-by-8 Johnson Counter with eight glitch free active HIGH Decoded Outputs ( $O_0-O_7$ ), an active LOW Output from the most significant flip-flop ( $\overline{O_4-7}$ ), an active HIGH and an active LOW Clock Input ( $CP_0, \overline{CP_1}$ ) and an overriding asynchronous Master Reset Input (MR).

The counter is advanced by either a LOW-to-HIGH transition at  $CP_0$  while  $\overline{CP_1}$  is LOW or a HIGH-to-LOW transition at  $\overline{CP_1}$  while  $CP_0$  is HIGH (see Functional Truth Table). When cascading the counters, the  $\overline{O_4-7}$  Output (which is LOW while the counter is in states 4, 5, 6 and 7) can be used to drive the  $CP_0$  Input of the next 4022B. A HIGH on the Master Reset Input (MR) resets the counter to Zero ( $O_0 = \overline{O_4-7} = \text{HIGH}, O_1 - O_7 = \text{LOW}$ ) independent of the Clock Inputs ( $CP_0, \overline{CP_1}$ ).

- CLOCK EDGE-TRIGGERED ON EITHER A LOW-TO-HIGH TRANSITION OR A HIGH-TO-LOW TRANSITION
- BUFFERED CARRY OUTPUT ( $\overline{O_4-7}$ ) AVAILABLE FOR CASCADING
- BUFFERED FULLY DECODED OUTPUTS

**PIN NAMES**

$CP_0$	Clock Input (L→H Edge-Triggered)
$\overline{CP_1}$	Clock Input (H→L Edge-Triggered)
MR	Master Reset Input
$O_0-O_7$	Decoded Outputs
$\overline{O_4-7}$	Carry (Active LOW) Output

**FUNCTIONAL TRUTH TABLE**

MR	$CP_0$	$\overline{CP_1}$	OPERATION
H	X	X	$O_0 = \overline{O_4-7} = \text{H}; O_1-O_7 = \text{L}$
L	H	H→L	Counter Advances
L	L→H	L	Counter Advances
L	L	X	No Change
L	X	H	No Change
L	H	L→H	No Change
L	L→L	L	No Change

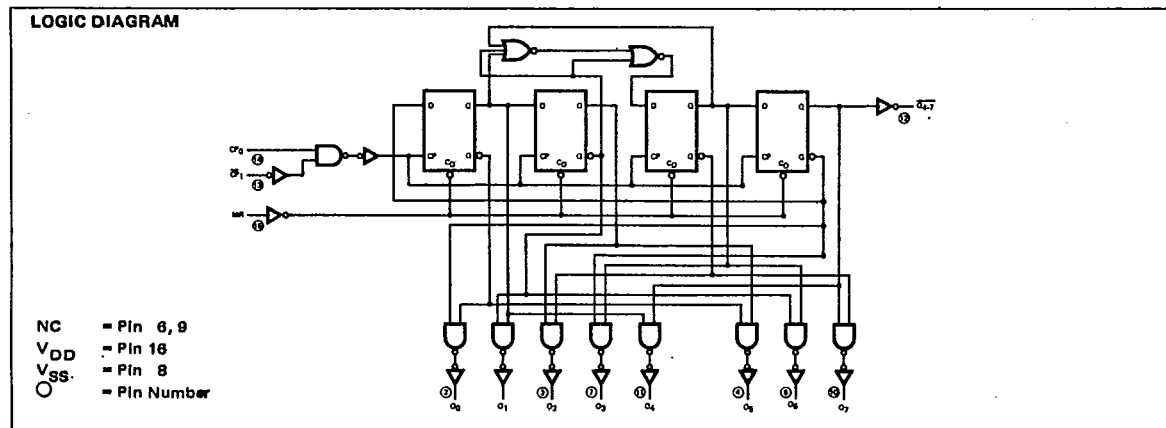
H = HIGH Level  
 L = LOW Level  
 L→H = LOW-to-HIGH Transition  
 H→L = HIGH-to-LOW Transition  
 X = Don't Care

**LOGIC SYMBOL**

$V_{DD}$  = Pin 16  
 $V_{SS}$  = Pin 8  
 NC = Pin 6, 9

**CONNECTION DIAGRAM  
DIP (TOP VIEW)**

**NOTE:**  
 The SO Package has the same pinouts (connection Diagram) as the Dual In-line package



GS CMOS · GD4022B

DC CHARACTERISTICS:  $V_{DD}$  as shown,  $V_{SS} = 0$  V (See Note 1)

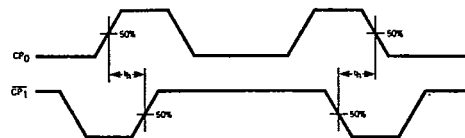
SYMBOL	PARAMETER	LIMITS									UNITS	TEMP	TEST CONDITIONS	
		$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V						
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX				
$I_{DD}$	Quiescent Power Supply Current	XC			20			40			80	$\mu$ A	MIN, 25°C	All inputs at 0 V or $V_{DD}$
					150			300			600		MAX	
	XM			5			10			20	$\mu$ A	MIN, 25°C		
				150			300			600		MAX		

AC CHARACTERISTICS AND SET-UP REQUIREMENTS:  $V_{DD}$  as shown,  $V_{SS} = 0$  V,  $T_A = 25^\circ$ C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
$t_{PLH}$	Propagation Delay, $CP_0$ or $\overline{CP_1}$ to $O_n$		245			95			60		ns	$C_L = 50$ pF, $R_L = 200$ k $\Omega$ Input Transition Times < 20 ns
$t_{PHL}$	Propagation Delay, $CP_0$ or $CP_1$ to $\overline{Q_{4,7}}$		190			75			50		ns	
$t_{PLH}$	Propagation Delay, MR to $O_n$		130			55			40		ns	
$t_{PHL}$	Propagation Delay, MR to $\overline{Q_{4,7}}$		110			45			35		ns	
$t_{TLH}$	Output Transition Time		70			35			25		ns	
$t_{THL}$	Output Transition Time		70			35			25		ns	
$t_{wCP}$	Min. $CP_0$ or $\overline{CP_1}$ Pulse Width		35			15			10		ns	
$t_{wMR}$	Minimum MR Pulse Width		35			15			10		ns	
$t_{rec}$	MR Recovery Time		10			5			5		ns	
$t_h$	Hold Time, $CP_0$ to $CP_1$		70			25			15		ns	
$t_h$	Hold Time, $\overline{CP_1}$ to $CP_0$		85			30			20		ns	
$f_{MAX}$	Input Count Frequency (Note 3)		6			16			24		MHz	

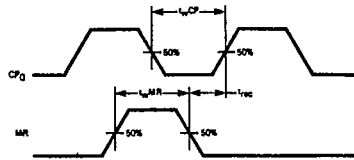
NOTES:

- Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
- Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
- For  $f_{MAX}$ , input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
- It is recommended that input rise and fall times to the Clock Input be less than 15  $\mu$ s at  $V_{DD} = 5$  V, 4  $\mu$ s at  $V_{DD} = 10$  V, and 3  $\mu$ s at  $V_{DD} = 15$  V.



HOLD TIMES,  $CP_0$  TO  $\overline{CP_1}$  AND  $\overline{CP_1}$  TO  $CP_0$

NOTE: Note: Hold Times are shown as positive values, but may be specified as negative values.



MINIMUM PULSE WIDTHS FOR CP AND MR AND RECOVERY TIME FOR MR

CONDITIONS:  $CP_1 =$  LOW while  $CP_0$  is triggered on a LOW-to-HIGH transition.  $t_{wCP}$  and  $t_{rec}$  also apply when  $CP_0 =$  HIGH and  $CP_1$  is triggered on a HIGH-to-LOW transition.